Progress on the RCU Prototyping

Bernardo Mota
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Overview

Architecture
Trigger and Clock Distribution
Instruction Sequences
Current Capabilities
Present Status

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Overall Frontend System
ALTRO Interface: Trigger Modes

1. **L1-L2**
   - **External**
   - **IF_L1**
   - **L1&L2 filter**
   - Final Operation Mode

2. **L1 only**
   - **L1**
   - **External**
   - **IF_L1**
   - Test Beam Mode

3. **SWTRG**
   - **exec via DCS**
   - **Data via DDL**
   - **L1**
   - **programmable drift time**
   - RCU
   - SWTRG
   - WAIT
   - **L2**

4. **17/05/04 ALICE TPC Meeting Bernardo Mota (CERN PH/ED)**
# Instruction Codebook

### Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Code</th>
<th>16'hxxxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>JUMP/LOOP</td>
<td>4'h0</td>
<td></td>
</tr>
<tr>
<td>RS_STATUS</td>
<td>4'h1</td>
<td></td>
</tr>
<tr>
<td>RS_L1CNT</td>
<td>4'h2</td>
<td></td>
</tr>
<tr>
<td>RS_L2CNT</td>
<td>4'h3</td>
<td></td>
</tr>
<tr>
<td>CHRDO</td>
<td>4'h6</td>
<td></td>
</tr>
</tbody>
</table>

### Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>4'hx</th>
<th>Channel Add.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMREAD</td>
<td>4'h7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMWRITE</td>
<td>4'h8</td>
<td>3'hx</td>
<td>bcast, chann. add.</td>
</tr>
<tr>
<td>END</td>
<td>4'h9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WAIT</td>
<td>4'ha</td>
<td></td>
<td>Nbr. Cycles CLK</td>
</tr>
<tr>
<td>IF_TRIGGER</td>
<td>4'hb</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Examples of Instruction Sequences

Accessing in infinite loop a given ALTRO Register

Scope probing for electrical integrity check

Testing Multi-Event Buffer & Readout with software trigger

- SWTRG (L1)
- WAIT
- WPINC (L2)
- CHRDO (Readout)
- RPINC
- *END*

From ALTROs to DAQ w/ software trigger
Examples of Instruction Sequences

Cardio Test

| READ HWADD ‘0’ |
| READ HWADD ‘1’ |
| - - - |
| READ HWADD ‘i-1’ |
| READ HWADD ‘i’ |
| *END* |

Which cards are responding to basic register access?

Test Beam Mode

- IF_TRIGGER (L1)
- CHRDO (Readout)
- RPINC
- JUMP

From ALTROs to DAQ w/ external L1-trigger:

- ADC sampled data
- Pattern stimuli
Examples of Instruction Sequences

Checking ALTRO Pedestal memory access in a fast way

Pedestal Memory Test

| PMWRITE | PMREAD | *END*
|---------|--------|--------|

Read Error register for mismatch error
Configuration and Readout Time

Overall configuration data: 7MByte/RCU - Worst case scenario:

- 3200 active channels
- 1000 samples/channel

Both paths

<1s

0.7s

3s

Transporter to DAQ scripts

Transporter to DCS scripts

RCU

buffer

FEC

FEC

Readout: 3ms
Active Channel / FEC List

16bit = 1 ALTRO chip

1: Good
0: Non-working

Channel not working will not be readout

Active Channel List

Active FEC List

32bit = max number of FEC / RCU

Updated by Slow control

Improving readout efficiency by storing the current status of one channel or board

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Current Trigger and Clock Distribution

- Trigger Input
  - Clock
  - L1-trigger
  - Trig.Messages

- VME crate
  - CORBO Module
  - TTC VI
  - TTC VX

- PC
  - ethernet

- RCU board
  - TTC chip
  - FPGA
  - 10MHz
  - 40MHz
  - busy signal
Operation in High Trigger Rate

- 4.7KHz Event Rate
- 80MByte/s

Conditions:
- 100 samples/channel
- 128 channels
- 40MHz Readout clk
- 10MHz Sampling clk

Exercise of full Readout Chain was performed successfully at KHz range trigger
Present Status

RCU Development

√ System fully tested and operational:

- 2 branches (12 + 13 frontend cards) in a total of 3200 channels
- DCS board running Linux on ARM processor and Ethernet link (Torsten Alt talk)
- DAQ with both DATE system and lower level script language for config.
- Communication between RCU and HLT fully operational
- Installed in the T10 Area, ready for beam (Roberto Campagnolo talk)

√ ALTRO Configuration tested using both the DCS board and the DDL link

√ Slow Control through I²C fully operational measuring Tₒ, Currents and Voltages (Carmen Gonzalez Gutierrez talk)

✗ Configuration of the RCU firmware from the DCS Board close to completion

? Improvement in readout time by a factor of 2: Replication of readout logic