ALICE TPC Collaboration Meeting

PASA Bulk Test

Status Update and Preliminary Results

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PASA Bulk Test

U.Bonnes  TU Darmstadt

for Cagliari TPC Meeting 16/17.05.2004

• Status

  – 31.760 packaged Chips from production run delivered to Darmstadt end of March
  – About 5 wafers not packaged by AMS due to bad parameters seen by process monitoring (PMOS transistors ?)
  – Test fixture, PC with software and about 10.000 chips transported by car to LUND
  – Communication with robot added to software there
• **Status**

  - Test socket changed from Clamp Shell to pressured air actuated Open Top Socket
  - New calibration for this socket was needed
  - Robot adapted by Lund to handle changed tray (60 vs. 48 chips) and changed socket
  - New PC (Athlon 3000+) needs about 13 seconds per chip, robot needs about 20 seconds for handling
  - Robot can handle 5 to 6 full tray with new chips and runs about 3 hours to test and sort them
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• Status

  – 835 tray in total
  – Since April 16, Lund is running the Test with mostly 4 tray change procedures per day, even on weekends
  – Switch from test of engineering run to production run already done, nearly on the fly
  – First Socket broke after around 35,000 insertions
  – Many thanks to the Lund people for that great work and cooperation
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• Sorting criterias
  – Few chip show gross errors (high current, no gain) and should be declared “non functional”
  – All other chips have close distribution in peaking time and an even smaller distribution in gain inside one run
  – Offset voltage fluctuations is noticable, has impact on dynamic range and is not correctable by software
  – Try to keep the sorting prodecure simple (few classes),
  – Try to satisfy Alice needs with the applied sorting criterias (35.600 + 10 % spare + X % stock)
• Choosen Limits

  – allow +/- 5% gain tolerance around estimated mean for given run
  – allow +/- 6% peaking time tolerance
  – allow +/- 50 mV tolerance in Offset voltage
  – Looking back, offset voltage mean was estimated about 2 mV too high
• Production versus Engineering Run
  - Gain: - 2.1% (13.11 versus 13.29 mV/fC)
  - Peaking Time: +3.8% (162.7 versus 156.7 ns)
  - Offset Voltage: -1 mV (nearly the same)
  - Offset Voltage distribution: +2%
Gain vs Peaking Time (Eng.)

Peaking Time (ns)

Gain (mV/fC)
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• Results

  – 36.172 Chips tested with robot so long (May 14)
  – 1.8 % non functional against 3.6 % reported in Heidelberg (better socket contact?, less manual handling and so less ESD damage?)
  – 10.1% out of tolerance (will slightly go up)
  – Expect around 43.000 good chips in total

• Recycle “out of tolerance” chips

  – About 70 % of the out of tolerance can be recuperated by resorting in two additional classes (same offset span, but different center ( +/- 15 mV))