Front-End Card Interface of the RCU

- Readout network (ALTRO Interface)
- Local Slow Control
Readout network

1. **Provides communication between the RCU and the ALTRO chips for Configuration and Readout.**
2. **Provides a simple and direct interface, as slave, to the DDL-SIU, DCS -Trigger Board and the RCU master.**

- 4 different memories
  - *INSTRUCTION MEM* -> ALTRO commands and macros
  - *DATA MEM* -> Double “ping-pong” data buffer. One channel black event/buffer
  - *PEDESTAL MEM* -> Replica of ALTRO Ped. Memory. Used for both test and configuration purposes
  - *RESULTS MEM* -> Stores value of registers read from ALTRO

- Decoder
- Counter Table
- FSM
Readout Network: \textit{FSM Hierarchy}

- Decoder
- Instruction Memory
- Master FSM
- FSM 0
- FSM 1
- ... FSM N
- Slave FSM
- ALTRO Bus
- Data Memory
- Results Memory
- Pedestal Memory
**Readout network: RCU Macro Instructions**

*Sequence used in hardware test*

<table>
<thead>
<tr>
<th>INSTRUCTION MEMORY</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Addressing the BC</td>
<td>Write Configuration Status of the BC to enable the ALTROs and the PASA</td>
</tr>
<tr>
<td>Data to BC</td>
<td>Configure the ALTROs with the number of samples per event</td>
</tr>
<tr>
<td>Addressing TRG CONFIG</td>
<td>Macro Writing a full ALTRO Pedestal Memory</td>
</tr>
<tr>
<td>Data of TRG CONFIG</td>
<td>Configure ALTRO pedestal memory to generate event from data previously stored</td>
</tr>
<tr>
<td>PMWRITE</td>
<td></td>
</tr>
<tr>
<td>Address of Pedestal MEM Mode Register</td>
<td></td>
</tr>
<tr>
<td>Data of Pedestal MEM Mode</td>
<td></td>
</tr>
<tr>
<td>SWTRG</td>
<td>Send L1 Trigger to the processing chain</td>
</tr>
<tr>
<td>WAIT</td>
<td></td>
</tr>
<tr>
<td>WPINC</td>
<td>Send L2 Trigger</td>
</tr>
<tr>
<td>CHRDO</td>
<td>Readout of the specific channel</td>
</tr>
<tr>
<td>END</td>
<td></td>
</tr>
</tbody>
</table>
Local Slow Control

- Dedicated bus connection RCU – BC (I²C Protocol)
- Configure the power state of all FECs
- Monitor power and temperature
- Interrupts
- Read status parameters (errors)
Slow Control: block diagram

RCU

I^2C Master

Instruction
MEM

Result
MEM

Readout Network

I^2C

scl
sda in
sda out

RCU

FECs
RCU is able to  
- write and read the Register Table  
- send commands

Slow Control: block diagram
Board Controller (FEC)
# Registers Table

## Configuration Status Registers

<table>
<thead>
<tr>
<th></th>
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<th></th>
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<td>01</td>
<td>T_TH</td>
<td>Temperature Thr.</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Maximum Temperature Threshold</td>
</tr>
<tr>
<td>02</td>
<td>AV_TH</td>
<td>AV threshold</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Minimum Analog Voltage Threshold</td>
</tr>
<tr>
<td>03</td>
<td>AC_TH</td>
<td>AC threshold</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Maximum Analog Current Threshold</td>
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<tr>
<td>04</td>
<td>DV_TH</td>
<td>DV threshold</td>
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<td>Y</td>
<td>Minimum Digital Voltage Threshold</td>
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<tr>
<td>08</td>
<td>TEMP</td>
<td>Temperature</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Temperature Value</td>
</tr>
<tr>
<td>09</td>
<td>AV</td>
<td>Analog Voltage</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Analog Voltage Value</td>
</tr>
<tr>
<td>0A</td>
<td>AC</td>
<td>Analog Current</td>
<td>10</td>
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<tr>
<td>0B</td>
<td>DV</td>
<td>Digital Voltage</td>
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<tr>
<td>0C</td>
<td>DC</td>
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</tr>
<tr>
<td>10</td>
<td>L1CNT</td>
<td>L1 Counter</td>
<td>16</td>
<td>R</td>
<td>N/A</td>
<td>Number of L1 Trigger Received</td>
</tr>
<tr>
<td>11</td>
<td>L2CNT</td>
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<td>16</td>
<td>R</td>
<td>N/A</td>
<td>Number of L2 Trigger Received</td>
</tr>
<tr>
<td>12</td>
<td>SCLKCNT</td>
<td>Sampling clk counter</td>
<td>16</td>
<td>R</td>
<td>N/A</td>
<td>Sampling Clock counter</td>
</tr>
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<td>13</td>
<td>DSTBCNT</td>
<td>Data Strobe Counter</td>
<td>8</td>
<td>R</td>
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<td>Number of Data Strobe in the last Read - Out</td>
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<tr>
<td>14</td>
<td>CSR0</td>
<td>Configuration Status 0</td>
<td>14</td>
<td>R/W</td>
<td>Y</td>
<td>Interrupt – Mask Register</td>
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<tr>
<td>15</td>
<td>CSR1</td>
<td>Configuration Status 1</td>
<td>14</td>
<td>R</td>
<td>N/A</td>
<td>Error Status Register</td>
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<tr>
<td>16</td>
<td>CSR2</td>
<td>Configuration Status 2</td>
<td>16</td>
<td>R/W</td>
<td>Y</td>
<td>Card Configuration Status Register</td>
</tr>
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## Registers Table, commands

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<tr>
<td>18</td>
<td>CNTLAT</td>
<td>Counters Latch</td>
<td>-</td>
<td>W</td>
<td>Y</td>
<td>Latch L1, L2, SCLK counters</td>
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<tr>
<td>19</td>
<td>CNTCLR</td>
<td>Counters Clear</td>
<td>-</td>
<td>W</td>
<td>Y</td>
<td>Clear L1, L2, SCLK counters</td>
</tr>
<tr>
<td>1A</td>
<td>CSR1CLR</td>
<td>Config Status Reg1 Clear</td>
<td>-</td>
<td>W</td>
<td>Y</td>
<td>Clear Error Status Register</td>
</tr>
<tr>
<td>1B</td>
<td>ALRST</td>
<td>ALTRO Reset</td>
<td>-</td>
<td>W</td>
<td>Y</td>
<td>Reset all the ALTROs</td>
</tr>
<tr>
<td>1C</td>
<td>BCRST</td>
<td>BC Reset</td>
<td>-</td>
<td>W</td>
<td>Y</td>
<td>Set default values in registers of BC</td>
</tr>
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<td>1D</td>
<td>STCNV</td>
<td>Start Conversion mADC</td>
<td>-</td>
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*from ADC (AD7417):* 4 channel ADC with an on-chip Temperature sensor
Readout of the ADC

I²C Master, FEC

FSM

Instruction MEM

Data address

ST_CNV command

Temp and Voltage Registers

Registers Table

I²C

scl

sda

ADC

(Slave I²C)

Slow Control OR ALTRO bus

BC
SC Interface: *Sequence used in hardware test*

**INSTRUCTION MEMORY, RCU**
- Send FEC address
- Send command ST_CNV
- Read CSR1
- Read DC
- Read DV
- Read AC
- Read AV
- Read TEMP
- Read CSR2
- Read CSR0
- Write and read back DC_TH
- Write and read back DV_TH
- Write and read back AC_TH
- Write and read back AV_TH
- Write and read back T_TH
- Send command ST_CNV

**RESULT MEMORY, RCU**
- T_TH
- AV_TH
- AC_TH
- DV_TH
- DC_TH
- CSR0
- CSR0
- TEMP
- AV
- AC
- DV
- DC
- CSR1

ADC starts to read Temp and Voltages
Read the different thresholds
Read Configuration Status 0 : Interrupt Mask
Read Configuration Status 2 : Card Configuration
Read Temperature from ADC
Read Analog Voltage from ADC
Read Analog Current from ADC
Read Digital Voltage from ADC
Read Digital Current from ADC
Read Configuration Status 1 : Error Status
Test Set - up

- Using the R&C backplane with several FECs and the new RCU board
- Status Analyzer
- Pattern generator
- R/O clock generated with a 40 MHz quartz oscillator
- Sampling clock is derived from r/o clk using the FPGA PLL
- Firmware uploaded using the ALTERA Byte Blaster

- Some pictures ...
Connectors RCU – backplane

FPGA:
- ALTRO bus protocol
- Local Slow Control

RCU

FECs
Adaptor Card:
RCU connectors – State Analyzer
Stimuli from pattern generator & Acquisition of signals to state analyzer
Present Status

- **Readout Network**
  - Basic FEC communication functionality, tested **OK**
    - Read/Write ALTRO registers
    - Configure Pedestal Memories
    - Send L1-L2 triggers and Event Readout
  - No electrical or timing problems were detected **OK**

- **Slow Control**
  - Access to the Register Table to write and read from RCU, tested **OK**
  - Answers to the commands, tested **OK**

- **Still to be accomplished: X**
  - Integration with other RCU modules
  - Testing of the full chain: PASA -> DDL/DCS
  - Answers to the interrupt line from the FEC