Front End Card and Readout Backplane Status

Alice TPC Meeting – Heidelberg 12-13 February 2004

Roberto Campagnolo

October – December 03: 50 FECs from Note-Xperi (Lund) delivered and tested at CERN:

- 3 class of errors:
  1. Altros’ memory single bit stuck (6 chip out of 400) – expected, because the test procedure in Lund was not yet the complete one.
  2. Pasas’ single channel not working (1 chip out of 280) – baselines’ steady state wrong
  3. Errors in assembly: 6 Cards (12%)
Alice TPC Front End Card – status 2/2

- **January 04: Completion of the radiation test campaign in Oslo:**
  
  Last components irradiated (p-beam at 60 MeV):
  
  20 Tantalum capacitors from AVX and Kemet (2.2, 10, 15 and 22µF)
  
  (irradiated up to ~120 Krad, no variations in C and ESR)
  
  4 Schottky diodes from Philips (BAT54)
  
  (irradiated up to ~400 Krad, no variations in $V_\gamma$)
  
  4 BJT transistors from Motorola (MMBT2222ALT1)
  
  (irradiated up to ~400 Krad, variations of 10% in Vce-sat at ~120KRad)
  
  6 Voltage references from Micrel (LM4040-2.5; LM4041-1.2)
  
  (linear drift with irradiation for 2500mV: 1% output variation at ~45 Krad)
  
  (1225mV model: stable up to ~300 KRad)
  
  5 Operational Amplifiers from Texas Instruments (OPA4364AI)
  
  (spikes in output when irradiation reaches ~140KRad)

- **February 04: Launched production of 200 Cards (4.6% of Alice!)**
Radiation Tests (Oslo, past 19-20 January)

- Tantalum Capacitors
- 2222A BJTransistor
- BAT54 Schottky diode
- OPA4364 OA Buffers
- LM404X Ref Voltage

Roberto Campagnolo – CERN
Tantalum caps: AVX 15uF, 10 V

(Up to 120 KRad)
BJT MMBT2222ALT1

(volutions of 10 % in Vce-sat every ~140KRad)

Exposition Time ( ~ 21KRad/min)
Reference Voltages LM4040-2.5 and LM4041-1.2

(output stable within 0.3 %)

(1 % output variation @ 45 Krad)

(~21 Krad/min)
Exposition Time ( ~21 KRad/min)

Output Voltage

Series 1

(Output stable ‘till ~140 Krad)
Readout Backplane – Status

All the backplanes have been designed

No differences in the RCU connectors positions

( despite the different topology of the FECs)

Backplanes for C2 and C6 have been manufactured and tested (very good signal integrity)

Overall TPC : 36 trapezoidal sectors (216 crates)
Readout Backplane design

Technology:
4 Layers, Class 4, flexible PCB
(4 x 35µm Cu + 3 x 200µm FR4)

Electrical Characteristics:
• 76 ohm - Impedance controlled signal lines
• Low resistance (~10mOhm) and Low Inductance (~8nH) lines for Termination Voltage distribution
Backplane Mechanical aspects 1

- FEC SLOTS (13-slot branch)
- 19.5 cm
- service card integrated in the backplane
- FEC slot
- RCU slot
25 FECs Readout Partition (3200 channels)

- Readout and Control Backplane
- Backplane connectors for the Readout Control Unit
- I2C Connectors
- Power Supply Connectors
End of presentation
TPC IROC
Alice TPC Front End Card - schematics

- Front End Connectors w/ additional GND conn. → Detector PADs
- Back End Connectors → Backplane

**Modifications on:**
- Card Switch and re-Conf. !
- LDOs default state
- Board Controller
- ALTROs TSTMode addr’ing
- Clock signals ‘tap-off’
New Feature: FPGA re-conf. without ALTROs’ conf. losing

FPGA RE-CONF. TIMING PRINCIPLE:

- **CARD_SW**: 2.69 MICROSECONDS (CARD OFF)
- **BC_CONF** (FOLLOW CARD SW)
- **CONF_DONE**: 110 MICROSECONDS
- **INTERRUPT**: 110 MICROSECONDS
- **MPS_ENABLE**: 400 MICROSECONDS

**BC_CONF**

**CARD_SW** (ACTIVE HIGH)
- **CARD_SW_AUX** (FROM BACKPLANE CONNECTOR)
- **BC_INT** (ACTIVE LOW)
- **MPS_ERROR** (OPEN DRAIN - ACTIVE LOW)

FEC Power, re-Conf and Interrupt Control block
Low Drop Out Regulators Section
Acex 1K30 SRam FPGA based Board Controller
Tap-off resistors for M/Drop clock signals distribution