ALTRO Mass-Testing

ALTRO TEST SETUP at LUND
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Example - Distribution of digital Current

The majority of the chips are rejected for bit-stuck in the digital circuit.
Summary

• As of Yesterday 39 000 chips tested

• Yield of directly accepted chips is 82.5 %

• Testing of remaining 6000 chips and reverification of rejected chips (~7500) will be completed by March 15

• At present, test rate of about 1000 chips a day
TEST EQUIPMENT

TOP VIEW

- DEVICE UNDER TEST
- CARRIER BOARD
- CLAMSHELL TEST SOCKET

BOTTOM VIEW

- 1-CHANNEL DAC piggy-back board
- PROGRAMMABLE PULSE GENERATOR
- FPGA
  - Control
  - RCU interface

DARMSTADT TU

51 March 2004 Luciano Musa
PASA Mass-Testing

Distribution of the Conversion Gain measured in about 38400 channels

All good chips have a conversion gain within ~3% from the nominal value
All good chips have a peaking time within ~5% from the nominal value.
Summary

• 2500 PASAs (production lot) have been tested
• Yield of accepted chips is 96.4%
• 55000 chips to be tested (Lund): 22 March – 30 June
• Test rate: 2 chips / minute ⇒ 1000 chips / day (8h)
Faulty chips

- 18 chips with high current (> 2 x nom. Value)
- 4 chips with functional errors in all channels (large dist.)
- 4 chips with all channels main parameters off-limits
- 2 chips with high noise (> 1000 electrons)
- 61 chips with gain off limits (> 50% from nom value)

Majority of the chips with no response