Content

- Purpose and scope of a model for the readout electronics of the ALICE Detectors
- Some examples of modeling the R/O electronics: TPC, SPD, SDD, HMPID, TOF, MUON-ARM
- Description of the general R/O Model
- R/O characterization table
Purpose

- Study the ALICE read out: consistency and performance
- Common description of the Detector R/O electronics
- Optimization of the readout electronics: the MEB and dataflow organization is, for some detectors, still open (programmable devices)

Scope

- Model for the data Readout from the DETECTOR to the RORC
- Basic Readout Partition: readout electronics combined to one RORC
- Description Model: RTL (Register Transmission Level), algorithmic, stochastic
MODELING THE TPC READOUT ELECTRONICS (1/2)

FUNCTIONAL VIEW

216 RORCs (216 R/O Partitions)

Readout Time (RT) = 88 µs
Data Volume (DV) = 80MB
DV = F[μ(occ), σ]

Latency = 2.1 µs

MEB FULL ⇒ BUSY

<Readout time> = 5ms
Reset Time = 0
Latency = 2 µs

Multi-Event Buffer (MEB)
Fixed Length Buffer (FLB)
Random Access (RA)

Event generation

Strobe (event in)
readout/abort (event out)

BUSY = 88µs (DL)
RT = 88 μs
<DV> = 0.5MB
DV = F[μ(occ), σ]

Capacity = 8
Input Latency = 0
Output Latency: <5ms>, F(DV)
Reset Time = 0
I/O Type: FLB, RA

The system is busy when:
• Detector Latency after L0
• L1- MEB full
MODELLING THE SPD READOUT ELECTRONICS

FUNCTIONAL VIEW

- DET (PIXEL)
- AMP
- DISCR
- DLY LINE
- 4x1-bit REG
- OUTPUT REG
- PILOT

Fixed Length Buffer (FLB) FIFO

Input Latency
Output Latency
Reset Time

Readout Time = 256 $\mu$s

ABSTRACT VIEW

- DET
- L1 – DL
- L1 MEB
- L2 – DL
- L2 SEB
- L2 - IDL
- L2 MEB
- F2D - DL
- RORC

Input Latency
Output Latency
Reset Time

VME

GLINK

N (81920)
MODELLING THE SDD READOUT ELECTRONICS

FUNCTIONAL VIEW

- DET (SDD) -> AMP -> SCA (MEM) -> A/D -> MUX -> MEB (64 ch)
- AMBRA (64 ch)
- CARLOS (256 ch)
- CARLOS_rx (concentrator)

Readout time = 256μs
Reset Time = 0.2μs

L0

Readout Time = 1.6ms
Reset Time = 0.3μs

L1 x L2 (readout)
L1 + L2 (abort)

ABSTRACT VIEW

- DET -> L0 – DL -> L0 SEB -> L0 MEB -> F2D - DL -> RORC

L0

M E L O
MODELLING THE HMPID READOUT ELECTRONICS

FUNCTIONAL VIEW

GASSIPLEX

AMP

T/H

A/MUX

A/D

DILOGIC

REG

FIFO

DDL

RORC

L0

L1

L2

ABSTRACT VIEW

DET

L0 – DL

L0 SEB

L1 - DL

L1 SEB

L1 MEB

F2D - DL

RORC
MODELLING THE TOF READOUT ELECTRONICS

FUNCTIONAL VIEW

ON DETECTOR

DET (TOF) → AMP → DT DISCR → FEC (8 ch)

OFF DETECTOR

TDC (8 ch) → FIFO 16 EV → RAM <16> EV → FIFO

TRM (192 ch) – VME BOARD

L0 ‾ L1 ‾ L2

VME - CRATE

DRM (192 ch)

2nd VME

ABSTRACT VIEW

DET → L0 – DL → L0 MEB → L1 – DL → L1 MEB → L2 – DL → L2 MEB → F2D – DL → RORC
MODELLING THE MUON ARM READOUT ELECTRONICS

FUNCTIONAL VIEW

MANAS CHIP (16CH)

AMP

T/H

AMUX

A/D

ZS

MEM (1 EV)

MARC CHIP (64CH)

MEM 6-10 EV (5 DSPs)

CROCUS

DDL

RORC

MANU BOARD (64CH): 4 MANAS + 2ADCs + 1MARC

5 BUS x 20 MANU/BUS

32us

32us

100

L0 x L2 (readout)

L1 + L2 (abort)

ABSTRACT VIEW

DET

L0 – DL

L0 SEB

L0 MEB

F2D - DL

RORC
Data flows from the **Detector** (Data Source) to the **RORC** (Data Destination) through a number of analogue and digital **Storage Blocks** (SB). The Storage Blocks are organized in three levels: L0, L1 and L2. Upon arrival of the trigger signal, data is registered in the corresponding Storage Block.

Each storage block is composed by two **Storage Elements** (SE): a Single Event Buffer (SEB), which has the capacity to store a single event, and a Multi Event Buffer (MEB), which has the capacity to store several events.

The Storage Elements can be either analogue (track/hold, switched capacitors, etc.) or digital (flip-flop, RAM, FIFO, Circular Buffer, etc.). Each **Storage Element** will be characterized by the following parameters:

- **Capacity (CY)**: the number of events it can contain
- **Input Latency (IL)**: time to input an event in the SE
- **Output Latency (OL)**: time to output an event from the SE
- **Reset Time (RT)**: time to clear the SE after the event has been output or after a trigger abort
Subsequent Storage Blocks are linked by a Data Link (DL). There are in general four DLs: the level-0 DL (L0-DL), the level-1 DL (L1-DL), the level-2 DL (L2-DL) and the Front-end to DAQ DL (F2D-DL). The DL is characterized by its Transmission Latency (TL).

The IL, OL and TL parameters depend in general on the Data Volume (DV).

Other relevant parameters, for the characterization of the readout model, are the type and the input/output mechanism of the MEB.

**MEB TYPE:**

1. Fixed Length Buffer (FL)
2. Variable Length Buffer (VL)

**I/O Mechanism.** Two main schemes seem, so far, representative of all those employed in the different ALICE sub-detectors.

1. Random Access (RA)
2. First-In First-Out (FIFO)
### TPC (L. Musa)

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Preliminary!
## DESCRIPTION OF THE DETECTOR READOUT (1/4)

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### SDD (F. Tosello)

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_Preliminary!_
### DESCRIPTION OF THE DETECTOR READOUT (1/4)

#### MUON ARM (P. Courtart)

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#### Preliminary!

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#### Preliminary!
The system is busy when:

- after L0 for a time interval equal to the Detector Readout Time
- L1- MEB full

L1-MEB is full if: (Nr. of L2/accept) – (Nr. Of Events in RORC) = N