FEC – PCI based RCU tests

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this presentation is available on the website http://cern.ch/ep-ed-alice-tpc/
• Interface Cards Overview
• Tests and Measurements
• Future work
PCI based RCU and the Mezzanine Card

PCI CARD (PLDa)

FEC- INTERFACE (PMC CARD)

PMC-PCI

DDL-SIU CONNECTOR
PLDa based RCU test set-up

- Mezzanine with local termination
- PLDa PCI Interface
- 1 m GTL bus
- Termination card
Front End bus behaviour in the PLDa set-up

Test: Transmission of a repetitive pattern and verification at the receiving end

33 MHz CLOCK
PLDa-based RCU main hints

• April 01: Development of the 32 bit PMC mezzanine card (CERN)

• June 01: VHDL MODEL of the RCU’s interface to DDL-SIU (Bergen-J.Lien)

• July 01: Test of PCI-RCU + PMC mezzanine + DDL-SIU emulator:
  (transmission of single words to DDL-SIU emulator) (CERN and Bergen)

• October 01: VHDL code for the RCU’s interface to FEC (Bergen – J.Lien)

• November 01: Readout of events from a 32 bit Front End Card
  (CERN - R.Campagnolo)
PLDa-based RCU future work:

- Enhancement of the FPGA code in the PLDa card to include the new ALTRO communication protocol (Bergen)

- Development of a 40 bit mezzanine card (CERN)

by the end of February 2002