ALTRO CHIP

ALICE TPC Meeting

GSI (Darmstadt), December 11, 2001

OUTLINE

◆ Summary of the prototyping activities
◆ Chip main features
◆ System for the chip characterization
◆ Documentation
ALTRO CHIP – SUMMARY OF THE PROTOTYPING ACTIVITIES

FEE ARCHITECTURE

DETECTOR

L1: 5μs 200 Hz

FEC (Front End Card) - 128 CHANNELS (CLOSE TO THE READOUT PLANE)

8 CHIPS x 16 CH / CHIP

PASA

ADC

Digital Circuit

RAM

CUSTOM IC (CMOS 0.35μm)

CUSTOM IC (CMOS 0.25μm)

570132 PADS

pad plane

gating grid

anode wire

570132 PADS

Power consumption: < 40 mW / channel

L2: < 100 μs 200 Hz

DDL (4096 CH / DDL)

1 MIP = 4.8 fC
S/N = 30 : 1
DYNAMIC = 30 MIP

CSA SEMI-GAUSS. SHAPER
GAIN = 12 mV / fC
FWHM = 190 ns

10 BIT < 10 MHz

• BASELINE CORR.
• TAIL CANCEL.
• ZERO SUPPR.

MULTI-EVENT MEMORY

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ALTRO CHIP – SUMMARY OF THE PROTOTYPING ACTIVITIES

◆ 1st prototype (‘98):
  - Digital circuit: pedestal subtraction, zero suppression, data formatting, data memory (512 x 10-bit words)
  - Implementation with FPGAs (1ch / FPGA) for the readout of FTPC (NA49)

◆ 2nd prototype (‘99):
  - Digital circuit: pedestal subtraction, zero suppression, data format, data memory (768 x 10-bit words)
  - 4 channels: (6 x 9 mm²)
  - AMS CMOS 0.6 um
  - Fully working

◆ 3rd prototype (‘01):
  - Mixed analogue-digital circuit: ADC, pedestal correction and subtraction, tail cancellation, zero suppression, data formatting, data memory (4K x 10-bit words)
  - 16 channels - ST CMOS 0.25um
  - Contract procurement: Jul ‘01
  - Submission: Sep ‘01
  - Delivery (50 packaged samples): Jan ‘02
  - Testing: Jan – Feb ‘02
ALTRO CHIP – SUMMARY OF THE PROTOTYPING ACTIVITIES

1998
channels per chip: 1
ADC: 1 external
Digital Filter: no

1999
channels per chip: 4
ADC: 4 external
Digital Filter: no

2001
channels per chip: 16
ADC: 16 internal
Digital Filter: yes

External ADCs (fallback solution)
Integrated ADCs

4 cards
16 ch
135 mm

4 PQFP 100
8 SSOP 28
24 mm
**ALICE TPCE READOUT CHIP (ALTRO-16)**

**SAMPLING CLOCK 20 MHz**
**READOUT CLOCK 40 MHz**

16-ch signal digitizer and processor
- **HCMOS7 0.25 µm (ST)**
- area: 64 mm²
- power: 29 mW / ch
- **PACKAGE: TQFP176**
- SEU protection (Hamming)
ALTRO CHIP – CIRCUIT MAIN FEATURES

CORE BUILD-UP

interface

register block

pedestal memory manager

data memory manager

trigger manager

16 CHROL

ADC Block 0

ADC Block 1

output registers

digital (ADC clock)
digital (Readout clock)
ALTRO CHIP – CIRCUIT MAIN FEATURES

CHANNEL BUILD-UP

adc data
individual config

adc data
individual config

adc data
individual config
common config

CHROL 0

CHROL 1

CHROL 15

reg out
16

40 memory out
ALTRO CHIP – CIRCUIT MAIN FEATURES

CHANNEL DATA PATH

From ADC

- pedestal / pattern substraction
- 2's C
- 3rd order IIR filter
- 2's C
- adaptive baseline correction
- zero suppression

10

ADC clock

10

Readout clock

10

flag

data formatting

40

write

memory

40

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ALIROOT CLUSTERS + BASELINE PERTURBATIONS

Simulated baseline perturbation:
- electronics temp. variation (ramp-up)
- gating grid switching (systematic)
- power supply instability
- pick-up noise

FRONT-END SIGNAL PROCESSING
INPUT SIGNAL

AFTER 1st BASELINE CORRECTION

AFTER TAIL CANCELLATION

AFTER 2nd BASELINE CORRECTION

FRONT-END SIGNAL PROCESSING

ALTRO CHIP – CIRCUIT MAIN FEATURES

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ALTRO CHIP – CIRCUIT MAIN FEATURES

FRONT-END SIGNAL PROCESSING

INPUT SIGNAL

EVENT 2

AFTER 1st BASELINE CORRECTION

EVENT 2

AFTER TAIL CANCELLATION

EVENT 2

AFTER 2nd BASELINE CORRECTION

EVENT 2

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DIGITAL TAIL CANCELLATION PERFORMANCE

ALTRO CHIP – CIRCUIT MAIN FEATURES

Filter input and threshold

Filter output and fixed threshold
ALTRO CHIP – CIRCUIT MAIN FEATURES

LAYOUT AND PACKAGE

- ADC Channel 0
- ADC Channel 7
- Data Memory 1K x 40
- Processing Logic
- Pedestal Memory 1K x 10

Dimensions:
- 7.7 mm
- 24 mm
- 8.3 mm
- 14.1 mm
- 12 mm

Package: TQFP 176
PACKAGE AND PINOUT
The layout of the chip has been optimised to minimise the influence of the digital circuitry on the integrated ADCs.

- Supply (VCC / GND) for the digital core
- Supply (VCC / GND) for the ADC

The supply voltages for the PASA are distributed on a different plane.
ALTRO CHIP – SYSTEM FOR THE CHIP CHARACTERIZATION

Test set-up for the characterization of the ALTRO prototype

Status:
- Analogue Daughter Cards: ready
- Analogue Test Board: delivered in wk 49 - test in wk 50 and 51
- Digital Test Board: delivery in wk 50 – test in wk 51
- FPGA logic: ready
- PC software: basic tests routines ready
DOCUMENTATION AVAILABLE ON THE WEB

http://cern.ch/ep-ed-alice-tpc

- **ALTRO User Manual**
- **Interface Module** (Verilog RTL description)
- **Interface Driver** (Verilog behavioral description)