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ALICE TPC READOUT CHIP (ALTRO-16)

MAX SAMPLING CLOCK 40 MHz
MAX READOUT CLOCK 60 MHz

16-ch signal digitizer and processor
- HCMOS7 0.25 μm (ST)
- area: 64 mm²
- power: < 20 mW / ch
- prototype delivery: Feb ‘02
- 300 samples fully tested
ALTRO Test Setup

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ALTRO Test Board

- Analogue input signal
- 16 x differential linear drivers
- Altro chip under test
- Logic analyzer interface
- Power regulation
- Clock & trigger signals
- PC interface
- Test controller (FPGA)
16 channels in one shot
Effective Number of Bits (ENOB)

1MHz SINE WAVE

400 measurements with 1000 samples / measurement

THE ADC SHOWS ONLY THE QUANTIZATION ERROR
ENOB vs Frequency

Effective Number of Bits vs Input Frequency

Quartz Jitter:
25ps r.m.s.
100ps absolute

Amplitude Uncertainty:
\[
\frac{jitter}{4 \cdot f_{in}} \cdot 2^{10}
\]

0.5 bits at 4.8 MHz
Differential and Integral Non-Linearity
Chip Performance

ENOB vs Analog Vcc

ENOB vs Duty Cycle

ENOB vs Sampling Frequency

Digital Power Consumption vs Sampling Frequency

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Crosstalk and Digital Noise

DIGITAL NOISE

Readout Clock below -78 dBc (WC)

Bus interference below -65 dBc (WC)

CHANNEL-TO-CHANNEL CROSSTALK

\[
\begin{align*}
F_{in} = 1 \text{ MHz} & \quad 0.05 \text{ LSB rms} \quad (-80 \text{ dBc}) \\
F_{in} = 5 \text{ MHz} & \quad 0.2 \text{ LSB rms} \quad (-68 \text{ dBc})
\end{align*}
\]

Dynamic Range of a 10-bit ADC: 60 dB
Power Consumption

ADC Operating Point

<table>
<thead>
<tr>
<th>ONE CHIP</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital leakage current</td>
<td>1.2 mA</td>
</tr>
<tr>
<td>ADC Clock Tree (10 MHz)</td>
<td>23 mA</td>
</tr>
<tr>
<td>Readout Clock Tree (40 MHz)</td>
<td>1.4 mA</td>
</tr>
<tr>
<td>Processing Logic during Trigger (1%)</td>
<td>28 mA</td>
</tr>
<tr>
<td>16 ADCs at 10 MS/s</td>
<td>77 mA</td>
</tr>
</tbody>
</table>

Average Power Per Chip
- 257 mW

Average Power Per Channel
- 16 mW
Testing Strategy

ALTRO CHIP Testing

Functional Validation
- Fulfills all the processing functions required
  - ADC performance is satisfactory
- Realistic input patterns (Montecarlo & Measurements)
  - Consistent with HDL Simulations
    - Performed in one chip

Physical Validation
- Toggle all possible nodes and memory cells
  - Several million of test vectors
- Verify ADC performance
  - Repetitive and automatic for $n$ chips
ALTRO CHIP

Functional Validation: Register Control Panel

Baseline Correction 1

Multi-Event Memory

Errors
- Readout Error
- Trigger Overlap
- Instruction Error
- Parity Error

SEU
- Interface
- Memory Unit
- Double Upset
- Simple Upset

Tail Cancellation Filter

Baseline Correction 2

Zero Suppression

Trigger
- Samples per Event
- Trigger Delay
- Pretrigger
- Trigger Counter

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Functional Validation: Realistic Input Pattern

The test input signal combines the signal measured on the TPC prototype with the amplitude and arrival time distributions generated by ALIROOT.

Zero suppression threshold: 5 ADC counts

Altro output filter disabled

Altro output filter enabled
Functional Validation: Realistic Input Pattern

Simulated baseline perturbation:
- electronics temp. variation (ramp-up)
- gating grid switching (systematic)
- power supply instability
- pick-up noise

Time samples: 0 to 8000
ADC counts: 0 to 500

EVENT 1
EVENT 2
EVENT 3