Irradiation results

K.Røed, D.Röhrich, K. Ullaland
B.Skaali, J.Wikne, E.Olsen
V.Lindenstruth, H.Tilsner S.Martens
Marc Stockmaier
Luciano Musa

University of Bergen, Norway
University of Oslo, Norway
KIP, University of Heidelberg, Germany
Physikalisches Institut, University of Heidelberg
CERN

• SEU
• Test setup
• Cross section measurement
• Error estimate per run
**Single Event Upset (SEU)**

- Charge deposition by ionizing particle can lead to a change in state of a transistor
- Critical charge $Q_{\text{crit}} = 0.0023 \text{ pC/µm}^2 \cdot L^2$
  
  $L = \text{feature size (APEX 20k400: } L=0.18 \text{ µm)}$

- Energy deposition $E_{\text{dep}} = \text{LET} \cdot \rho \cdot s$
  
  $\rho = \text{density (Si: } \rho = 2.33 \text{ g/cm}^3)$
  
  $s = \text{path length } (s^2 = 2L^2 + c^2, c = \text{device depth})$

- Charge deposition $Q_{\text{dep}} = E_{\text{dep}} \cdot q / w_{\text{ehp}}$
  
  $w_{\text{ehp}} = \text{electron-hole pair creation energy (Si: } w_{\text{ehp}} = 3.6 \text{ eV})$

- $Q_{\text{dep}} > Q_{\text{crit}}$: SEU -> minimum LET: $\text{LET}_{\text{threshold}}$

- $\text{LET}_{\text{threshold}}$ (APEX) $\approx 100$ keV/mg/cm$^2$

- $\text{LET}(30 \text{ MeV proton in Si}) = 15$ keV/mg/cm$^2$
Single Event Upset (SEU)

- High-energetic hadrons induce nuclear reactions in the silicon (E > 20 MeV - protons, neutrons, pions, kaons)
- Intermediate energy neutrons (2 MeV < E < 20 MeV) contribute little (10%) to SEUs
- (Almost) no effect due to thermal neutrons
- Heavy recoil ions from reactions ionize the material
- Protons do not deposit enough charge deposited by direct ionization to cause a SEU
- Charge deposition leads to a change in state of a transistor (SEU)
- Soft error – can be corrected (rewriting or reprogramming)

\[ \text{Si}(p,2p)\text{Al} \]
\[ \text{Si}(p,p\alpha)\text{Mg} \]
\[ \text{Si}(n,p)\text{Al} \]
\[ \text{Si}(n,\alpha)\text{Mg} \]
\[ \text{Spallation} \]
Test setup

Oslo Cyclotron

- 29 MeV external proton beam
- beamspot 1 x 1cm
- beam intensities > 10pA
  (flux : $0.6 \times 10^8$ protons/s cm$^2$)
- beam distribution made uniform by defocusing and using a gold foil placed upstream in beampath.
Upset detection in ALTERA FPGAs

Two types of concern
- Upsets in configuration SRAM cells
- Single bitflips in register elements

The APEX20K400E offers no direct readout of configuration SRAM
- Indirectly detection of configuration upset through the VHDL design

Error observed reflects a change in logic due to a configuration upset, and not the configuration upset itself
Upset detection

Possibility of undetectable configuration upsets
- Not 100% usage of SRAM bits --> some upset do not influence logic
- Test results give an estimate of configuration upsets.

First glance – configuration upsets and single bitflips induced in logic look the same
- Distinguishable by looking at them over time
- Configuration upset: Permanent until reprogramming of device
- Single upsets: Limited in time, present until next clock cycle

Task: Design hardware that detects SEU's in both logic and internal RAM blocks of the device

VHDL design
- 32 bit wide and 400 bit long shiftregister implemented in logic elements
  (approx. 90% of the LEs)
- 32 bit wide and 4096 bit deep FIFO implemented in internal RAM blocks
  (approx 60% of the internal RAM bits)
Upset detection

A fixed pattern is shifted through and compared for setups when read out.

Communication through SCSN (Slow Control Serial Network)
- Introduces problem of SEUs in the SCSN

Software on Linux PC to read out and analyse data (C, Matlab)
Example of analyzing data

FIFO in internal RAM

Shiftregister in logic elements

Single upset

Configuration upset
Preliminary results

Observations

Configuration upsets in logic and internal RAM

- Single upsets in internal RAM only
  - Many interconnection in logic elements
  - Low density of SRAM cells compared to internal RAM blocks

- SEU - uncorrelated
- Expecting linear dependency
Cross section results

• General observation
  – No SEU at a proton beam energy of 10 MeV
  – Dependence on orientation of device in respect to beam direction
    » increase of cross section by a factor of 2 at 45° orientation as compared to 0°
Cross section results

- FPGA APEX 20K400

<table>
<thead>
<tr>
<th>Component</th>
<th>Cross section [cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration RAM</td>
<td></td>
</tr>
<tr>
<td>Logic</td>
<td>$1.9 \times 10^{-10} \pm 0.8 \times 10^{-10}$</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>$1.5 \times 10^{-10} \pm 0.8 \times 10^{-10}$</td>
</tr>
<tr>
<td>Single upsets</td>
<td></td>
</tr>
<tr>
<td>Logic</td>
<td>$&lt;5.3 \times 10^{-12}$</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>$4.1 \times 10^{-10} \pm 2.2 \times 10^{-10}$</td>
</tr>
</tbody>
</table>

- FPGA ACEX 1K30

<table>
<thead>
<tr>
<th>Component</th>
<th>Cross section [cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration RAM</td>
<td>$4 \times 10^{-11}$</td>
</tr>
</tbody>
</table>
Cross section results

- External components

<table>
<thead>
<tr>
<th></th>
<th>Cross section [cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>External SRAM</td>
<td>≈ 2 x 10⁻¹⁰</td>
</tr>
<tr>
<td>SDRAM</td>
<td>≈ 3 x 10⁻¹¹</td>
</tr>
</tbody>
</table>

- FLASH errors after 7 x 10¹¹ protons

- FPGA EPX1

<table>
<thead>
<tr>
<th></th>
<th>Cross section [cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM core program</td>
<td>1.5 x 10⁻¹⁰</td>
</tr>
</tbody>
</table>
### Error estimates per run

<table>
<thead>
<tr>
<th>Particle</th>
<th>Fluence $[\text{cm}^{-2}]$ per 10 ALICE years (Simulation 1, non-absorber &amp; absorber side)</th>
<th>Fluence $[\text{cm}^{-2}]$ per 10 ALICE years (Simulation 2, incl. absorber side)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Protons</td>
<td>$6 \times 10^8$</td>
<td>$8.6 \times 10^8$</td>
</tr>
<tr>
<td>Pions, kaons</td>
<td>$3.5 \times 10^9$</td>
<td>$1.4 \times 10^9$</td>
</tr>
<tr>
<td>Neutrons (5%)</td>
<td>$1.9 \times 10^9$</td>
<td>$5 \times 10^9$</td>
</tr>
<tr>
<td></td>
<td>$\approx 10^{10}? \text{ tbc}$</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Particle</th>
<th>Flux $[\text{sec}^{-1}\text{cm}^{-2}]$ (Simulation 1)</th>
<th>Flux $[\text{sec}^{-1}\text{cm}^{-2}]$ (Simulation 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Protons</td>
<td>24</td>
<td>34</td>
</tr>
<tr>
<td>Pions, kaons</td>
<td>140</td>
<td>56</td>
</tr>
<tr>
<td>Neutrons (5%)</td>
<td>76</td>
<td>450? tbc</td>
</tr>
</tbody>
</table>


Error estimates per run

- High-energetic hadron flux:
  \[ 250 \text{ – } 550 \text{ hadrons/sec}^{-1}\text{cm}^{-2} \]

<table>
<thead>
<tr>
<th></th>
<th>Error rate per run (4 hours) per device</th>
<th>Error rate per run (4 hours) per system</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEC</td>
<td>(3 \times 10^{-4})</td>
<td>1.4</td>
</tr>
<tr>
<td>RCU</td>
<td>(1.5 \times 10^{-3})</td>
<td>0.3</td>
</tr>
<tr>
<td>DCS</td>
<td>(3 \times 10^{-3})</td>
<td>0.6</td>
</tr>
</tbody>
</table>
Conclusion

• SRAM based FPGAs
  – SEU rate acceptable?

• Alternative: FLASH based FPGA (Actel)
  – Supposed to be radiation tolerant
  – Provide similar resources
  – Irradiation tests are underway