Readout Control Unit Status

Overview
RCU card and sub-cards
Status of different modules/tasks
Milestones
RCU Main Building Blocks

- Power
- FEB A
- FEB B
- TTCrx
- DCS
- Bus Termination
- Config
- FPGA
- SIU
RCU Main Building Blocks Implementation

- RCU Mother-board
- SIU Mezzanine board
- TTCrx/DCS Mezzanine board

Components:
- Power
- Bus Termination
- Config
- TTC
- DCS
- FPGA
- FEB A
- FEB B

Connections:
- FPGA to SIU
- FPGA to TTC
- FPGA to DCS
- FEB A to FEB B
RCU Main PCB Top View
RCU Main PCB Bottom View
TTCrx/ DCS Mezzanine Board
SIU board
RCU card with FEC
Internal and external connections

- **Internal**
  - Connections from the FECs via backplane to the RCU MB
  - Connections from RCU MB to TTCrx/DCS board via 144 pin connector
    - Includes programming interface from TTCrx/DCS board to RCU MB
  - Connections from RCU MB to SIU card via CMC connectors
  - Possible JTAG to TTCrx/DCS board from neighbour TTCrx/DCS board

- **External**
  - Trigger information on Optical Link
  - Data stream from SIU to DAQ on Optical link
  - Power to RCU MB which is distributed to the DCS and the SIU boards
  - Ethernet to TTCrx/DCS board
Configuration Scheme

RCU FPGA to be configured from DCS daughterboard. Configuration pins are overlaid DCS database. All configuration schemes supported. Transceiver UI to be enabled during configuration only.

DCS_R100 master control line for config enable. LEDs are for post config debug.
Read out Control Unit (revision 1.1 - Oct '03)

- Schematics (pdf)
- Components numbering top (pdf)
- Components numbering bottom (pdf)
- Printing table EP20K20CEFL-BGA672 (generated from Capture Cis) (dls)
- More to come
- PCB GERBER files

Lay01.pdf (top)
Lay02.pdf
Lay03.pdf
Lay04.pdf
Lay05.pdf
Lay06.pdf
Lay07.pdf
Lay08.pdf
Lay09.pdf
Lay10.pdf
Lay11.pdf
Lay12.pdf (bottom)

Picture of the PCB
Status of external Communication

- **RCU <-> DCS**  
  DIM Server Client Scheme over ethernet  
  (Presented by Christian Kofler)

- **RCU <-> Trigger**  
  VME based test setup (VP 110 CPU board running LINUX, TTCvi – Bergen)  
  Developed during summer 2003 at Cern

- **RCU <-> DiU**  
  pRORC or HRORC based Test setup

- **RCU <-> FEC**  
  Front End Card Interface  
  (Presented by Bernardo Mota)
Milestones

- **Milestones:**
  - Design Document: 1st ed Finished
  - Module interface definitions: Finished
  - Module functional definitions: Finished
  - Implementation of the essential modules: June/July 2003
  - Radiation tests: Partially finished
    - Oslo Cyclotron: October/November 2003
    - Uppsala TSL: November 2003
  - Schematic design: Finished August 2003
  - PCB Layout: Finished September 2003
  - Engineering prototype: Finished October 2003
  - Test Firmware: December 2003
  - Hardware/Firmware integration: December 2003
  - Partial System Integration: January 2004
  - Qualification of the final design: October 2003-March 2004
  - Production: Apr. 2004-July 2004
  - RCU ready for installation: October 2004
Open issues

• Migration to Actel