Front-End Card Interface of the RCU

(Bernardo Mota & Carmen Gonzalez Gutierrez)

ALTRO Interface
- Block diagram
- Memories and Functionality
- Macro Instructions
- “Microcontroller” Code
- FEC debugging capabilities

Board Controller Interface
- Block diagram
- Table of Registers
- Present Status
FEC Interface: Block Diagram
ALTRO Interface: Memories and Functionality

Instruction Memory
- DI
- AD
- WE
- INCLK

23 bit

Result Memory
- DI
- AD
- WE
- INCLK

20 bit

Data Memory x 2
- DI
- AD
- WE
- INCLK
- OUTCLK

128

Pattern Memory
- DI
- AD
- WE
- INCLK

40 bit

256

1024
**ALTRO Interface: RCU Macro Instructions**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>JUMP</td>
<td>4'h0 8'hxx Add.</td>
<td>19 16 15 8 7 0</td>
</tr>
<tr>
<td>RS_STATUS</td>
<td>4'h1 16'hxxxx</td>
<td>19 0</td>
</tr>
<tr>
<td>RS_L1CNT</td>
<td>4'h2 16'hxxxx</td>
<td>19 0</td>
</tr>
<tr>
<td>RS_L2CNT</td>
<td>4'h3 16'hxxxx</td>
<td>19 0</td>
</tr>
<tr>
<td>LOOP</td>
<td>4'h4 8'hxx N cycles</td>
<td>19 16 15 8 7 0</td>
</tr>
<tr>
<td>RETURN</td>
<td>4'h5 8'hxx Add.</td>
<td>19 16 15 8 7 0</td>
</tr>
</tbody>
</table>

**RCU Macro Instructions**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHRDO</td>
<td>4'h6 16'hxxxx</td>
<td>19 0</td>
</tr>
<tr>
<td>PMREAD</td>
<td>4'h7 4'hx channel add.</td>
<td>19 16 15 12 11 0</td>
</tr>
<tr>
<td>PMWRITE</td>
<td>4'h8 3'hx bcast chann. add.</td>
<td>19 16 15 13 12 11 0</td>
</tr>
<tr>
<td>END</td>
<td>4'h9 16'hxxxx</td>
<td>19 0</td>
</tr>
<tr>
<td>WAIT</td>
<td>4'ha Nbr. Cycles CLK</td>
<td>19 16 15 0</td>
</tr>
</tbody>
</table>
ALTRO Interface: *Microcontroller “code”*

Testing Multi-Event Buffer & Readout

SWTRG (L1)
WAIT
WPINC (L2)
CHRDO (Readout)
RPINC
*END*

Normal Trigger sequence

Testing Registers and Memories of the ALTROs & Configuration

LOOP
WRITE ‘N’ REG
READ ‘N’ REG
PMWRITE
PMREAD
CONFIG
JUMP

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ALTRO Interface: Debugging Capabilities
BC Interface: *Block Diagram*

[Diagram of the BC Interface with labels for each component and connections.]

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## BC Interface: Table of Registers

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>T_TH</td>
<td>Temperature Thr.</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Maximum Temperature Threshold</td>
</tr>
<tr>
<td>02</td>
<td>AV_TH</td>
<td>AV threshold</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Minimum Analog Voltage Threshold</td>
</tr>
<tr>
<td>03</td>
<td>AC_TH</td>
<td>AC threshold</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Maximum Analog Current Threshold</td>
</tr>
<tr>
<td>04</td>
<td>DV_TH</td>
<td>DV threshold</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Minimum Digital Voltage Threshold</td>
</tr>
<tr>
<td>05</td>
<td>DC_TH</td>
<td>DC threshold</td>
<td>10</td>
<td>R/W</td>
<td>Y</td>
<td>Maximum Digital Current Threshold</td>
</tr>
<tr>
<td>08</td>
<td>TEMP</td>
<td>Temperature</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Temperature Value</td>
</tr>
<tr>
<td>09</td>
<td>AV</td>
<td>Analog Voltage</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Analog Voltage Value</td>
</tr>
<tr>
<td>0A</td>
<td>AC</td>
<td>Analog Current</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Analog Current Value</td>
</tr>
<tr>
<td>0B</td>
<td>DV</td>
<td>Digital Voltage</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Digital Voltage Value</td>
</tr>
<tr>
<td>0C</td>
<td>DC</td>
<td>Digital Current</td>
<td>10</td>
<td>R</td>
<td>N/A</td>
<td>Digital Current Value</td>
</tr>
<tr>
<td>10</td>
<td>L1CNT</td>
<td>L1 Counter</td>
<td>16</td>
<td>R</td>
<td>N/A</td>
<td>Number of L1 Trigger Received</td>
</tr>
<tr>
<td>11</td>
<td>L2CNT</td>
<td>L2 Counter</td>
<td>16</td>
<td>R</td>
<td>N/A</td>
<td>Number of L2 Trigger Received</td>
</tr>
<tr>
<td>12</td>
<td>SCLKCNT</td>
<td>Sampling clk counter</td>
<td>16</td>
<td>R</td>
<td>N/A</td>
<td>Sampling Clock counter</td>
</tr>
<tr>
<td>13</td>
<td>DSTBCNT</td>
<td>Data Strobe Counter</td>
<td>8</td>
<td>R</td>
<td>N/A</td>
<td>Number of Data Strobe in the last ReadOut</td>
</tr>
</tbody>
</table>

### Meanings:

- **Thresholds**
- **Measurables**
- **Counters**
### BC Interface: Table of Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Access</th>
<th>R/W</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>CSR0 Configuration Status 0</td>
<td>14</td>
<td>R/W</td>
<td>Interrupt - Mask Register</td>
</tr>
<tr>
<td>15</td>
<td>CSR1 Configuration Status 1</td>
<td>15</td>
<td>R</td>
<td>Error Status Register</td>
</tr>
<tr>
<td>16</td>
<td>CSR2 Configuration Status 2</td>
<td>16</td>
<td>R/W</td>
<td>Card Configuration Status Register</td>
</tr>
<tr>
<td>18</td>
<td>CNTLAT Counters Latch</td>
<td>18</td>
<td>- W</td>
<td>Y</td>
</tr>
<tr>
<td>19</td>
<td>CNTCLR Counters Clear</td>
<td>19</td>
<td>- W</td>
<td>Y</td>
</tr>
<tr>
<td>1A</td>
<td>CSR1CLR Conf. St. Reg 1 Clear</td>
<td>1A</td>
<td>- W</td>
<td>Y</td>
</tr>
<tr>
<td>1B</td>
<td>ALRST ALTRO Reset</td>
<td>1B</td>
<td>- W</td>
<td>Y</td>
</tr>
<tr>
<td>1C</td>
<td>BCRST BC Reset</td>
<td>1C</td>
<td>- W</td>
<td>Y</td>
</tr>
<tr>
<td>1D</td>
<td>STCNV Start Conversion mADC</td>
<td>1D</td>
<td>- W</td>
<td>Y</td>
</tr>
</tbody>
</table>

**08/10/03**  
ALICE TPC Meeting  
Bernardo Mota (CERN EP/ED)
Each TPC Sector is served by 6 Readout Subsystems

The control network shares the same back-plane as the ALTRO bus, using the same GTL transceivers.

The Electrical implementation of the I²C bus consists of 3 unidirectional lines instead of 2 bi-directional links.

Overall TPC: 4356 Front End Card    216 Readout Control Unit
THE FRONT-END CARD (FEC)

BC Interface: Physical Layout

- 5-channel 10bit ADC
- FPGA hosting Board Controller logic and register set
- Current monitoring & supervision
- ALTROs
- Shaping Amplifiers (PASAs)
- Voltage regulators
- Power connector
- Control bus connector
- Readout bus connectors
- GTL transceivers (back side)

Dimensions:
- Width: 155 mm
- Height: 190 mm
BC Interface: I2C Protocol
BC Interface: \textit{I2C Protocol}

- Transmission rate up to 3.4Mbit/sec in High Speed mode
- Worldwide standard protocol developed by Philips
- Maximum allowed bus capacitance of 400pF
- FECs can be connected or disconnected without disturbing the network functioning
- Bi-directional 8-bit serial data transfer
- Multi-master protocol with Arbitration
Present Status

ALTRO Interface

- √ IP design completed and simulated
- X Testing in PLDA board: End of October
- √ Additional macro instructions and active channel list to be included

Board Controller Interface

- √ BC ↔ ADC: Design completed, simulated and tested
- X RCU ↔ BC (I2C + ALTRO bus): integration and test missing