TPC FRONT END ELECTRONICS
Approaching the production

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TPC FEE - ARCHITECTURE (1/2)

FEE ARCHITECTURE

DETECTOR

- Anode wire
- Pad plane (570132 pads)
- Drift region (88 μs, 200 Hz)
- Gating grid

FEC (Front End Card) - 128 CHANNELS
(CLOSE TO THE READOUT PLANE)

- 8 chips x 16 CH/CHIP
- CUSTOM IC (CMOS 0.35 μm)
- CUSTOM IC (CMOS 0.25 μm)
- CPA
- ADC
- Digital Circuit
- RAM
- ALTRO
- Multi-event Memory
- Base and tail canceller
- Zero suppression
- Gain: 12 mV/fC
- FWHM: 190 ns
- Dynamic: 30 MIP
- Digital Delay Line (4096 CH/DL)

Power consumption: 40 mW/channel

Power consumption: 40 mW/channel

1 MIP = 4.8 fC
S/N = 30:1
Dynamic = 30 MIP

L1: 5 μs, 200 Hz

L2: < 100 μs, 200 Hz

DDL (4096 CH / DDL)
GLOBAL ARCHITECTURE

Each TPC Sector is served by 6 Readout Subsystems

Overall TPC: 4356 Front End Card 216 Readout Control Unit
**PRE-AMPLIFIER SHAPING AMPLIFIER (PASA) MAIN FEATURES**

- Noise < $10^3$ e
- MIP = $3 \times 10^4$ e
- $Q/C_f$
- $C_f/R_f$
- $(RC)^4$
- < 1 mV
- 30 mV

16-ch Amplifier / Shaper (PASA)

- CMOS 0.35 µm (AMS)
- Area: 16.7 mm$^2$
- Power: 12 mW / ch
- Gain: 12 mV / fC
- Noise: 400 e
- Crosstalk: < 0.4%

CHIP LAYOUT
THE PASA CONTEST

Nr. CH: 16
POWER/CH: 47mW
NOISE (12pF): 722 e

Nr. CH: 9
POWER/CH: 7.25mW
NOISE (12pF): 670 e

Nr. CH: 16
POWER/CH: 12mW
NOISE (12pF): 400 e

1996
STAR TPC

2000
ALICE TPC prototype

2001
ALICE TPC final
PERFORMANCE OF PASA EMBEDDED IN FEC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
<th>Measured (preliminary)</th>
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</thead>
<tbody>
<tr>
<td>Noise</td>
<td>1000 e</td>
<td>(700 + 13/pF) e</td>
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<tr>
<td>Conversion gain</td>
<td>12mV / fC</td>
<td>11.8 mV / fC</td>
</tr>
<tr>
<td>Shaping time</td>
<td>190ns</td>
<td>190ns</td>
</tr>
<tr>
<td>Non linearity</td>
<td>&lt;1%</td>
<td>&lt; 0.35%</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>&lt;0.3%</td>
<td>&lt;0.4%</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 20mW / ch</td>
<td>12mW / ch</td>
</tr>
<tr>
<td>Area</td>
<td></td>
<td>16.7mm²</td>
</tr>
</tbody>
</table>

**MILESTONES**

- January ‘02: delivery of 40 samples of final PASA
- Feb - Apr ‘02: test of PASA in stand-alone mode
- May ‘02: integration of PASA in the FEC
- June ‘02: test of PASA connected to the IROC
- July ‘02: delivery of additional 200 samples
- July ‘02: engineering run
- October ‘02: full production
FEE ARCHITECTURE

DETECTOR
- Drift region: 88 μs, 200 Hz
- Gating grid
- Anode wire
- Pad plane
- 570132 pads

FEC (Front End Card) - 128 CHANNELS (CLOSE TO THE READOUT PLANE)
- 8 chips x 16 CH / chip
- Custom IC (CMOS 0.35 μm)
- Custom IC (CMOS 0.25 μm)

ADC
Digital Circuit
RAM

PASA

1 MIP = 4.8 fC
S/N = 30 : 1
DYNAMIC = 30 MIP

CSA
- Semi-Gauss. Shaper
- Gain = 12 mV / fC
- FWHM = 190 ns

10 bit
< 10 MHz
- Baseline corr.
- Tail cancel.
- Zero suppress.

Multi-event memory

Power consumption:
40 mW / channel

L1: 5 μs, 200 Hz

L2: < 100 μs, 200 Hz

DDL (4096 CH / DDL)

- Base 10 logarithmic scaling
- Semi-Gauss. Shaper
- Gain = 12 mV / fC
- FWHM = 190 ns
- 10-bit ADC
- 10 MHz sampling rate
- Multi-event memory
- Baseline correction
- Tail cancellation
- Zero suppression

Power consumption:
40 mW / channel
16 channels in 2002
TPC FEE – ALTRO: SUMMARY OF THE PROTOTYPING ACTIVITIES

1998
- CHANNELS / CHIP: 1
- POWER / CH: 120mW
- PRICE / CH: 50CHF

1999
- CHANNELS / CHIP: 4
- POWER / CH: 80mW
- PRICE / CH: 8CHF

2001
- CHANNELS / CHIP: 1
- POWER / CH: 16mW
- PRICE / CH: 5CHF

Integrated ADCs

24 mm

20 mm

4 PQFP 100
8 SSOP 28

4 cards
16 ch

135 mm

26 mm
**TPC FEE – ALTRO: MAIN FEATURES (1/2)**

- **Baseline Correction I**
  - 10-bit 20 MSPS
- **Baseline Correction II**
  - 18-bit CA2 arithmetic
- **Tail Cancellation**
  - 11-bit CA2 arithmetic
- **Zero Suppression**
  - 11-bit arithmetic
  - 10-bit arithmetic
- **Data Format**
  - 40-bit format
- **Memory + Multi-Event Buffer**
  - 40-bit format

**16-ch signal digitizer and processor**

- **HCMOS7 0.25 µm (ST)**
- **area**: 64 mm²
- **power**: 16 mW / ch
- **prototype delivery**: Feb ‘02
- **300 samples fully tested**
- **delivery of 4x10⁴ chips**: Dec ‘02

**MAX SAMPLING CLOCK 40 MHz**
**MAX READOUT CLOCK 60 MHz**
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TPC FEE – ALTRO TEST (1/8)

ALTRO TEST SETUP

CONTROL PC RUNNING LABVIEW BASED TEST SOFTWARE

ARPITARY WAVEFORM GENERATOR

PULSE GENERATOR

SINE WAVE GENERATORS

LP FILTERS

TEST BOARD

CLOCK GENERATORS

POWER SUPPLIES

MULTIMETER

TIMER / COUNTER
ALTRO TEST BOARD

- Analogue input signal
- Power regulation
- 16 x differential linear drivers
- Clock & trigger signals
- Logic analyzer interface
- PC interface
- Altro chip under test
- Test controller (FPGA)

TPC FEE – ALTRO TEST (2/8)
16 CHANNELS IN ONE SHOT
EFFECTIVE NUMBER OF BITS (ENOB)

1MHz SINE WAVE

400 measurements with 1000 samples / measurement

THE ADC SHOWS ONLY THE QUANTIZATION ERROR
ENOB vs Frequency

Effective Number of Bits vs Input Frequency

Quartz Jitter:
25ps r.m.s.

Amplitude Uncertainty:

\[ 4 \cdot f_{in} \cdot \text{jitter} \cdot 2^{10} \]

0.5 bits at 4.8 MHz
Crosstalk and Digital Noise

Readout Clock below -78 dBc (WC)

Bus interference below -65 dBc (WC)

Channel-to-Channel Crosstalk

\[ F_{\text{in}} = 1 \text{ MHz} \quad 0.05 \text{ LSB rms} \quad (-80 \text{ dBc}) \]

\[ F_{\text{in}} = 5 \text{ MHz} \quad 0.2 \quad \text{LSB rms} \quad (-68 \text{ dBc}) \]

Dynamic Range of a 10-bit ADC: 60 dB
Differential and Integral Non-Linearity

- **Differential Non-Linearity**: ±0.2 LSB
- **Integral Non-Linearity**: ±0.5 LSB

![Differential and Integral Non-Linearity Graphs](image)
Chip performance

ENOB vs Analog Vcc

ENOB vs Duty Cycle

ENOB vs Sampling Frequency

Digital Power Consumption vs Sampling Frequency
FUNCTIONAL VALIDATION: ALTRO CONTROL PANNEL

[Diagram showing various control panels and settings]

- **Baseline Correction 1**
  - Node: RT-f3d
  - Power Save: Enable
  - Polarity: Norm

- **Multi-Event Memory**
  - Event Buffer: 4
  - Empty/Full: Empty
  - Write Pointer: 0
  - Read Pointer: 0
  - Available Buffers: 4
  - Last Event Length: 0

- **Tail Cancellation Filter**
  - Enable
  - K1: 0.93560
  - L1: 0.93237
  - K2: 0.80395
  - L2: 0.76653
  - K3: 0.75737
  - L3: 0.76547

- **Baseline Correction 2**
  - Enable
  - LO Threshold: 7
  - HI Threshold: 7
  - Presamples: 1
  - Postsamples: 1

- **Zero Suppression**
  - Enable
  - Offset
  - Presamples: 0
  - Postsamples: 0

- **Trigger**
  - Samples per Event: 0
  - Trigger Delay: 0
  - Pretrigger: 0
  - Trigger Counter: 136

- **Errors**
  - Readout Error
  - Trigger Overlap
  - Instruction Error
  - Parity Error

- **SEU**
  - Interface
    - Double Upset
    - Simple Upset
  - Memory Unit
    - Double Upset
    - Simple Upset

- **Unwritten Changes**
- **Verification Error**
- **Tax/fix Error**
The test input signal combines the signal measured on the TPC prototype with the amplitude and arrival time distributions generated by ALIROOT.
FRONT END CARD

TOP SIDE

BOTTOM SIDE
INTEGRATION IN THE READOUT CHAMBER
Pre-series production of 30 FEC (60% of one IROC) started.

Market survey for mass production will be concluded by end of June.
GLOBAL ARCHITECTURE

Each TPC Sector is served by 6 Readout Subsystems

Overall TPC: 4356 Front End Card
216 Readout Control Unit

Detector Link (100 MB/s) (#216)

Front-end bus (200 MB/sec)

Data Compr.

Local Controller

BOARD CTRL

TTC-RX

Local Slow-Control Serial link

Detector Link (100 MB/s) (#216)
READOUT CONTROL UNIT
FIRST PROTOTYPE

PCI CARD (PLDa)

FPGA with PCI-core

DDL-SIU CONNECTOR

LEMO CONNECTOR
( L1, L2, RDOCLK, ADCCLK)

PMC CARD

GTL Transceivers

PMC connectors
TPC FEE – READOUT CHAIN

FRONT END CARD + READOUT CONTROL UNIT
READOUT CONTROL UNIT
SECOND PROTOTYPE
**MOUNTING**

**SIDE VIEW**
128 channels
Front End Card (FEC)

**FRONT VIEW**
36 trapezoidal sectors

- C6 : 20 FECs
- C5 : 20 FECs
- C4 : 20 FECs
- C3 : 18 FECs
- C2 : 25 FECs
- C1 : 18 FECs

**FEE POWER:**
- CHANNEL: 40 mW
- BOARD: 6.9 W
- SECTOR: 832 W
- TOTAL: 30.2 KW
SUMMARY

- The TPC FEE consists of 4 basic components:
  - PASA (40,000 chips)
  - ALTRO (40,000 chips)
  - FEC (4500 boards)
  - RCU (220 boards)

- Production:
  - ALTRO: Apr ’02
  - PASA: Nov ’02
  - FEC: Jan ’03

- A significant fraction of the complete electronics (5,000 channels) connected to the IROC will be tested during Summer ‘02