TPC FRONT END ELECTRONICS

Progress Report

CERN – 1 July 2002

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**BASIC READOUT CHAIN**

**DETECTOR**
- L1: 5 μs
- 200 Hz
- 88 μs
drift region
- anode wire
- pad plane
- 570132 PADS
- gating grid

**FEC (Front End Card) - 128 CHANNELS**
- CLOSE TO THE READOUT PLANE
- 8 CHIPS x 16 CH/CHIP

**ADC**
- Digital Circuit

**CUSTOM IC (CMOS 0.35 μm)**
- CUSTOM IC (CMOS 0.25 μm)

**PASA**
- CSA SEMI-GAUSS. SHAPER
- GAIN = 12 mV/fC
- FWHM = 190 ns
- 10 BIT
- < 10 MHz
- BASELINE CORR.
- TAIL CANCEL.
- ZERO SUPPR.

**MULTI-EVENT MEMORY**

**Power consumption**: 40 mW/channel

**L2**: < 100 μs
- 200 Hz

**DDL**: (4096 CH / DDL)

**Power consumption**: 40 mW/channel

**TPC FEE - ARCHITECTURE (1/2)**

**1 MIP = 4.8 fC**
**S/N = 30 : 1**
**DYNAMIC = 30 MIP**
GLOBAL ARCHITECTURE

Each TPC Sector is served by 6 Readout Subsystems

Overall TPC: 4356 Front End Card 216 Readout Control Unit

Detector Link (100 MB / s) (#216)

Slow – Control (1 Mbit – serial link)
AMPLIFIER / SHAPER – MAIN CHARACTERISTICS (1/2)

PRE-AMPLIFIER SHAPING AMPLIFIER (PASA) MAIN FEATURES

Noise < 10^3 e
MIP = 3x10^4 e

Noise < 1000e (@ 12pF)
< 1% INL
< 0.3% Crosstalk
< 20 mW / ch Power

MAIN REQUIREMENTS

Gain: 12mV / fC (@ 12pF)
FWHM: 190ns
Noise: < 1000e (@ 12pF)
INL: < 1%
Crosstalk: < 0.3%
Power: < 20 mW / ch

CHIP LAYOUT (AMS 0.35 μm)
THE PASA CONTEST

1.2μm  9.36 mm²
Single-signal
2nd order shaper

0.35μm  5 mm²
Single-signal
2nd order shaper

0.35μm
16.7 mm²
differential-signal
4th order shaper

Nr. CH: 16
POWER/CH: 47mW
NOISE (12pF): 722 e

Nr. CH: 9
POWER/CH: 7.25mW
NOISE (12pF): 670 e

Nr. CH: 16
POWER/CH: 12mW
NOISE (12pF): 566 e

1996
STAR TPC

2000
ALICE TPC
prototype

2001
ALICE TPC
final

Single-signal
2nd order shaper
PULSE SHAPE

REQUIREMENTS:  FWHM = 190ns,  GAIN = 12mV/fC

FWHM = 190ns

GAIN = 10.4mV/fC

C_in = 12pF

177.9 fC

19.2 fC
EQUIVALENT NOISE CHARGE

REQUIREMENT: ENC < 1000 e (@12pF)

ENC = (283 + 23.6 * C_{in}) e

ENC = 566 e (@12pF)
LINEARITY

Non linearity < 0.35%

REQUIREMENT: INL < ± 1%
BASELINE DISPERSION

- Baseline Dispersion < 60mV
- Positive Output
- Negative Output
- Differential Output
**PERFORMANCE OF PASA EMBEDDED IN FEC**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
<th>Measured (preliminary)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise</td>
<td>1000 e</td>
<td>(600 + 23/pF) e</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>12 mV / fC</td>
<td>10.8 mV / fC (*)</td>
</tr>
<tr>
<td>Shaping time</td>
<td>190 ns</td>
<td>190 ns</td>
</tr>
<tr>
<td>Non linearity</td>
<td>&lt; 1%</td>
<td>&lt; 0.35%</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>&lt; 0.3%</td>
<td>&lt; 0.4%</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 20 mW / ch</td>
<td>12 mW / ch</td>
</tr>
<tr>
<td>Area</td>
<td></td>
<td>16.7 mm²</td>
</tr>
</tbody>
</table>

(*) to be corrected in the ER

**MILESTONES**

- January '02: delivery of 40 samples of final PASA
- Feb - Apr '02: test of PASA in stand-alone mode
- May '02: integration of PASA in the FEC
- July '02: test of PASA connected to the IROC
- July '02: delivery of additional 200 samples
- July '02: engineering run (*)
- October '02: full production
16 channels in 1999
16 channels in 2002
ALTRO - SUMMARY OF THE PROTOTYPING ACTIVITIES

<table>
<thead>
<tr>
<th>Year</th>
<th>Channels / Chip</th>
<th>Power / CH</th>
<th>Price / CH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1998</td>
<td>1</td>
<td>120mW</td>
<td>50CHF</td>
</tr>
<tr>
<td>1999</td>
<td>4</td>
<td>80mW</td>
<td>8CHF</td>
</tr>
<tr>
<td>2001</td>
<td>1</td>
<td>16mW</td>
<td>5CHF</td>
</tr>
</tbody>
</table>

Integrated ADCs

- 1998: 4 cards, 16 channels, 135 mm
- 1999: 4 PQFP 100, 8 SSOP 28, 24 mm
- 2001: ALTRO16

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ALTRO - MAIN FEATURES

**16-ch signal digitizer and processor**

- HCMOS7 0.25 \(\mu\)m (ST)
- area: 64 mm\(^2\)
- power: 16 mW / ch
- prototype delivery: Feb ‘02
- 300 samples fully tested
- delivery of 4x10\(^4\) chips: Dec ‘02
ALTRO TEST SETUP
ALTRO TEST BOARD

- ANALOGUE INPUT SIGNAL
- POWER REGULATION
- CLOCK & TRIGGER SIGNALS
- PC INTERFACE
- ALTRO CHIP UNDER TEST
- TEST CONTROLLER (FPGA)
- LOGIC ANALYZER INTERFACE
- 16 X DIFFERENTIAL LINEAR DRIVERS

ALTRO – PERFORMANCE (1/12)
16 CHANNELS IN ONE SHOT
1MHz SINE WAVE

400 measurements with 1000 samples / measurement

THE ADC SHOWS ONLY THE QUANTIZATION ERROR

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB vs Frequency

Effective Number of Bits vs Input Frequency

Quartz Jitter:
25ps r.m.s.

Amplitude Uncertainty:

\[ 4 \cdot f_{in} \cdot \text{jitter} \cdot 2^{10} \]

0.5 bits at 4.8 MHz
Crosstalk and Digital Noise

Digital Noise

Readout Clock below -78 dBc (WC)

Bus interference below -65 dBc (WC)

Channel-to-Channel Crosstalk

\[ F_{in} = 1 \text{ MHz} \quad 0.05 \text{ LSB rms} \quad (-80 \text{ dBc}) \]

\[ F_{in} = 5 \text{ MHz} \quad 0.2 \text{ LSB rms} \quad (-68 \text{ dBc}) \]

Dynamic Range of a 10-bit ADC: 60 dB
Differential and Integral Non-Linearity
**POWER CONSUMPTION**

### Effective Number of Bits
- 9.7 bits

### Power Consumption per Channel
- 12 mW

### ONE CHIP
- Digital leakage current: 1.2 mA
- ADC Clock Tree (10 MHz): 23 mA
- Readout Clock Tree (40 MHz): 1.4 mA
- Processing Logic during Trigger (1%): 28 mA
- 16 ADCs at 10 MS/s: 77 mA

### Average Power Per Chip
- 257 mW

### Average Power Per Channel
- 16 mW
FUNCTIONAL VALIDATION - ALTRO CONTROL PANNEL
THE TEST INPUT SIGNAL COMBINES THE SIGNAL MEASURED ON THE TPC PROTOTYPE WITH THE AMPLITUDE AND ARRIVAL TIME DISTRIBUTIONS GENERATED BY ALIROOT.
Yield of the ALTRO16 (107 samples)

- Passed: 84%
- Failed: 11%
- Kept as spares: 5%

Recoverable chips correspond to single and double bit stuck in the Memories.
The specific location of single bit stuck can be known, and the error can be corrected while de-formatting the data packet.
Failure Analysis (17 samples)

- 41%: Single bit stuck in DM
- 24%: Single bit stuck in PM
- 12%: Multiple bit stuck
- 12%: Datapath/Multiplexers
- 6%: Non Responding

SPARES
FRONT END CARD

FIRST PROTOTYPE

NEW DESIGN

Dimensions:
- 300 mm (height)
- 240 mm (width)
- 190 mm (height)
- 155 mm (width)
FRONT END CARD LAYOUT

TOP SIDE

BOTTOM SIDE
FRONT END CARD COOLING

COOLING PLATES (COPPER)

COOLING PIPE (COPPER)
FEC READOUT BUS
INTEGRATION IN THE READOUT CHAMBER

FRONT VIEW

Outer chamber

FEC

Inner chamber
TPC FEE - INTEGRATION

SIDE VIEW

128 channels
Front End Card (FEC)

CAPTON CABLE

140mm

CAPTON CABLE

190mm

FRONT VIEW

36 trapezoidal sectors

C6 : 20 FECs
C5 : 20 FECs
C4 : 20 FECs
C3 : 18 FECs
C2 : 25 FECs
C1 : 18 FECs

OUTER CHAMBER

INNER CHAMBER

FEE POWER:

◆ CHANNEL: 40 mW
◆ BOARD: 6.9 W
◆ SECTOR: 832 W
◆ TOTAL: 30.2 KW
FRONT END CARD MILESTONES

- Pre-series production of 30 FEC (60% of one IROC) started
- Market survey for mass production concluded in June ‘02
- Radiation test of FEC Sept 02
- Start of mass production Jan 03
- End of production test Jan 04
Each TPC Sector is served by 6 Readout Subsystems

Overall TPC: 4356 Front End Card

216 Readout Control Unit
READOUT CONTROL UNIT
FIRST PROTOTYPE

PCI CARD (PLDa)

FPGA with PCI-core

DDL-SIU CONNECTOR

LEMO CONNECTOR
( L1, L2, RDOCLK, ADCCLK)

PMC CARD

GTL Transceivers

PMC connectors
FRONT END CARD + READOUT CONTROL UNIT
READOUT CONTROL UNIT
SECOND PROTOTYPE

CONTROL LOGIC
DDL – SIU PMC
RCU PMC
SRAM (4 Mbits)
The TPC FEE consists of 4 basic components:

- PASA (40,000 chips)
- ALTRO (40,000 chips)
- FEC (4,500 boards)
- RCU (220 boards)

Production:

- ALTRO: Apr ‘02
- PASA: Nov ‘02
- FEC: Jan ‘03

A significant fraction of the complete electronics (5,000 channels) connected to the IROC will be tested during Summer ‘02
CONVERSION GAIN

WITHIN PROCESS VARIATION

0.3% / pF

0.8% / pF
FRONT-END SIGNAL PROCESSING

ALIROOT CLUSTERS + BASELINE PERTURBATIONS

Simulated baseline perturbation:
- electronics temp. variation (ramp-up)
- gating grid switching (systematic)
- power supply instability
- pick-up noise

ADC data

ADC counts

time samples

EVENT 1

EVENT 2

EVENT 3

ALTRO CHIP – CIRCUIT MAIN FEATURES
FRONT-END SIGNAL PROCESSING

INPUT SIGNAL
EV 1
EV 2
EV 3

AFTER 1st BASELINE CORRECTION
EV 1
EV 2
EV 3

AFTER TAIL CANCELLATION
EV 1
EV 2
EV 3

AFTER 2nd BASELINE CORRECTION
EV 1
EV 2
EV 3
FRONT-END SIGNAL PROCESSING

INPUT SIGNAL

AFTER 1st BASELINE CORRECTION

AFTER TAIL CANCELLATION

AFTER 2nd BASELINE CORRECTION