TPC FEE Status and Planning

CERN, 22 November 2004

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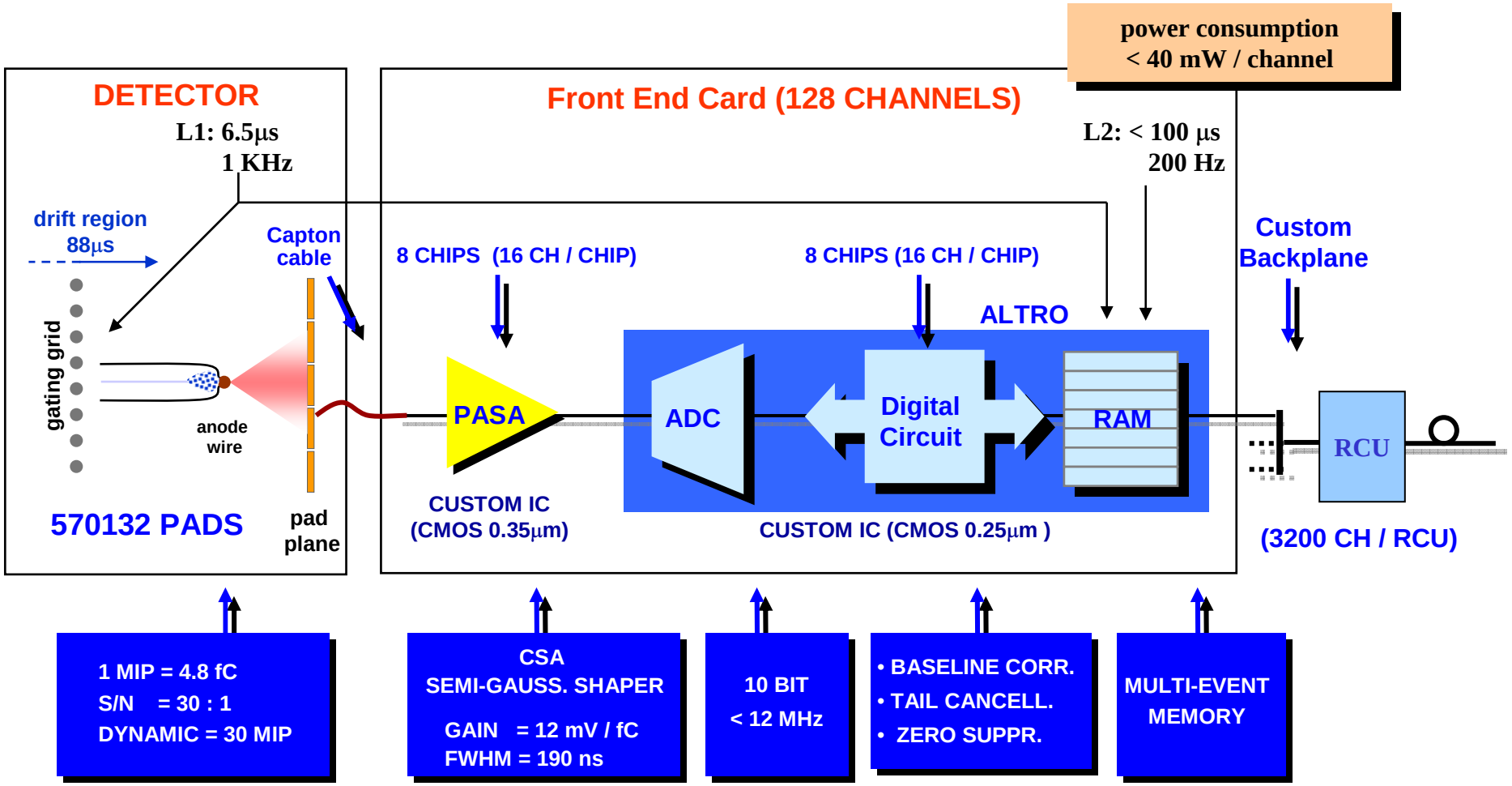
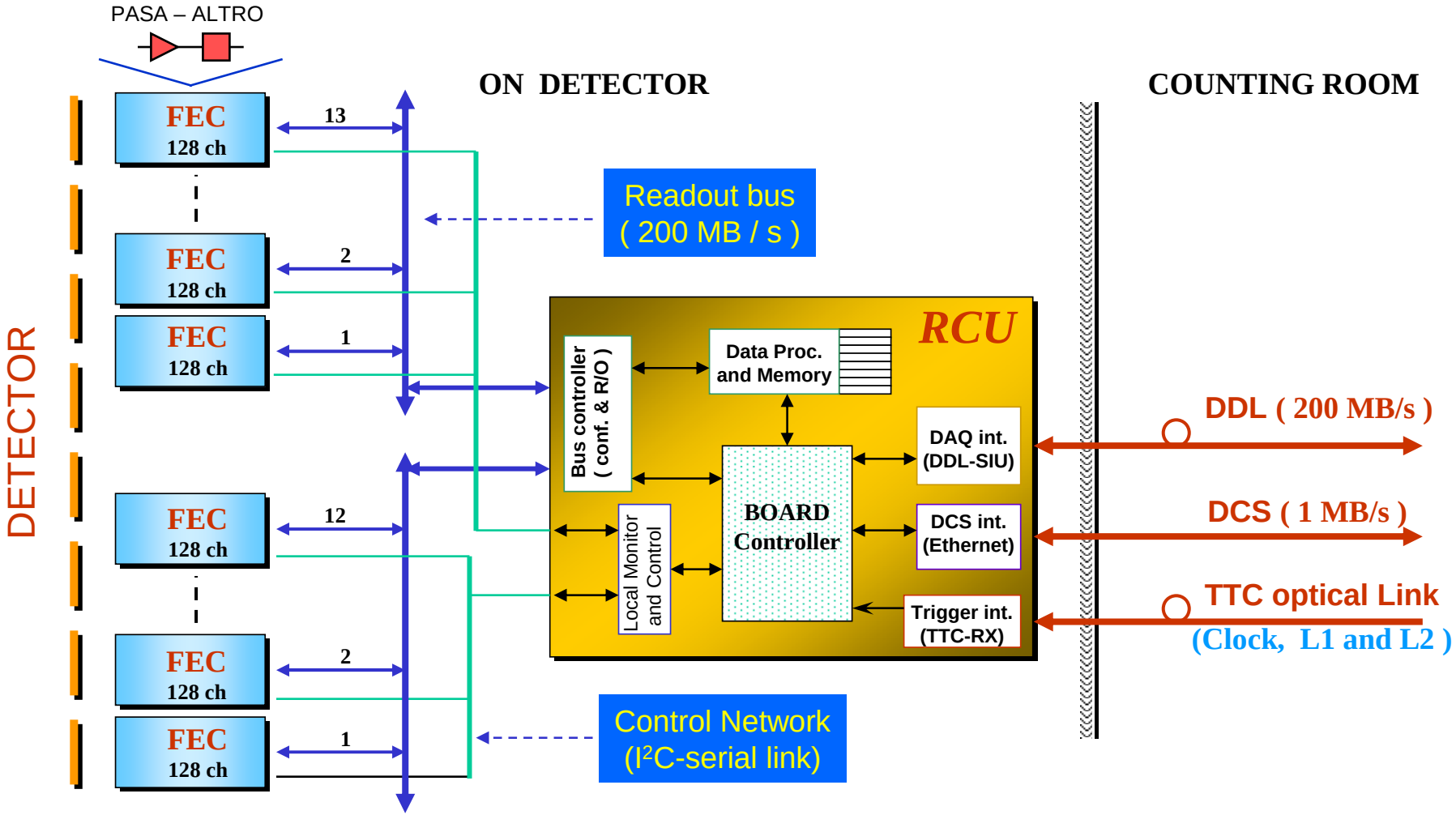
System Overview 1/2



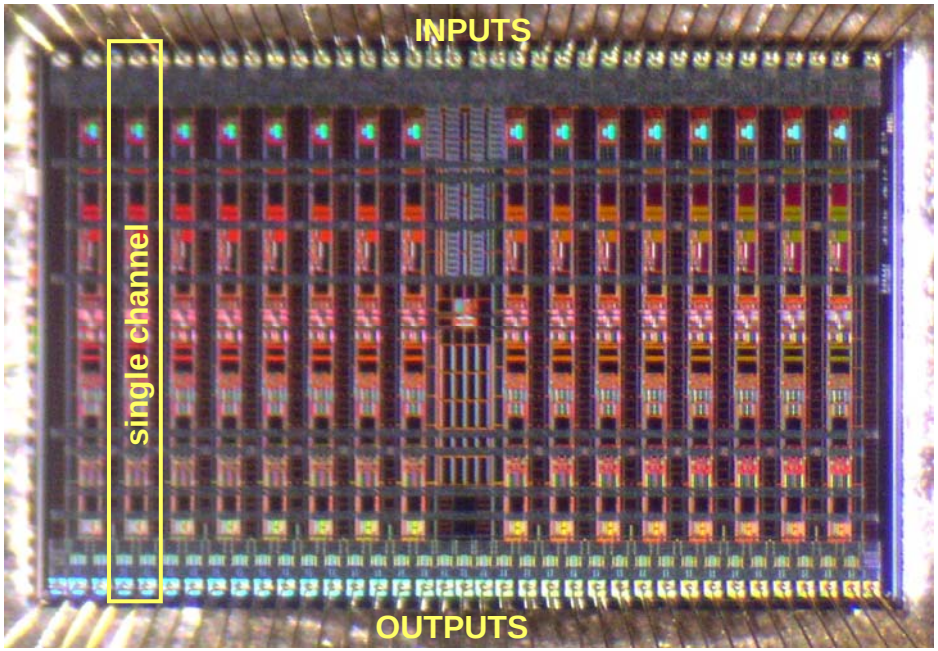
System Overview 2/2

Each of the 36 TPC Sectors is served by 6 Readout Partitions



Overall TPC: 4356 Front End Card 216 Readout Partitions

PASA Production and Test Summary

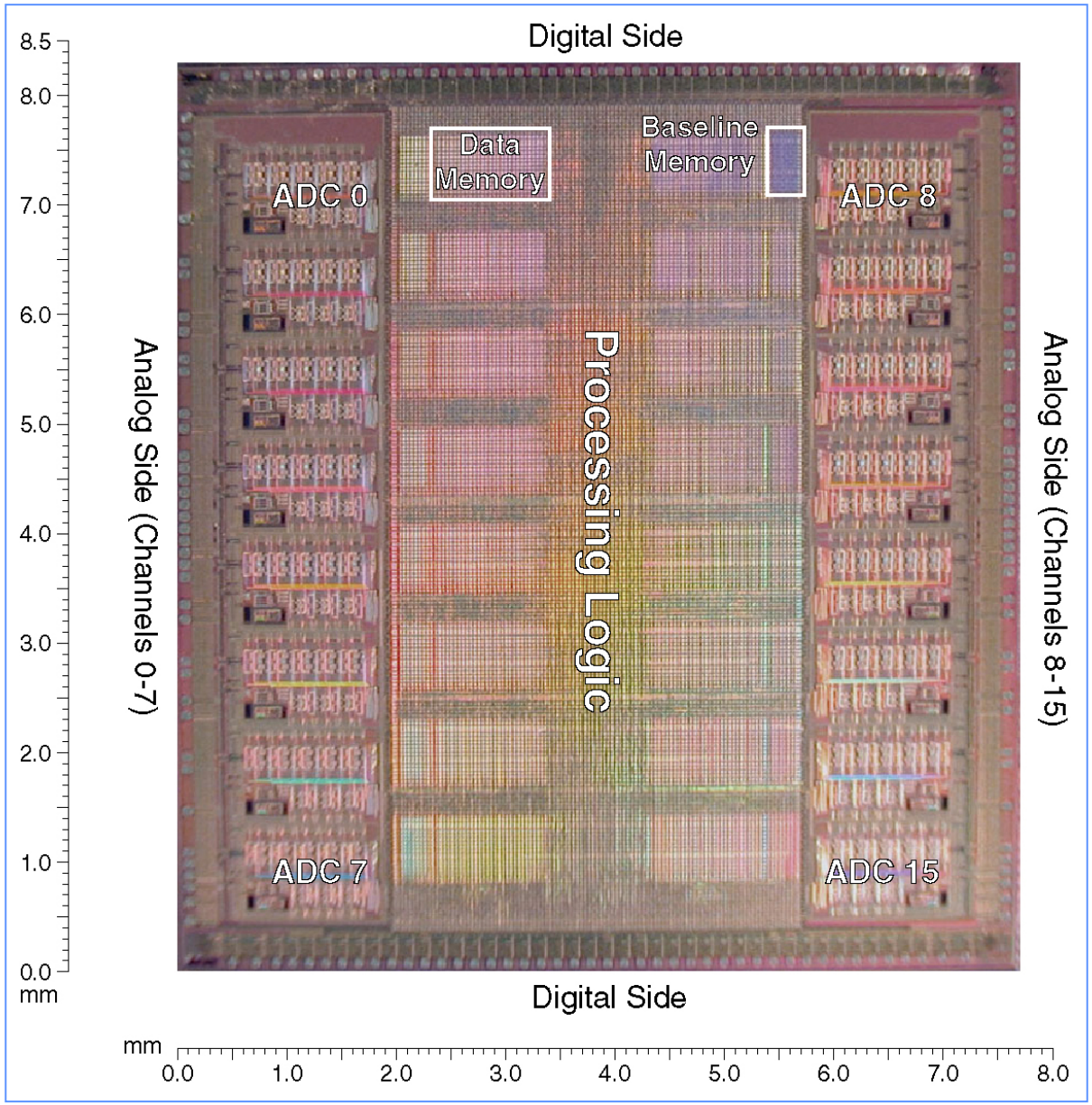


Production Engineering Data

- process: AMS CMOS 0.35 µm
- area: 18 mm^2
- MPR samples: Jan '02
- ER samples (500 chips): Sep '03
- full delivery (49359 chips): Jan '04
- Completion of mass test: May '04
- yield (working chips): 94%
- yield = 83% : |CG| < 5%, |PT|<5%, |BSL| < 5%

Parameter	Requirement	MPR Version	Production
Noise	**< 1000e**	566e (@12pF)	**560e (12pF)**
Conversion gain	**12mV / fC**	10.8mV / fC	**12mV / fC**
Shaping time	**190ns**	190ns	**188ns**
Non linearity	**< 1%**	< 0.35%	**0.2%**
Crosstalk	**<0.3%**	0.4%	**< 0.1%**
Gain dispersion		~1%	**2% (r.m.s.)**
Power consumption	**< 20mW**	12mW / ch	**11mW / ch**

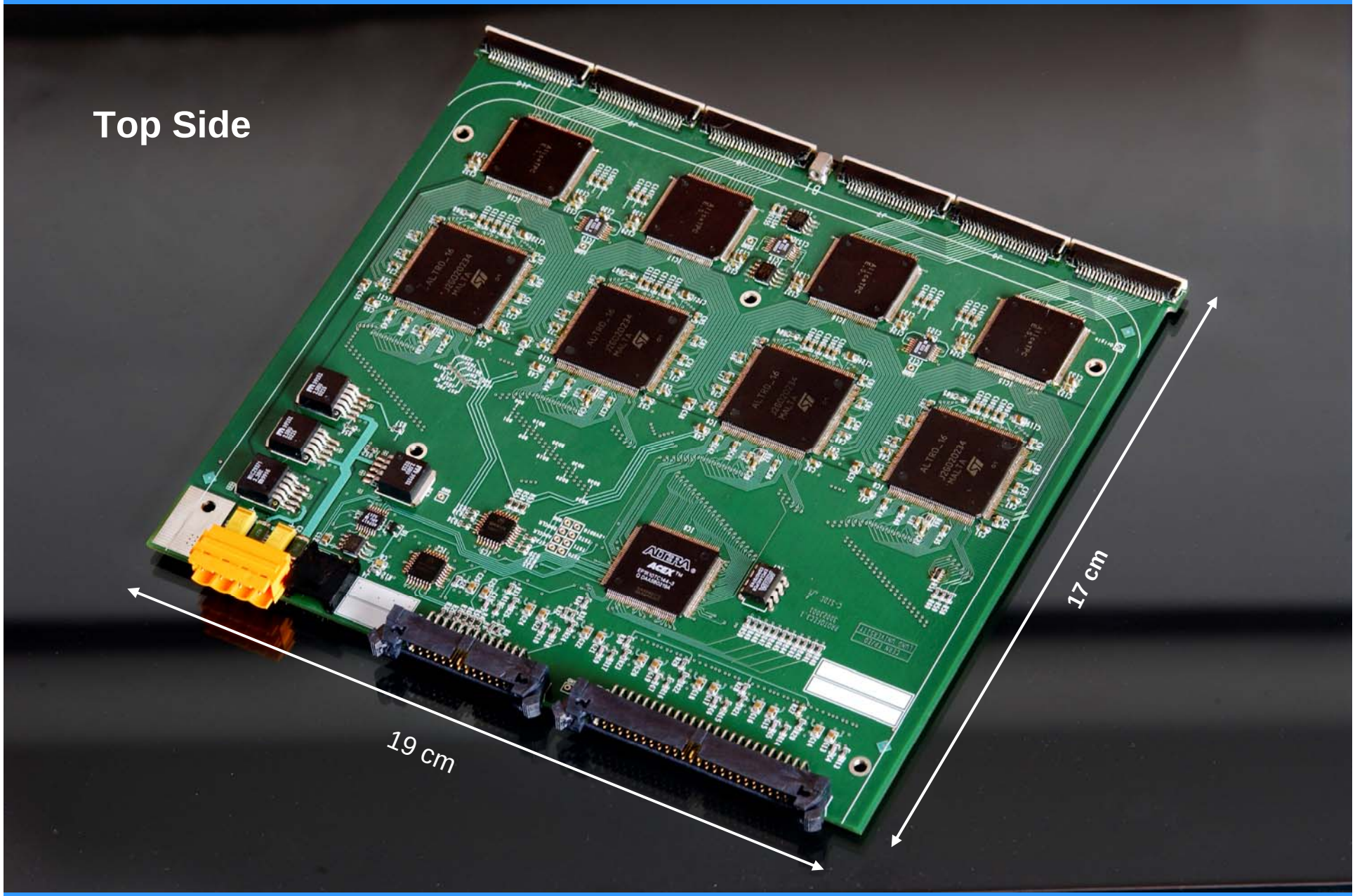
ALTRO Production and Test Summary



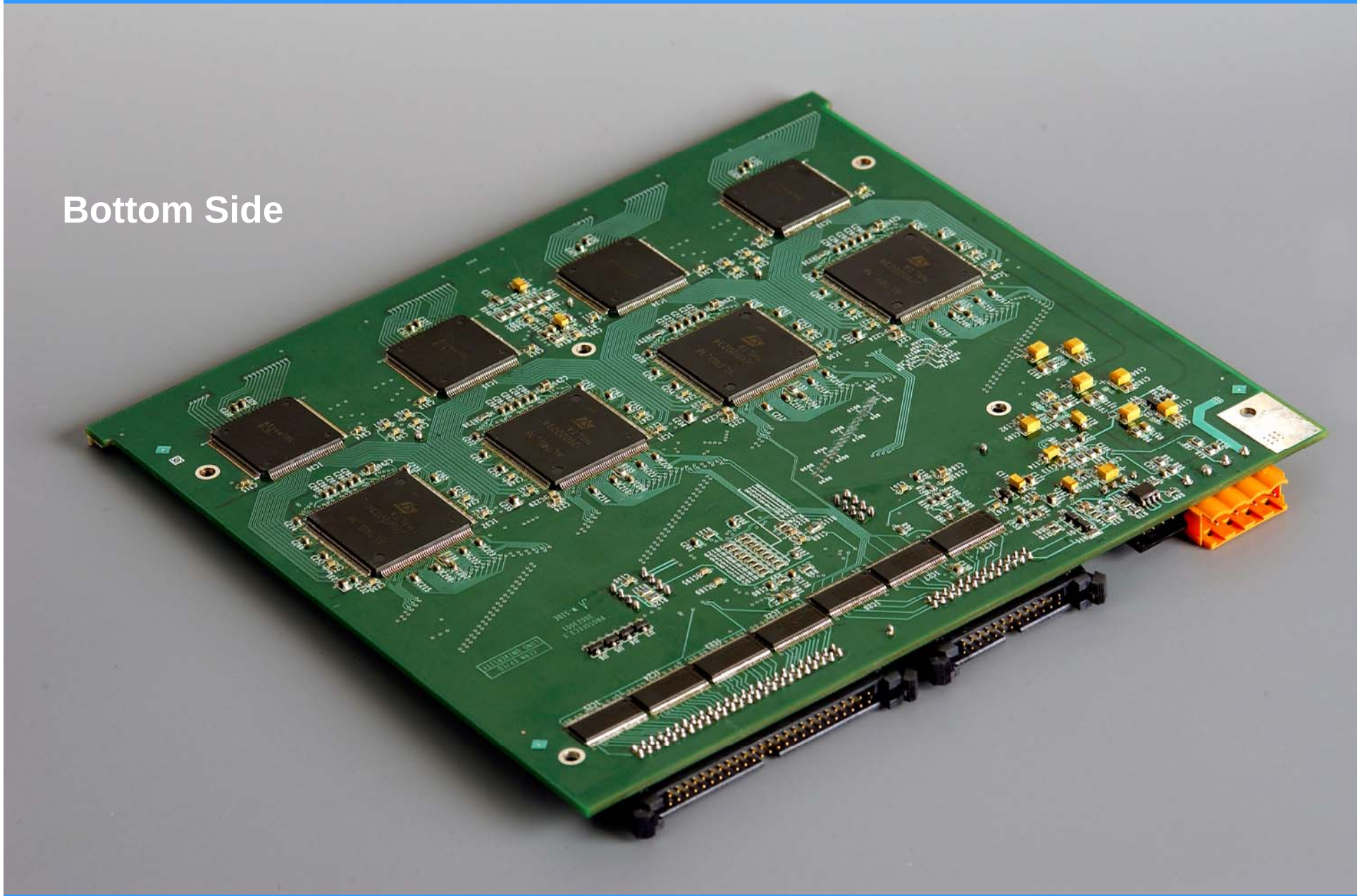
Process	HCMOS-7 (0.25 µm)
Area	64 mm^2
Transistors	6 milions
Embedded memory	800 kbit
ENOB	9.7
Power	16mW / channel

ER (4K chips)	Apr ’02
Mass prod. (44K chips)	Dec ’02
Mass test	Feb ‘04
Yield	84%

Front End Card 1/7



Front End Card 2/7



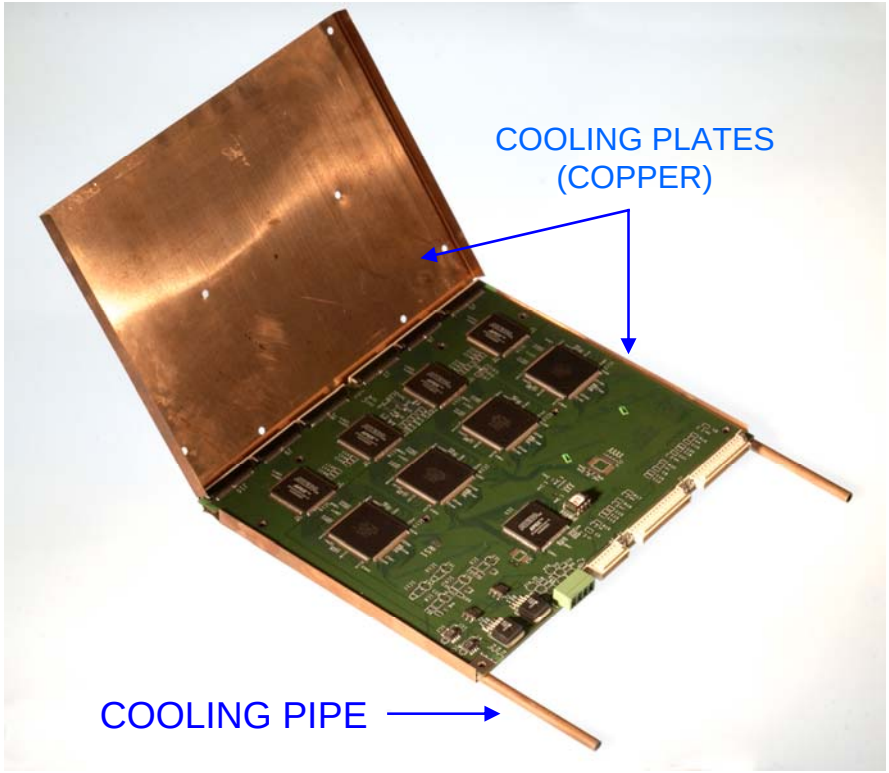
Front End Card 3/7

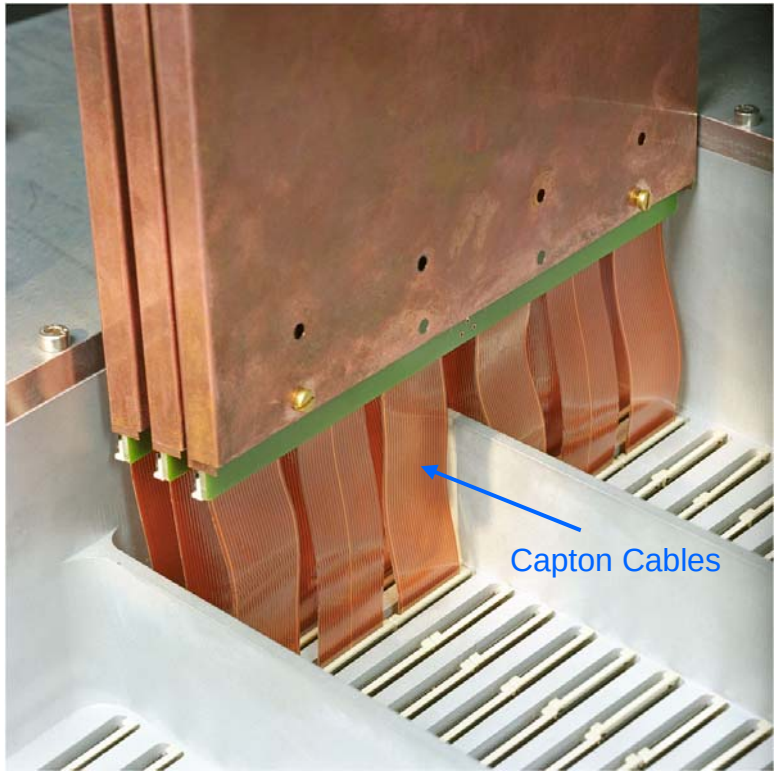
Production

- Production of 4800 FEC
  - Contract signed in Dec ’03 (Note-Xperi @ Lund)
  - Pre-series of 50 boards with good quality (Feb ’04)
  - Pre-series of 200 boards (May ’04)
  - Full production (according to flexible schedule) started in Aug ‘04
    - Production rate 300 boards/ week
    - Nr. of boards produced ~1000
    - Delivery temporary halted for logistic problems (removal) at the Institute (Frankfurt) in charge of the mass test
    - Delivery will be resumed 1st December ’04
    - Production quality is surveyed at CERN by testing 5x lots of 50 boards (5% of the full production)
    - Yield > 90%

Milestone #398, FEECards End Production Jan ‘05

Front End Card 4/7



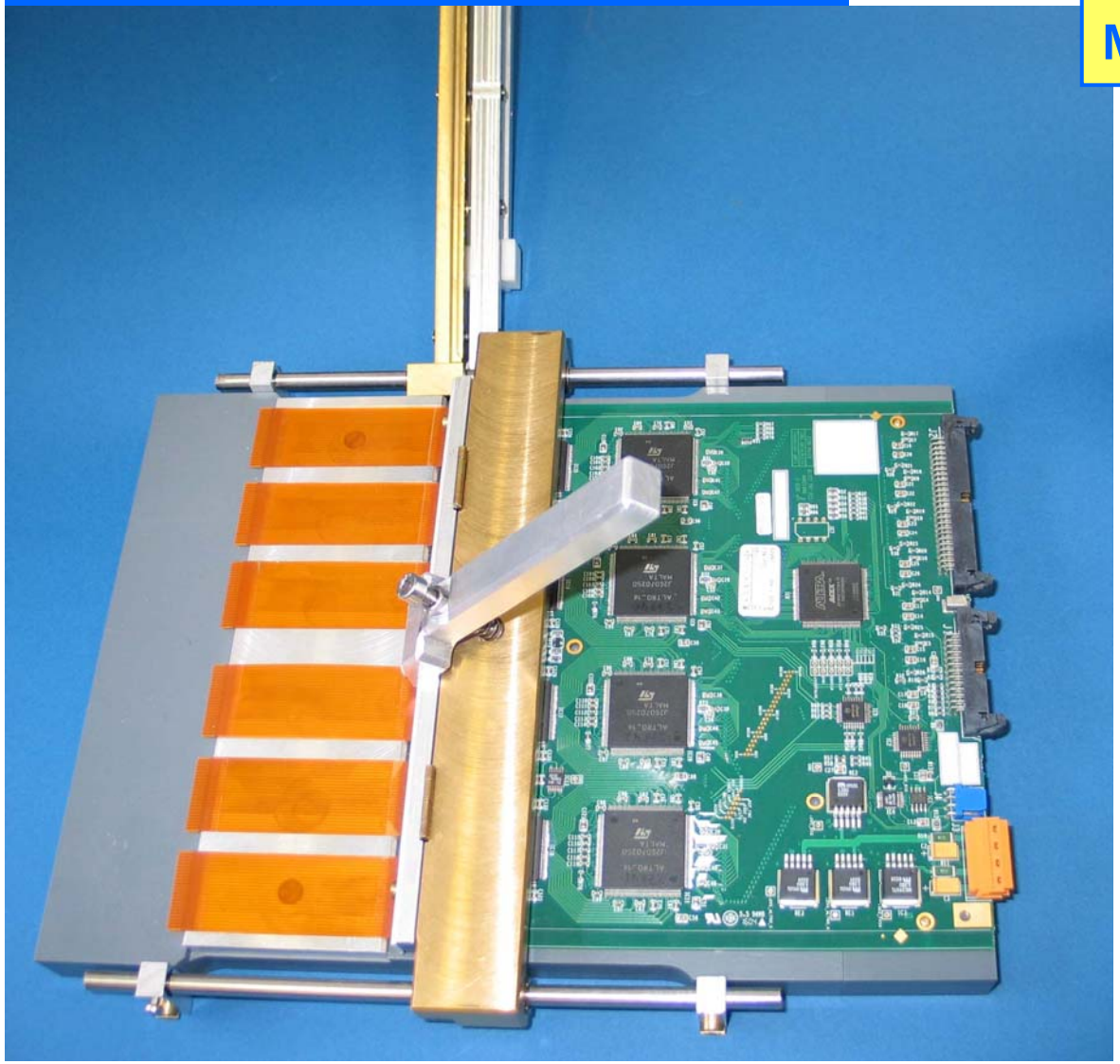


Milestone #230, FEE cables

- **Production of 4500 copper plates in progress**
- **Delivery: 1st lot Dec 04, 2nd lot Feb 05**
- **Production of 30K capton cables in progress**
- **Full delivery end Nov 04**

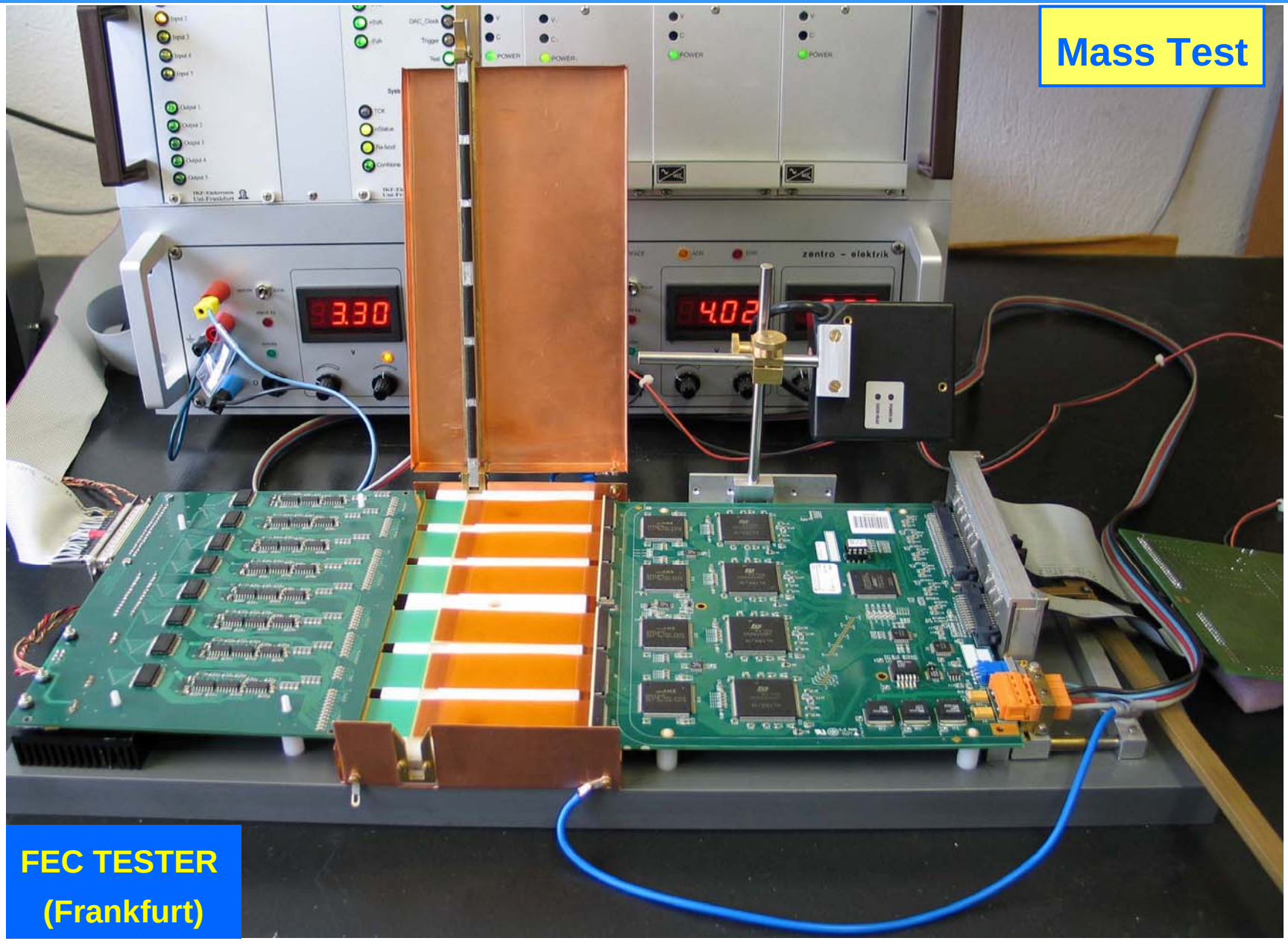
Front End Card 5/7

Tool for the insertion of the capton cables



Mass Test

Front End Card 6/7



Front End Card 7/7

Mass Test

Test site

- **go/no go test: Frankfurt**

Test Procedure (go / no go test)

- Verification of the supply voltages and currents
- Combination of the PASA and ALTRO tests
- Test of FPGA, Readout and Control Network interfaces
- All information stored in the ALICE Construction Database

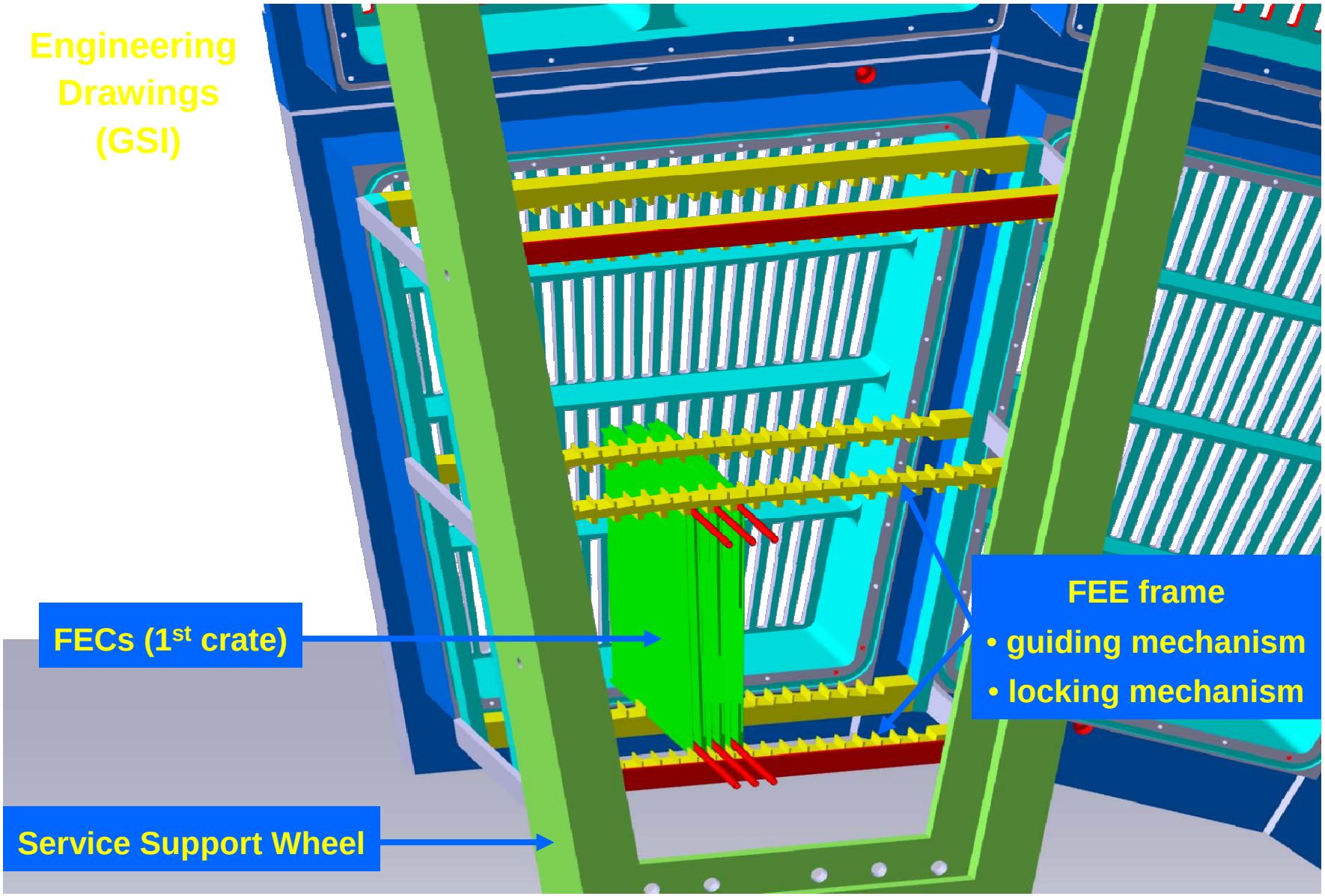
Status

- Hardware: test bench and test procedures (semi-automatic) fully operational
- Software:
  - Control and Acquisition: ready
  - Analysis: ready
  - Access to the database: expected to be completed by Nov ’04
- Projected test rate: 80 boards / dd → 1800 boards / mm

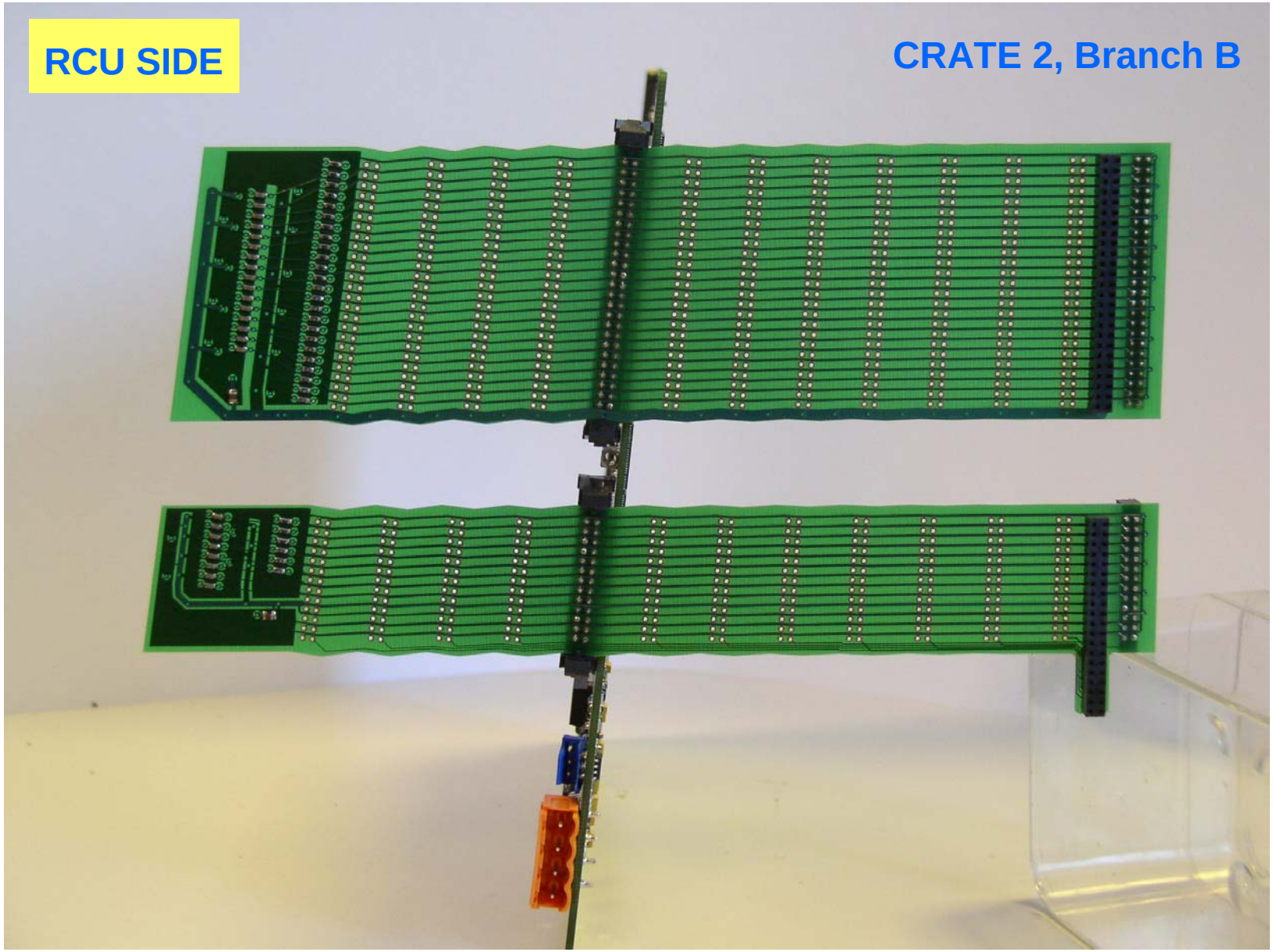
Milestone #239, FEECards Test, Jan - Apr ’05

Front End Card Mounting 1/2

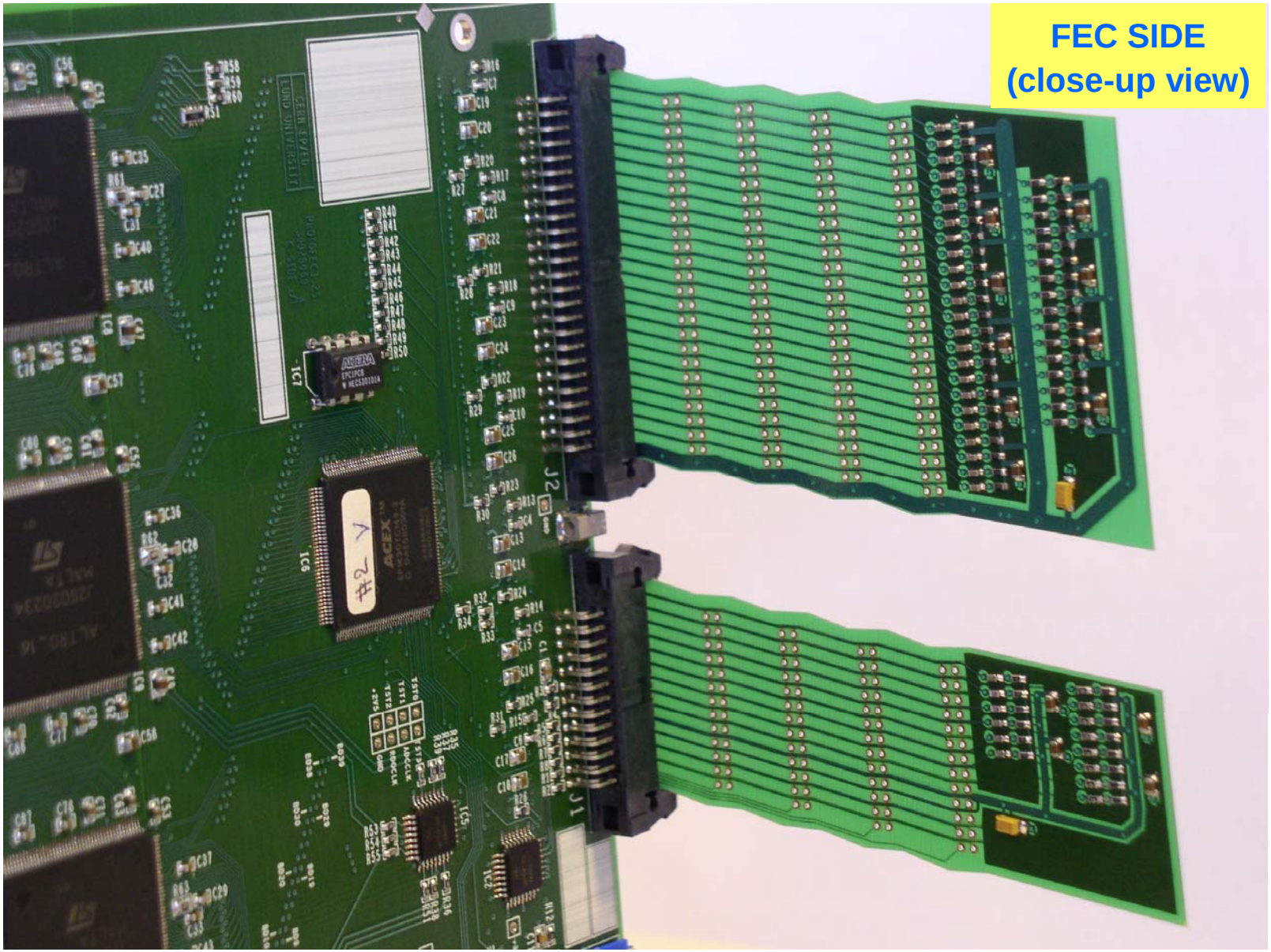
Engineering Drawings (GSI)



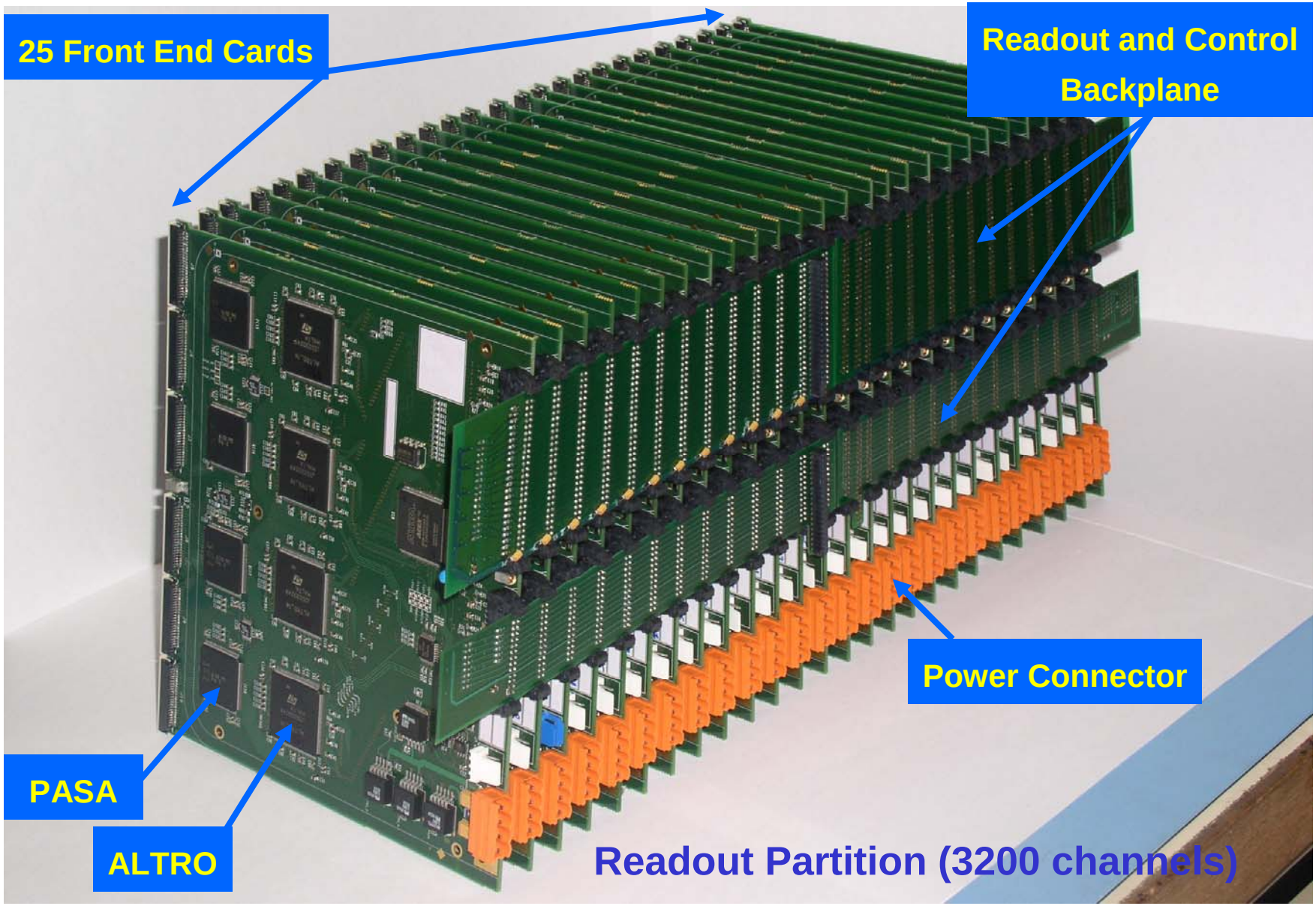
Readout & Control Backplane 1/4



Readout & Control Backplane 2/4



Readout & Control Backplane 3/4



Front End Card Mounting 2/2

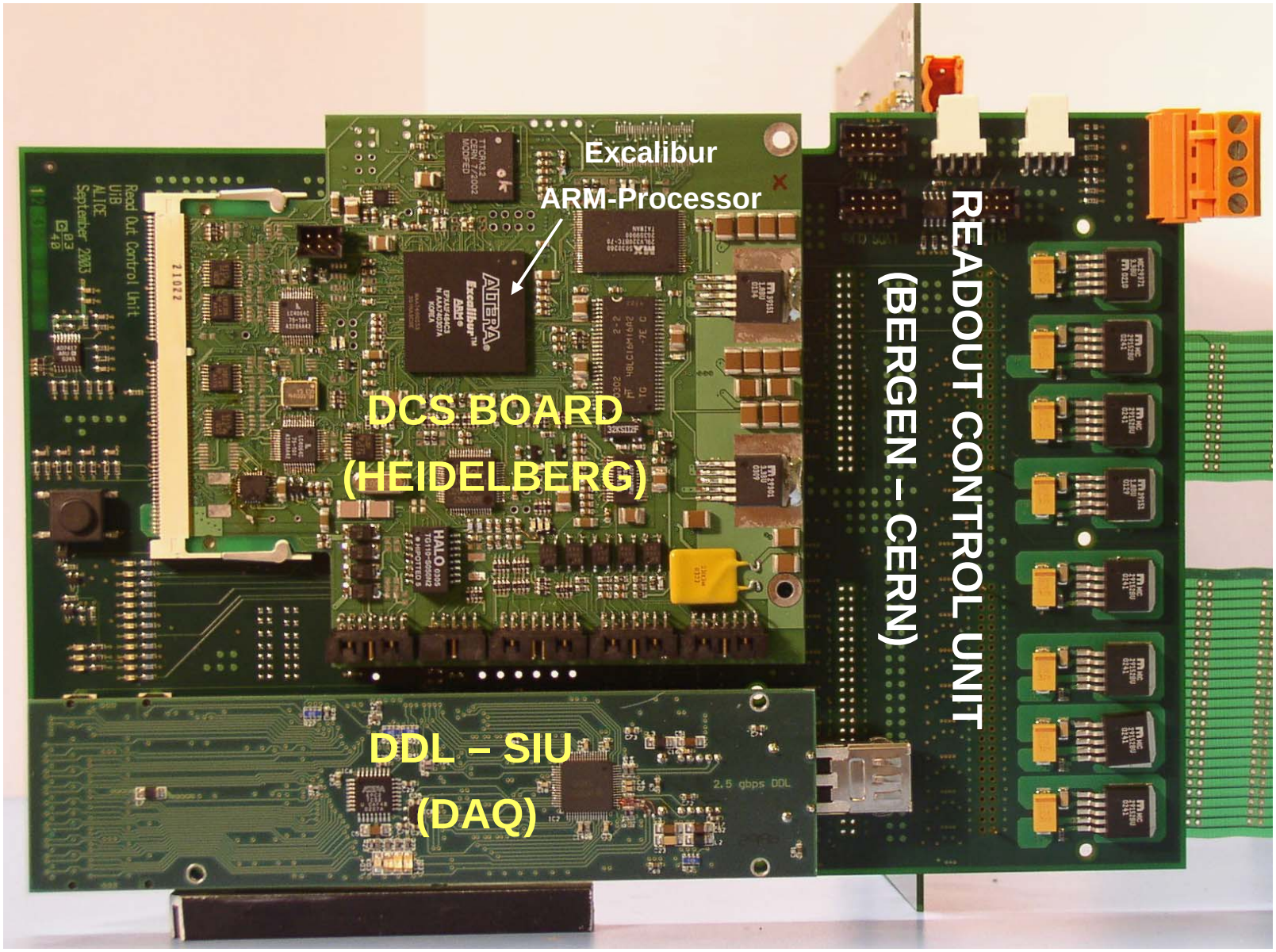
Readout & Control Backplane 4/4

Production

- All backplanes (24 PCBs) are ready for production (864 pcs)
  - Mechanical test OK
  - Electrical Test OK
  - Integration Test: in SSW OK, with new RCU to be done
  - Production database submitted to several Manufacturers
- Test Bench for mass test ready
- Test Software in progress
- Production will start after integration test with final RCU (Jan ’05)

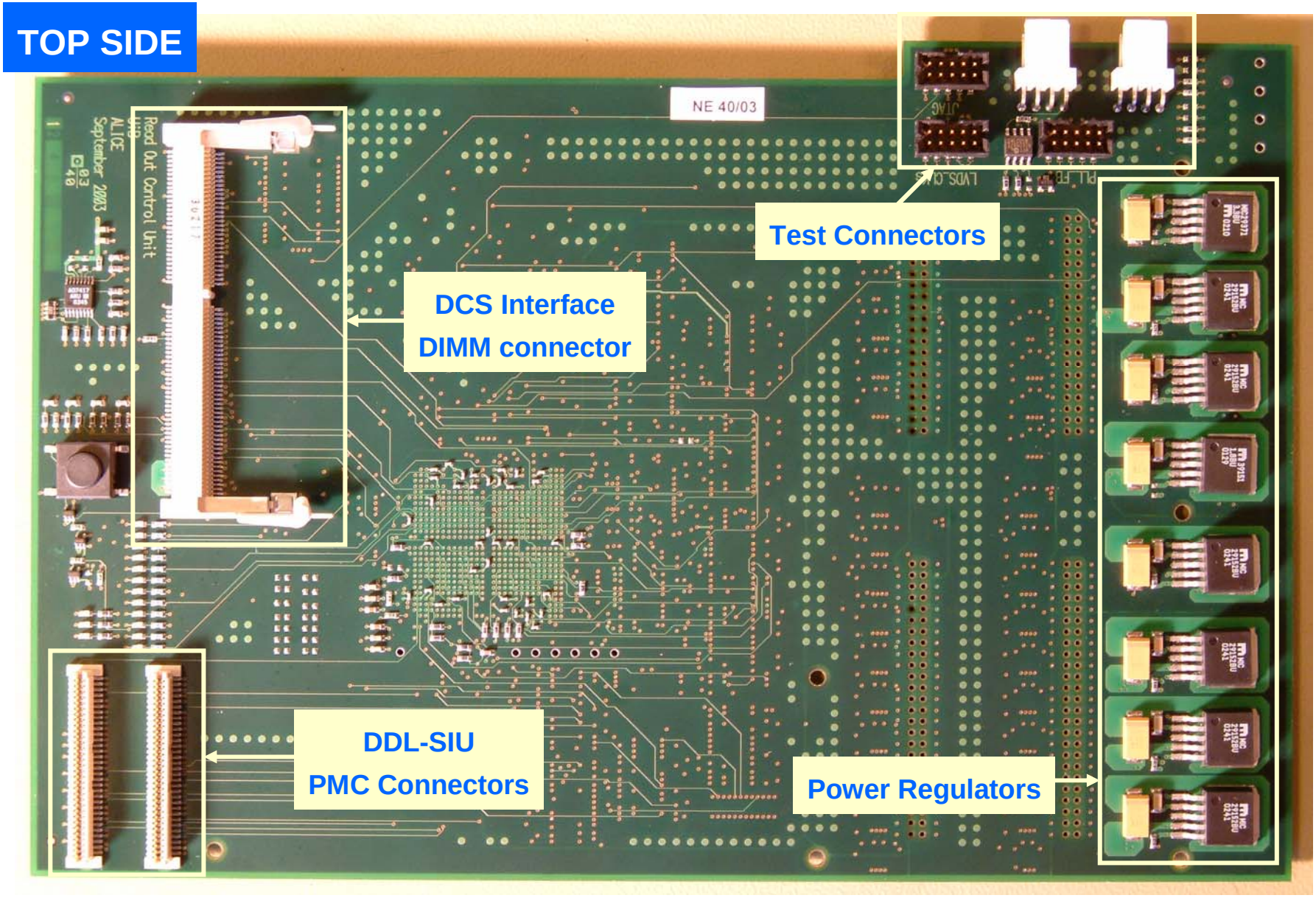
Milestone #394, FEE bus End Production Apr ‘05

Readout Control Unit

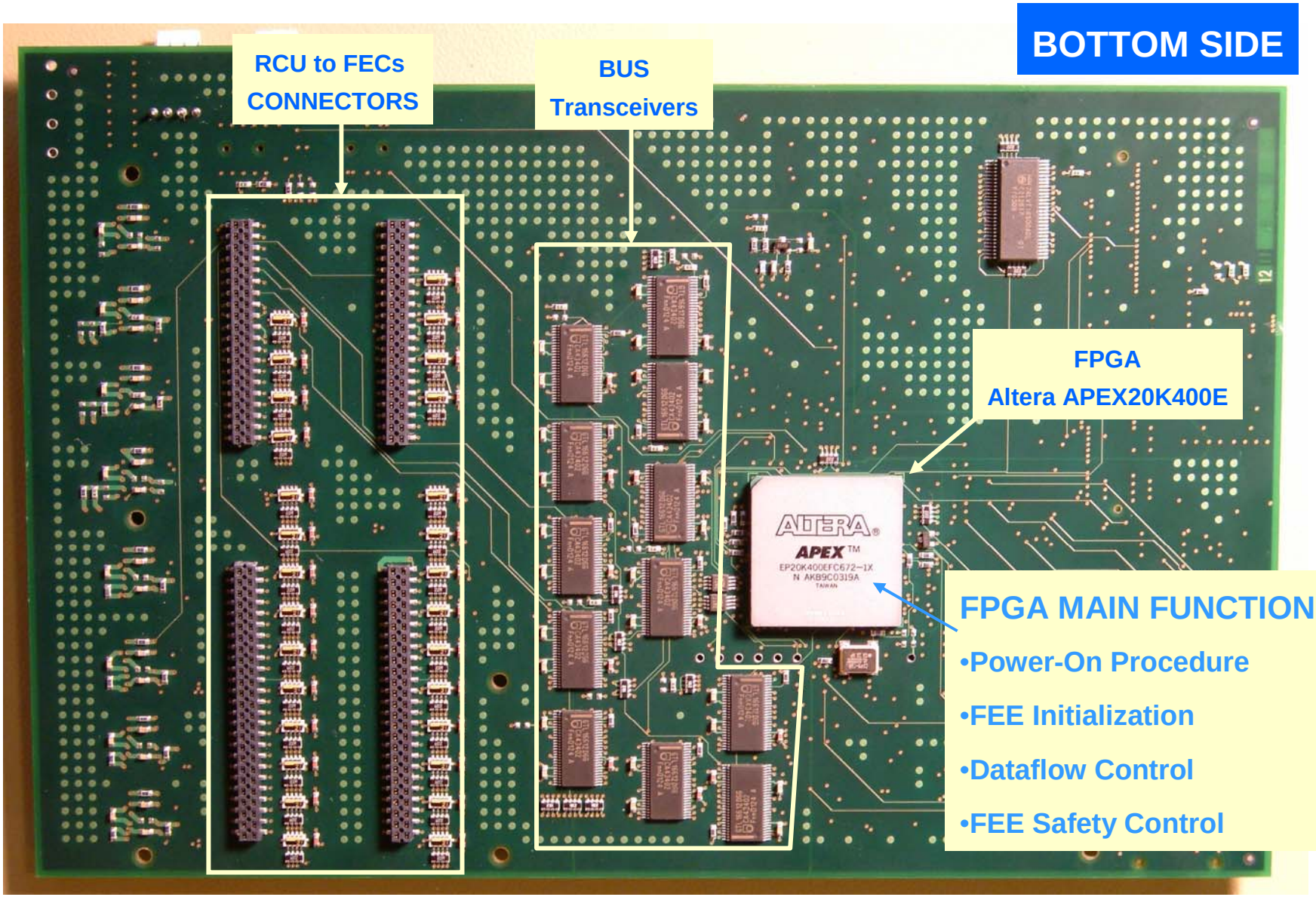


Readout Control Unit

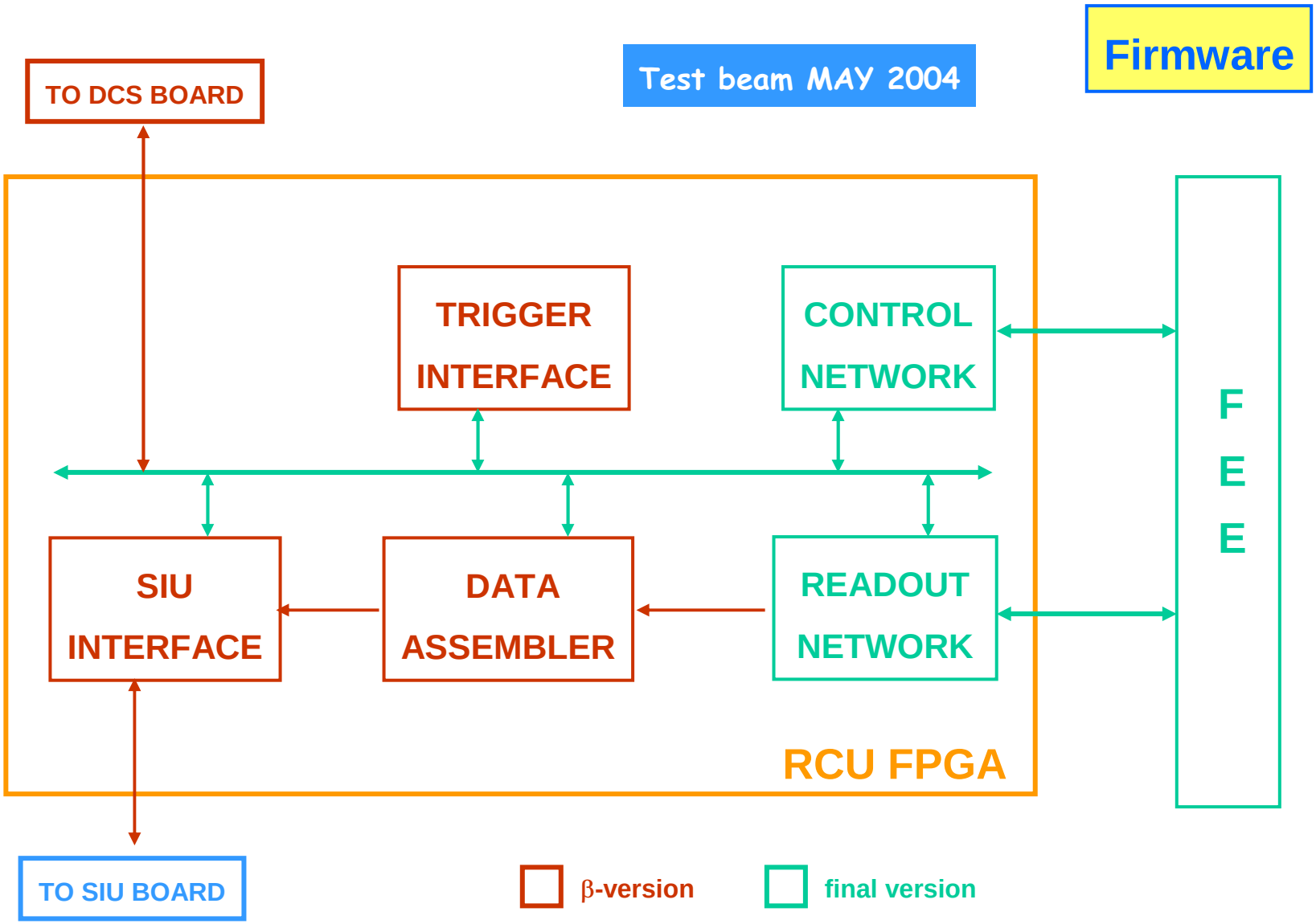
TOP SIDE



Readout Control Unit



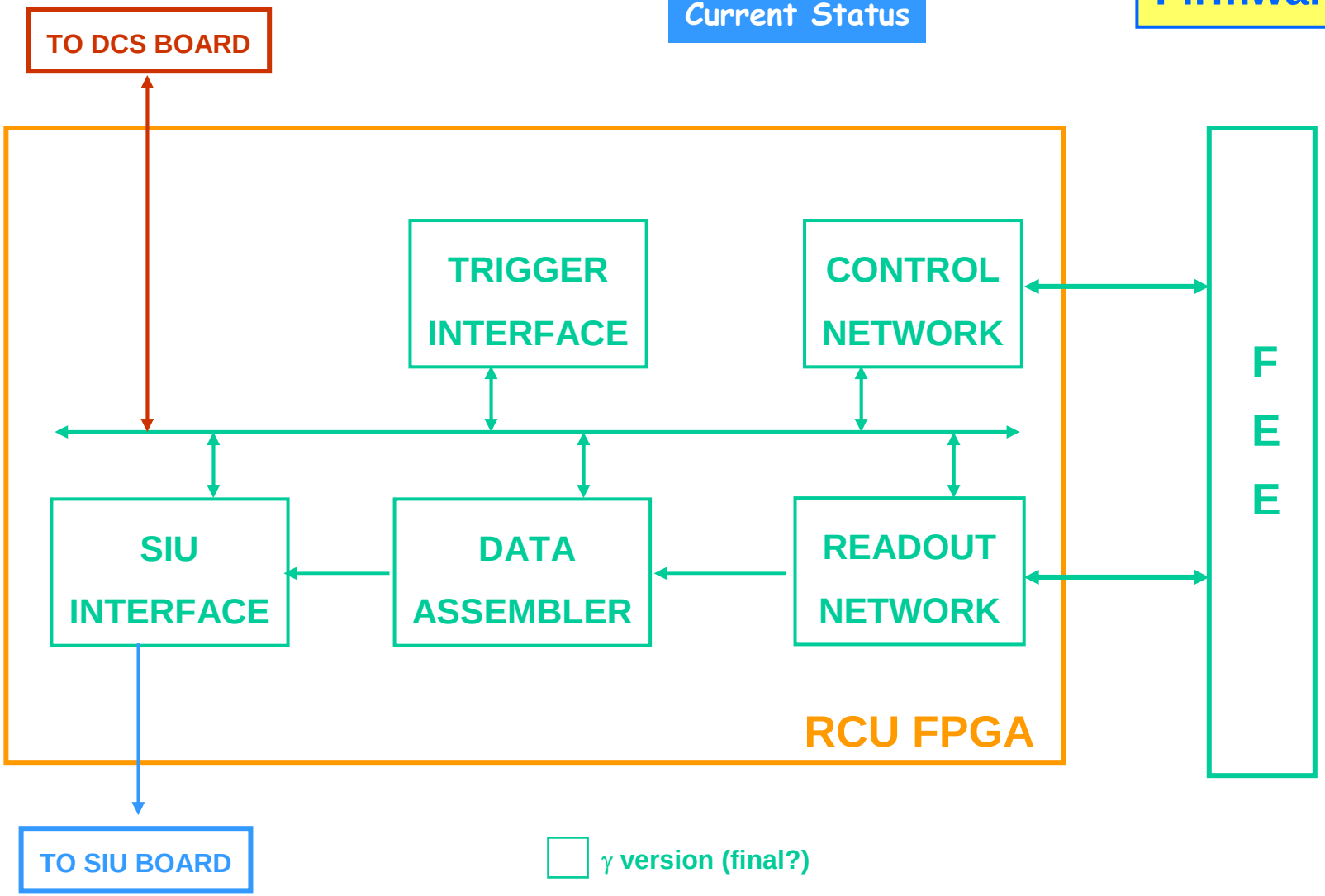
Readout Control Unit



Readout Control Unit

Firmware

Current Status



SEU in RCU FPGA

- **SEU in RCU FPGA**

Table 8.1: Expected numbers of SEUs for the different scoring regions in the TPC detector

	μ-absorber side					
Sector	1	2	3	4	5	6
SEU/(FPGA s) [$x\ 10^{-6}$]	2.4 ± 0.4	2.0 ± 0.4	1.6 ± 0.3	1.1 ± 0.2	0.9 ± 0.2	0.8 ± 0.1
	non-absorber side					
SEU/(FPGA s) [$x\ 10^{-6}$]	1.6 ± 0.3	1.3 ± 0.2	0.9 ± 0.2	0.7 ± 0.1	0.6 ± 0.1	0.5 ± 0.1

- **Errors per run (4 hours)**

	Errors per run (4 hours) per TPC system
RCU	3.7
SIU	1.0
DCS	1.9

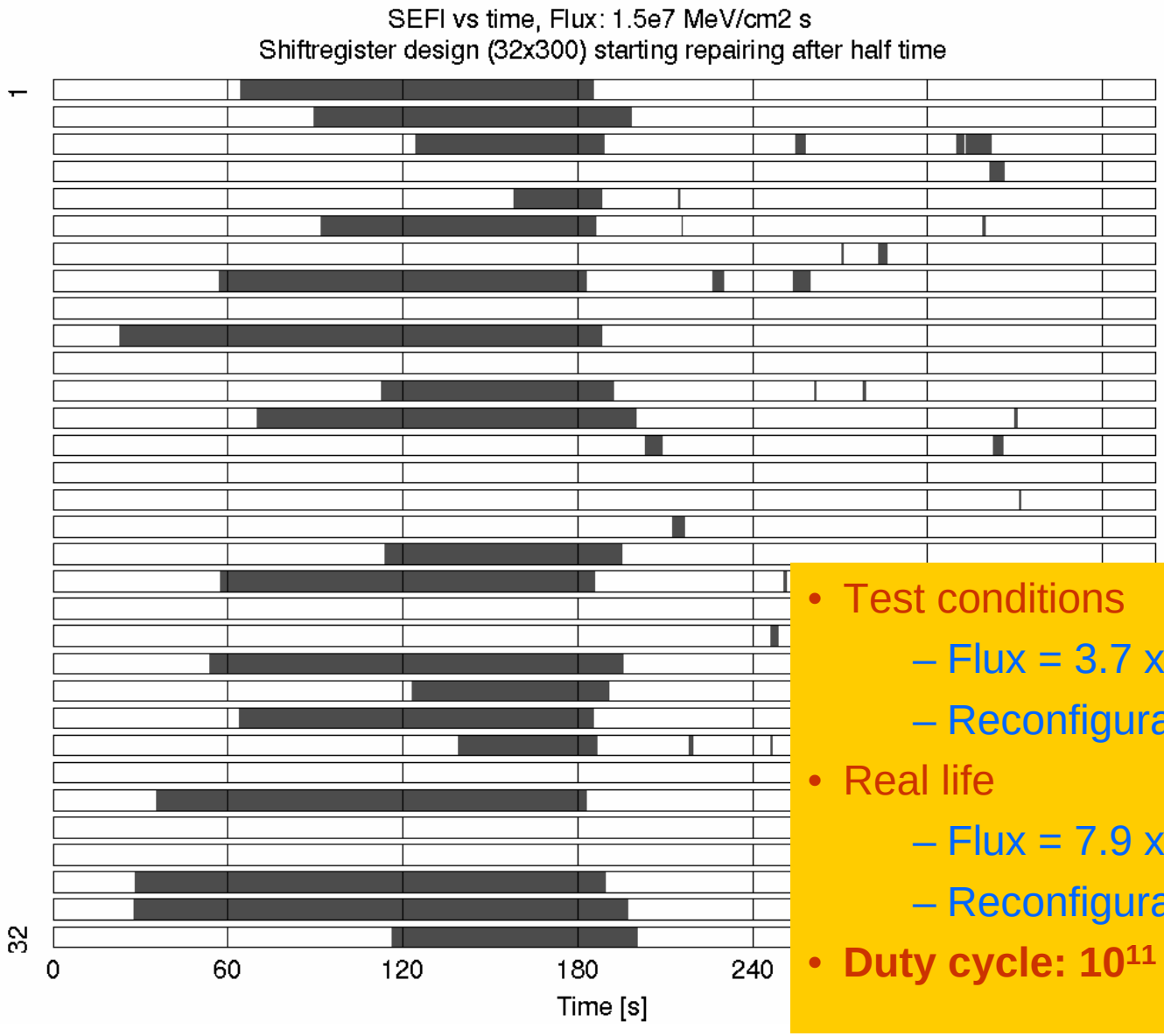
Radiation Tolerance Strategy

- SRAM based FPGAs
  - Error rate is so low that one can cope with it – if SEUs can be detected instantenously and FPGA can be reconfigured in real-time
  - ALTERA FPGAs do not provide real-time readback of configuration data nor disclose format of bitstream
  - Better choice: XILINX Virtex-IIPro FPGAs
    - Real-time (= while running) readback of configuration data for verification
    - Partial reconfiguration while running

Radiation Tolerance Strategy

- Decide to migrate RCU-FPGA to XILINX
- Select appropriate device w.r.t. resources (e.g. number of I/O cells)
- Decide to keep DCS board unchanged
- Port RCU design to new development environment
- Verify expected performance under irradiation
  - XILINX test @ OCL in August
  - System test @ TSL Q1 205 with large beam spot (∅ 30cm)

Readout Control Unit

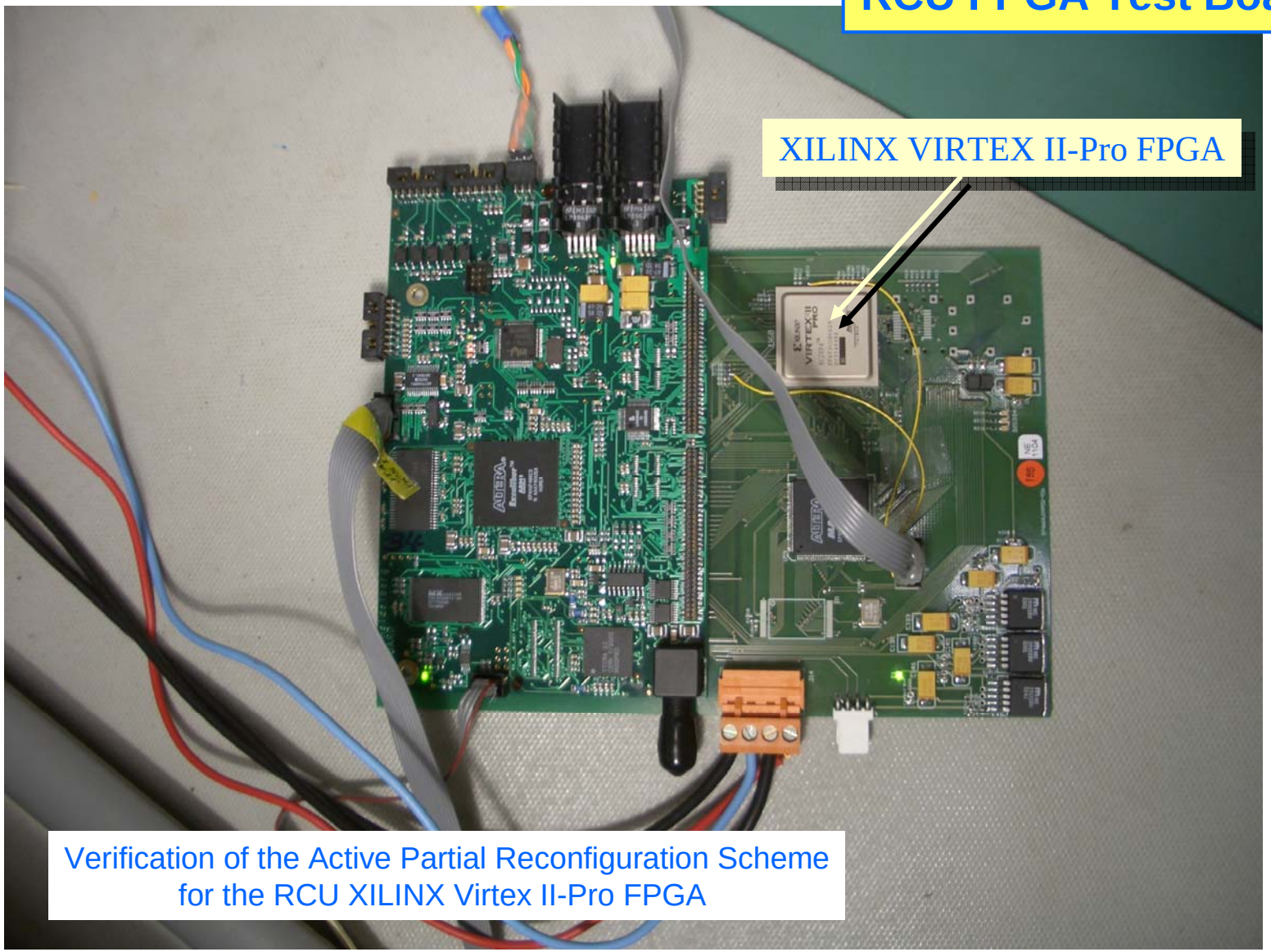


New Measurements

- SEFI test with Xilinx Virtex-II Pro FPGA
- reconfiguration started after 200 seconds:
- errors are corrected continuously

- Test conditions
  - Flux = 3.7 x 10^{11} protons/cm^2/s
  - Reconfiguration time = 5 s
- Real life
  - Flux = 7.9 x 10^{2} hadrons/cm^2/s
  - Reconfiguration time = 10 ms
- **Duty cycle: 10^{11} times better in real life**

RCU FPGA Test Board



Verification of the Active Partial Reconfiguration Scheme for the RCU XILINX Virtex II-Pro FPGA

Readout Control Unit

New RCU Status

- Schematic capture — Nov ’04
- PCB Layout — Nov ’04
- FPGA Test board — Done
- Board ready for test — Dec ’04
- Qualification of final RCU — Jan – Mar ’05

Milestone #231, RCU Start Production: Apr ‘05

Milestone #395, RCU End Production: May ‘05

Milestone #236, RCU Test: Jun-Sep ‘05

INSTALLATION ELECTRONICS (#247) Jun – Aug ‘05

Testing Procedure during the installation

During the installation, the FECs are tested separately by means of a dedicated "mounting test tool" (FEC to USB interface)

- Measurement of VCC_A, VCC_D, I_A, I_D
- Test of all CSRs, Control & Readout path
- Initialization of the FEC
- Generation of the trigger and clock signals
- Readout of trigger related data
- Connection to the pad plane

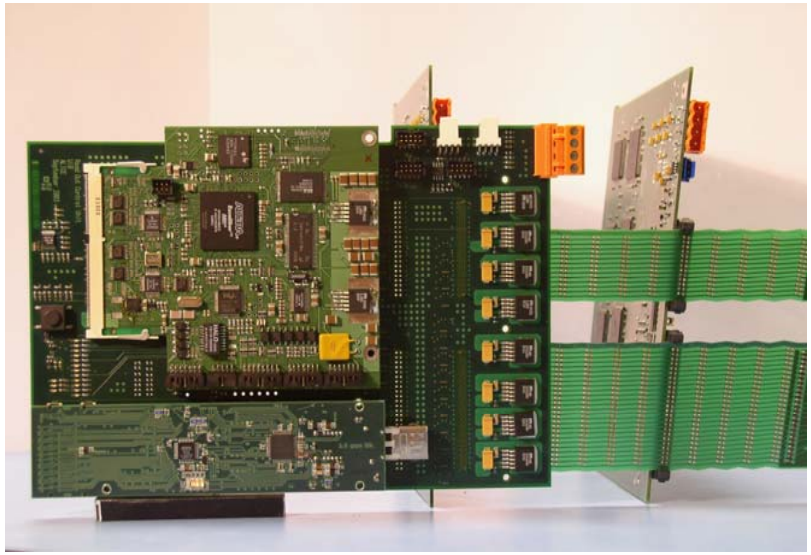
Requirements

- TPC PULSER (properly shaped pulse injected into all gate wires)

Post-installation Tests

Once all FECs of one Readout Partition are mounted on the SSW and connected to the chamber, the installation continues with:

- Backplane (2 x PCBs with 50 connectors)
- RCU
- Power cables
- DCS cable, Trigger fiber, DDL fiber
- Cooling pipes



Test procedure

- Communication with DCS, Trigger, and DAQ
- Special patterns to test the readout & ctrl backplane
- All tests performed separately on the FECs are repeated
- Legal and illegal trigger sequences