*Carmen González Gutierrez (CERN – PH/ED)*

# The ALICE TPC Readout Control Unit

10th Workshop on Electronics for LHC and future Experiments

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*Outline:*

- ✓ *System overview*
- ✓ *Readout chain*
- ✓ *Readout Electronics Architecture*
- ✓ *Summary and Conclusions*

**CERN**

- L. Musa
- R. Campagnolo
- C. González Gutiérrez
- B. Leitao Mota

**University of Bergen, Norway**

- D.Röhrich
- K.Ullaland
- B. Pommersche
- J. Lien
- J. Alme
- Ketil
- M.Richter

**University of Oslo, Norway**

- S. Solli

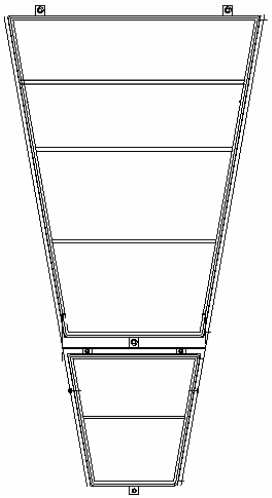
**Ruprecht-Karls Universität Heidelberg, Germany**

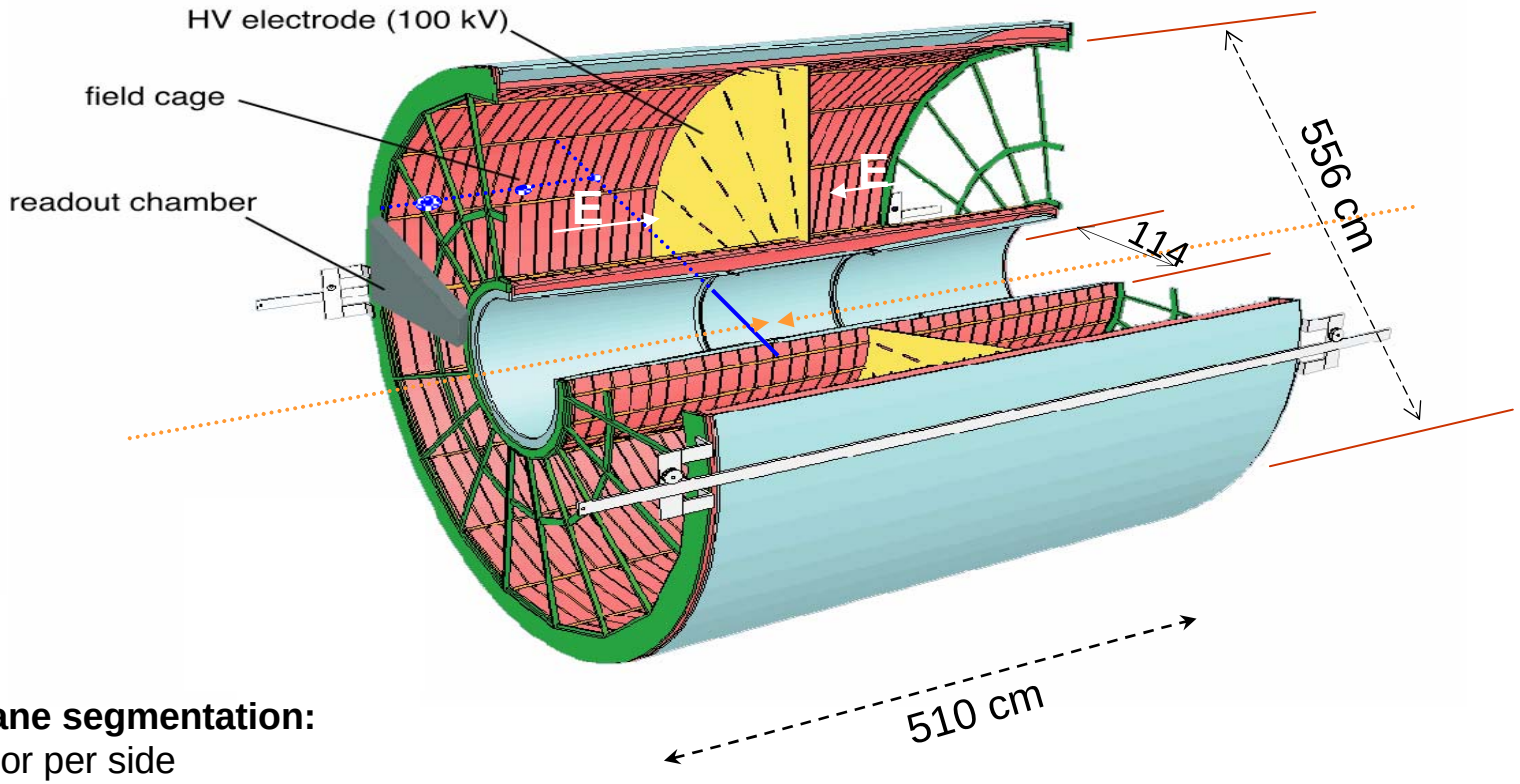
- V. Lindenstruth
- D. Gottschalk
- M. Stockmaier
- V. Kiworra
- T. Alt
- T. Krawutschke

**ZTT Worms, Germany**

- S. Bablock
- C. Kofler

# System Overview: The ALICE Time Projection Chamber



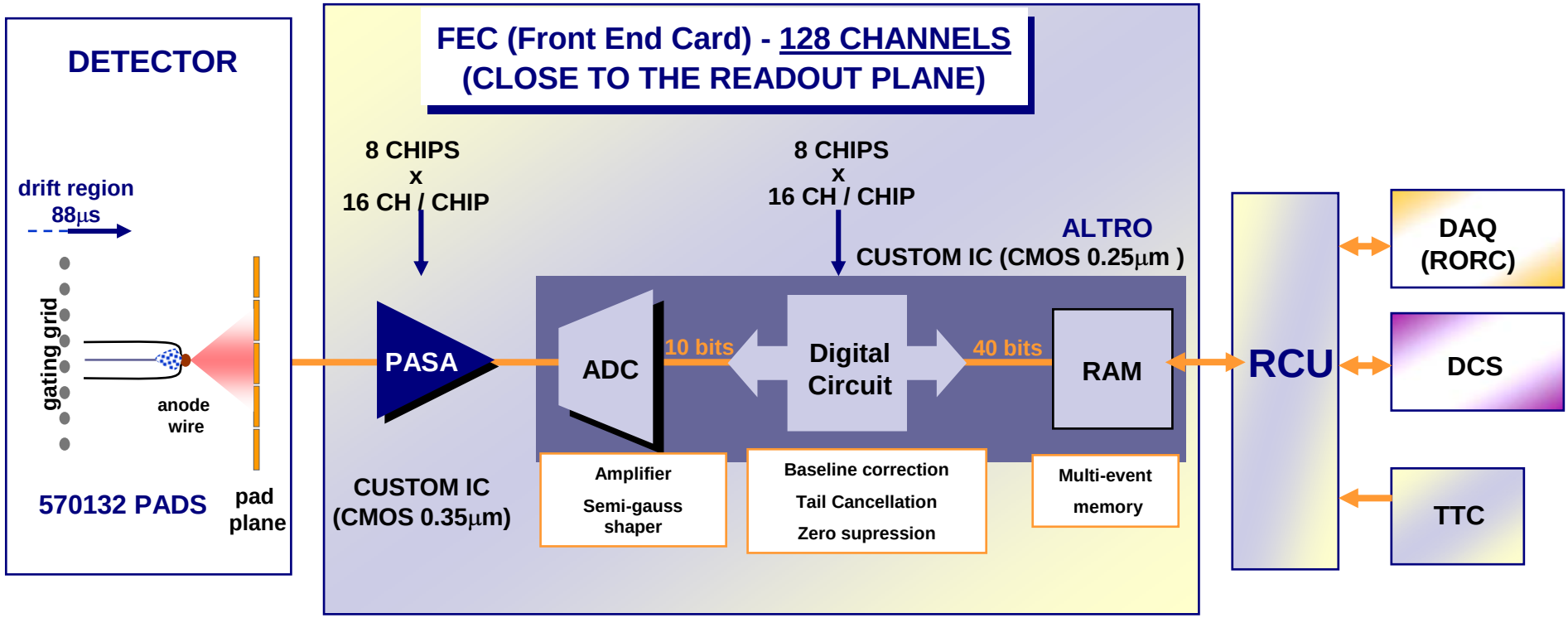



- **Readout plane segmentation:**
  - 18 sector per side
  - 6 readout partition (6 RCU)

- **Large Data Volume**:
  - **570132 pads** x 1000 samples = 712 Mbytes / event
  - 2 scenarios:
    - Pb – Pb (@ 200 Hz) → 142.5 Gbytes / s
    - p – p (@ 1 KHz) → 712 Gbytes / s
  - Data compression (zero suppression) in FEE

# Readout Electronics Architecture 1 / 2

*Data flow from the detector to the Data Acquisition System (DAQ)*

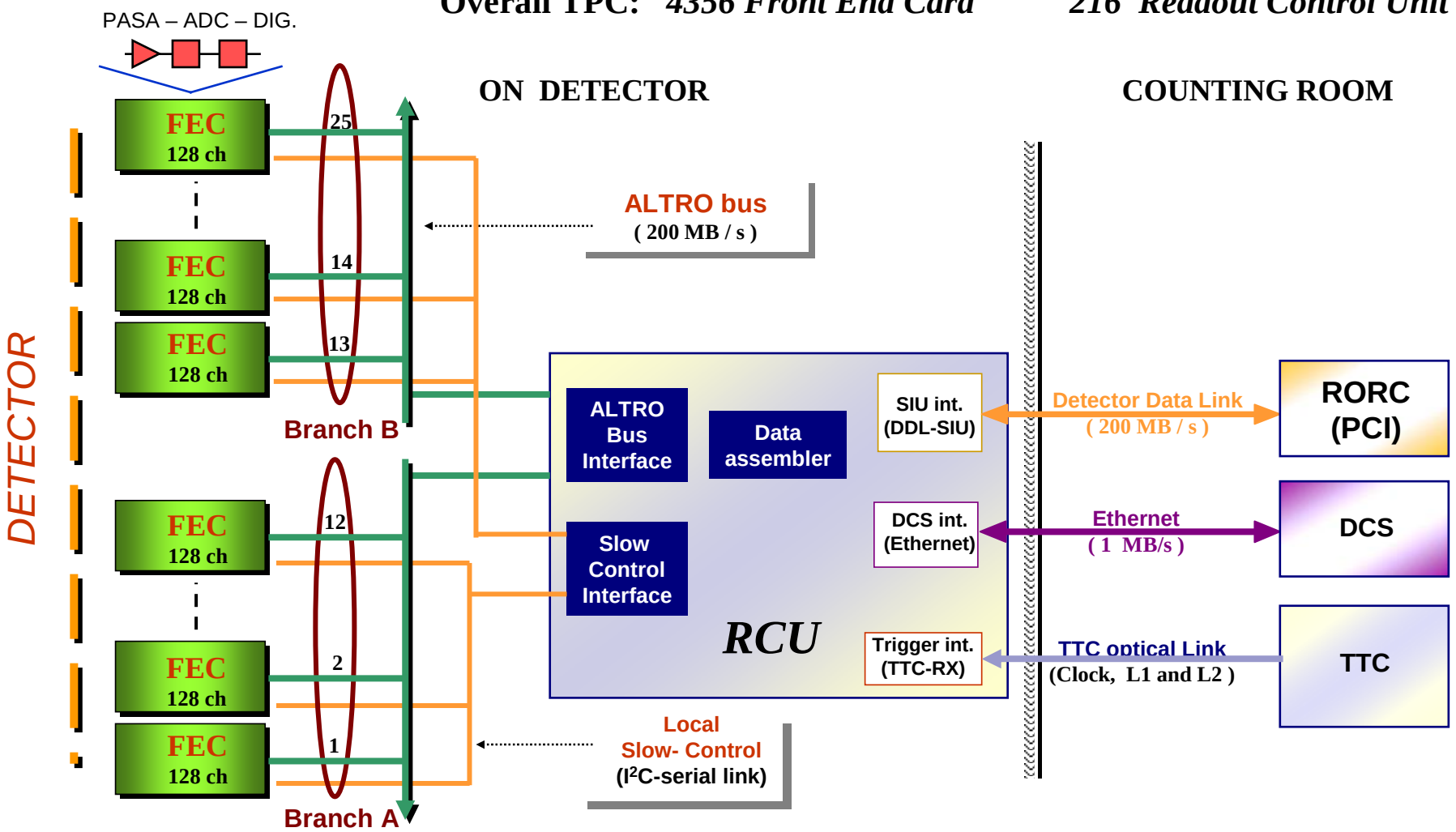



- A single readout channel is comprised of three units: a charge sensitive preamplifier/shaper (PASA), an 10 bits Analog-to-Digital Converter (ADC) and a digital processing chain with a multi-event-memory

# Readout Electronics Architecture 2 / 2

***Each of the 36 TPC Sector is served by 6 Readout Subsystems***

**Overall TPC:** *4356 Front End Card* *216 Readout Control Unit*



# Readout Control Unit (RCU)

- Functions:
  - Readout related:
    - Configuration of the ALTROs (via the DDL or the DCS)
    - Distribution of the trigger and clock signals (from the TTCrx)
    - FEC data readout and transfer to the DAQ via the DDL

    *by the **ALTRO bus (VME-like custom bus)***
  - Slow Control related:
    - Supervision and monitoring:
      - Configure the power state of the FECs
      - Temperature, Current and Voltage variations
      - Read status parameters (L1 and L2 counters …)
      - Interrupt and error handling

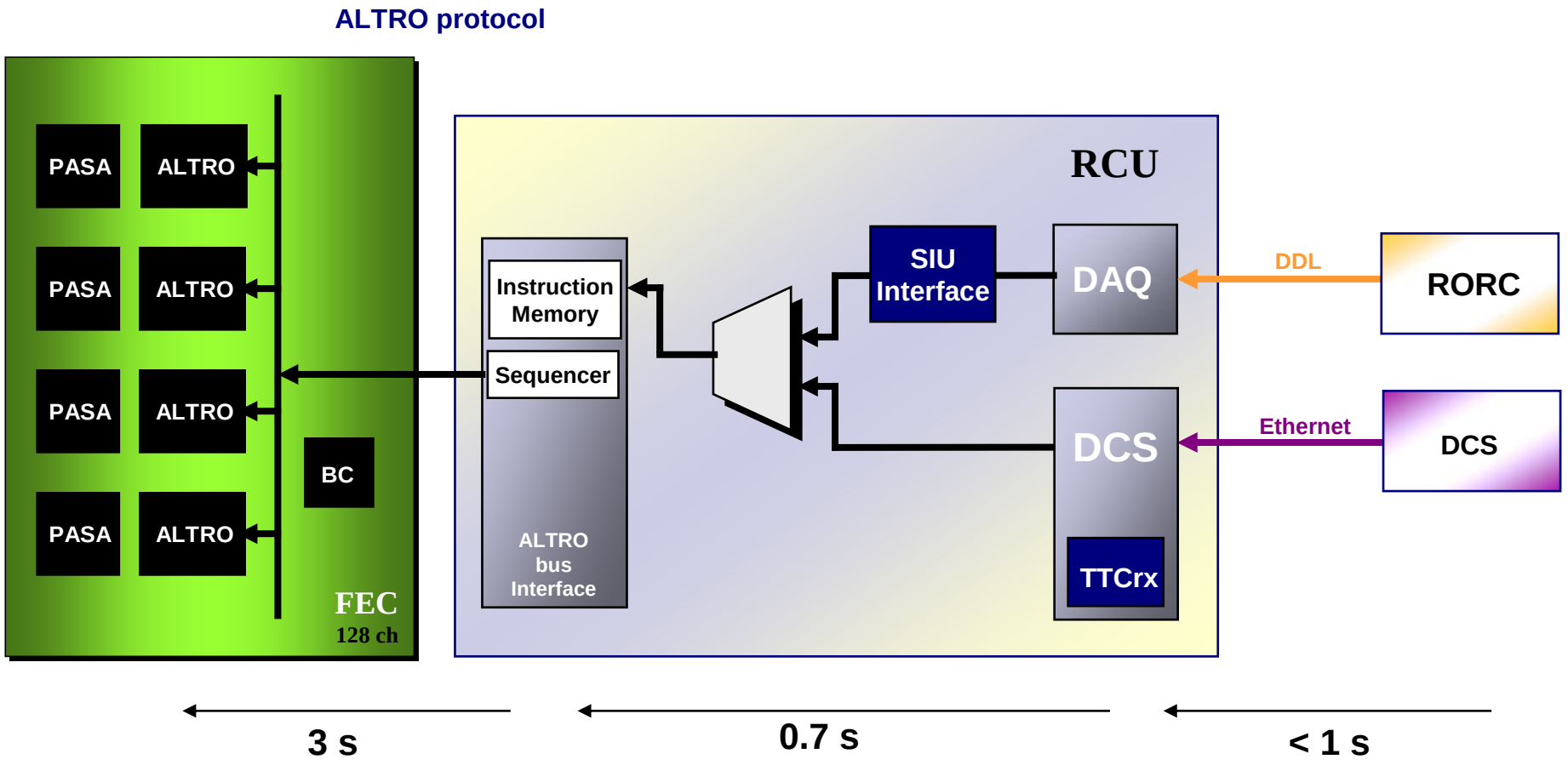
    *by the **Local Slow Control bus (I2C-like custom bus)***

- Implementation:

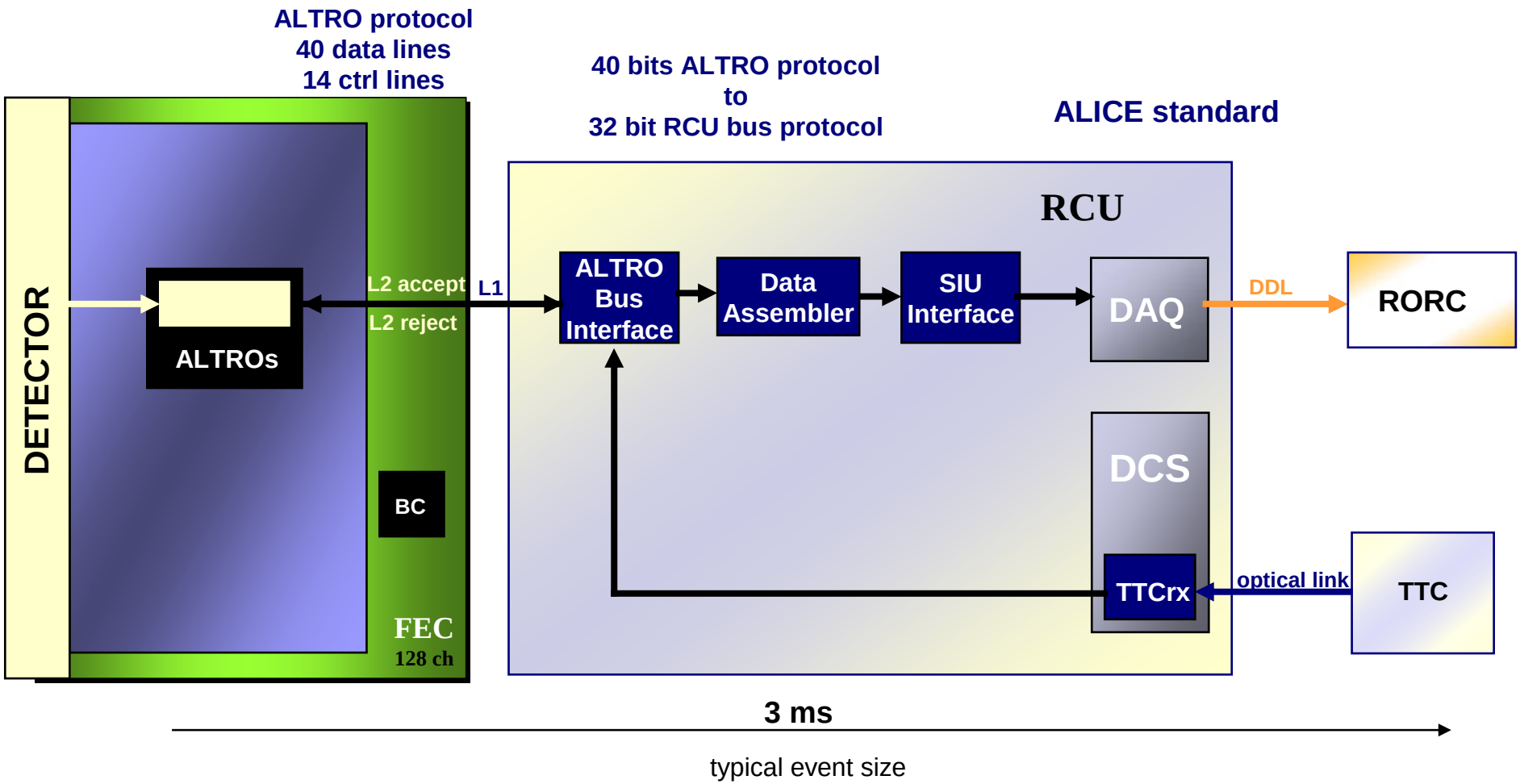
The RCU has been implemented as a motherboard with two mezzanine cards:
- SIU - DDL interface
- TTC and DCS interface.

# Initialization (set up time)

- The configuration of the electronic (baseline, thresholds, tail cancellation coefficients, etc) can be performed via both DAQ and DCS card
- Overall configuration data: 7 MByte/RCU
  - 3200 active channels
  - 1000 samples/channel



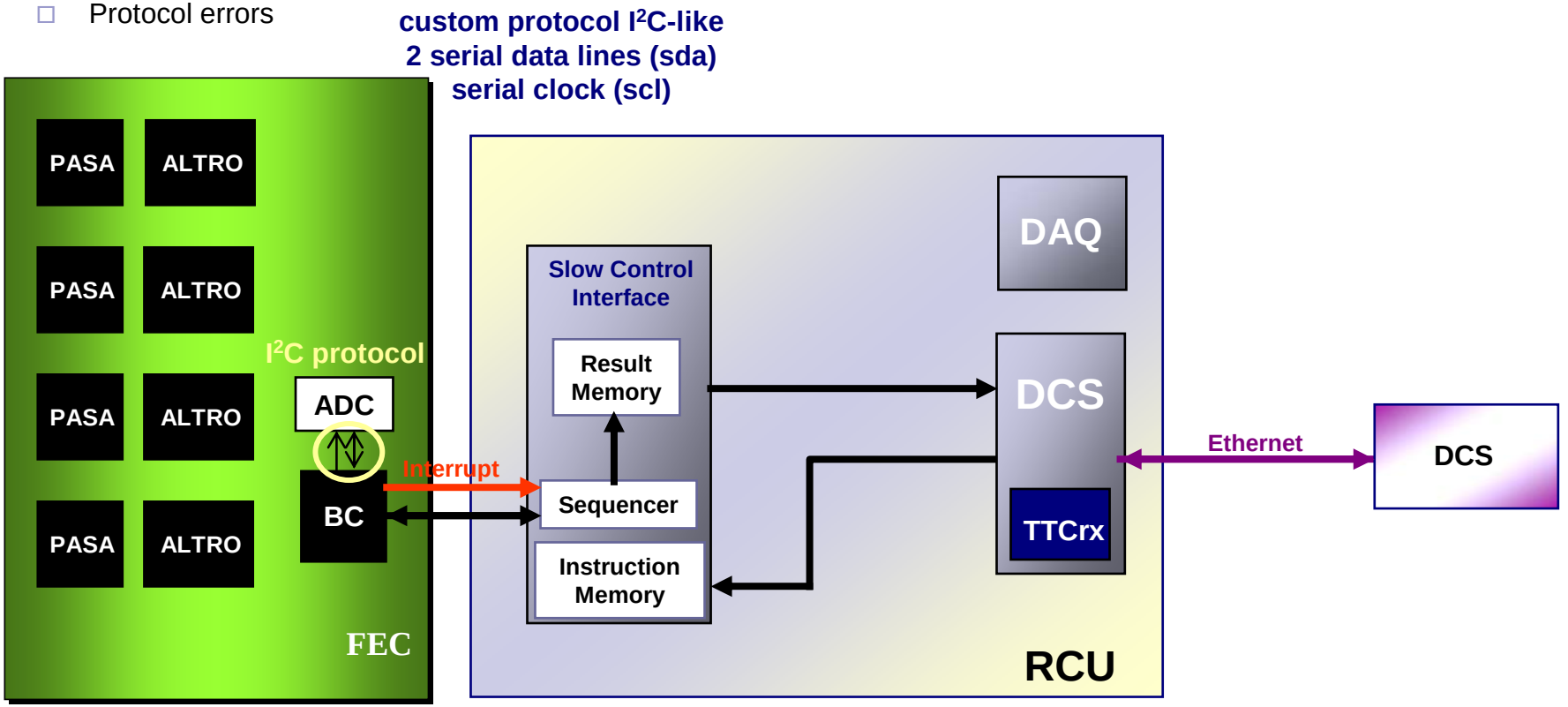
# Data Readout (run time)



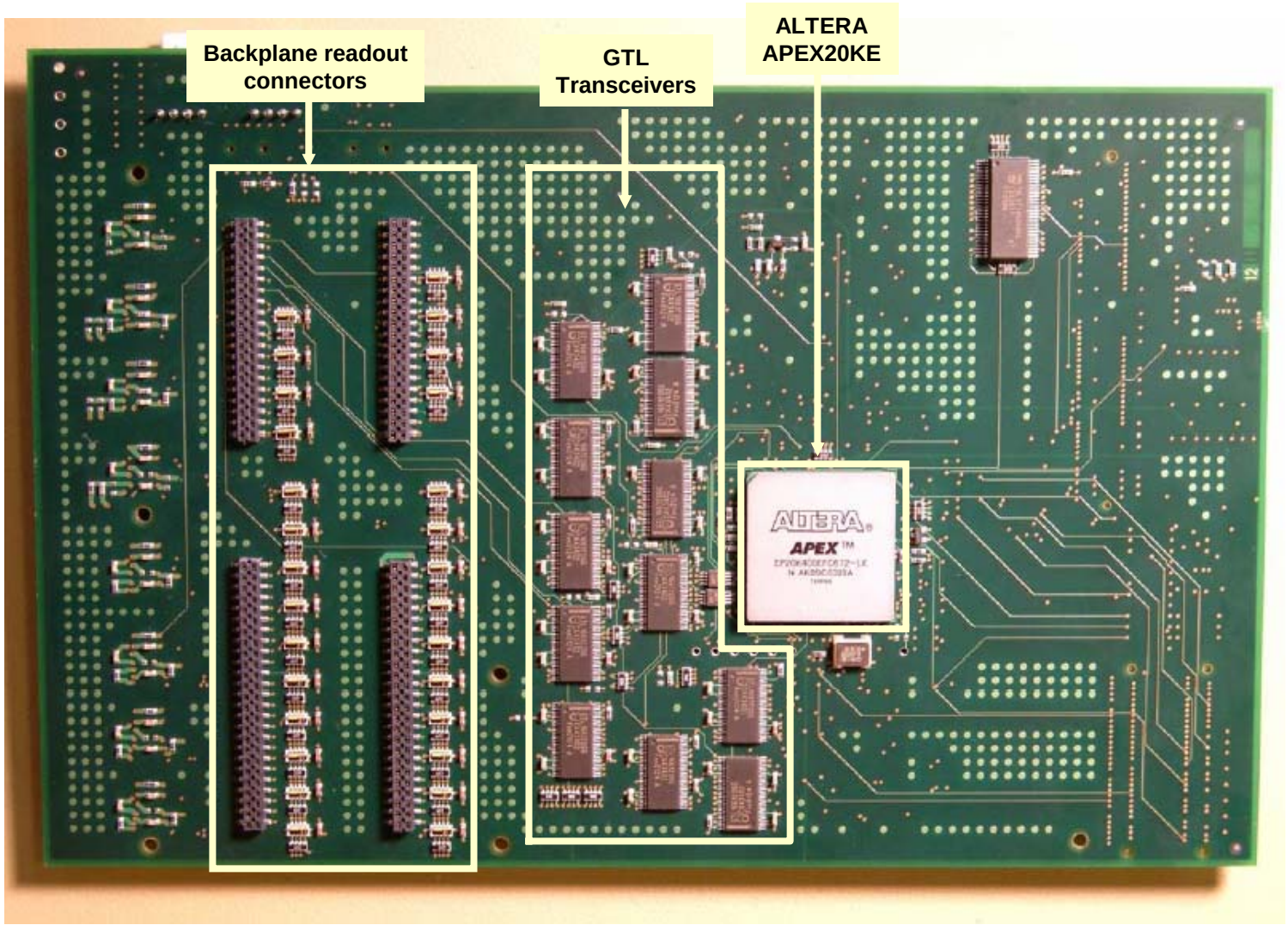
# Detector Control System

The functional requirements for the DCS interface are the following:

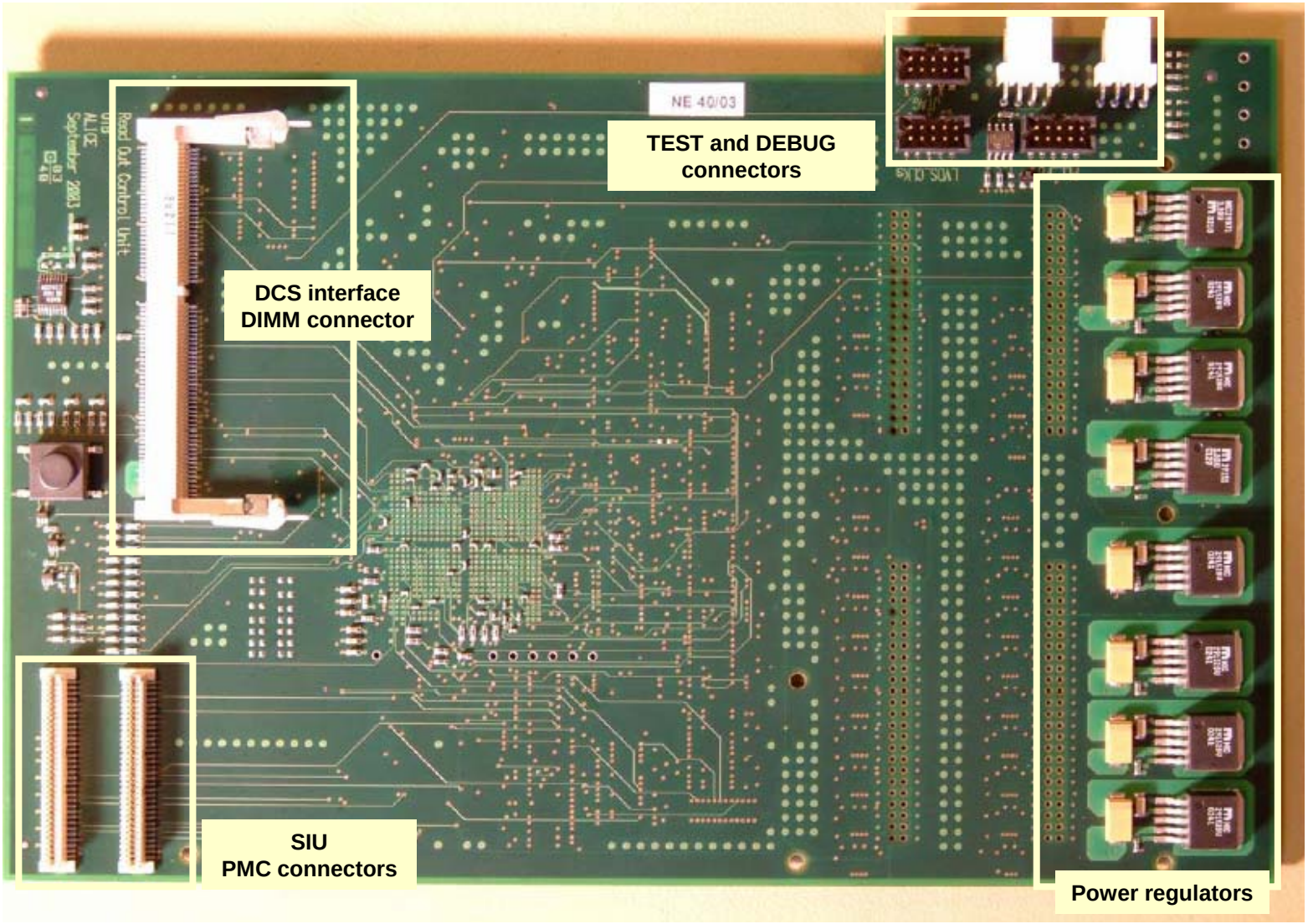
- **Configure power state on all FECs**
- **Monitoring**:
  - power and temperature on all FECs using a 4 Channel A/D Converter with an On-Chip Temperature Sensor
  - different counters (L1, L2, sclk …)
- **Error and Interrupt handling**
  - Temperature or currents over thresholds
  - Voltages under threshold
  - Power supply errors
  - Missed sclk
  - Protocol errors



# RCU Motherboard - Bottom view



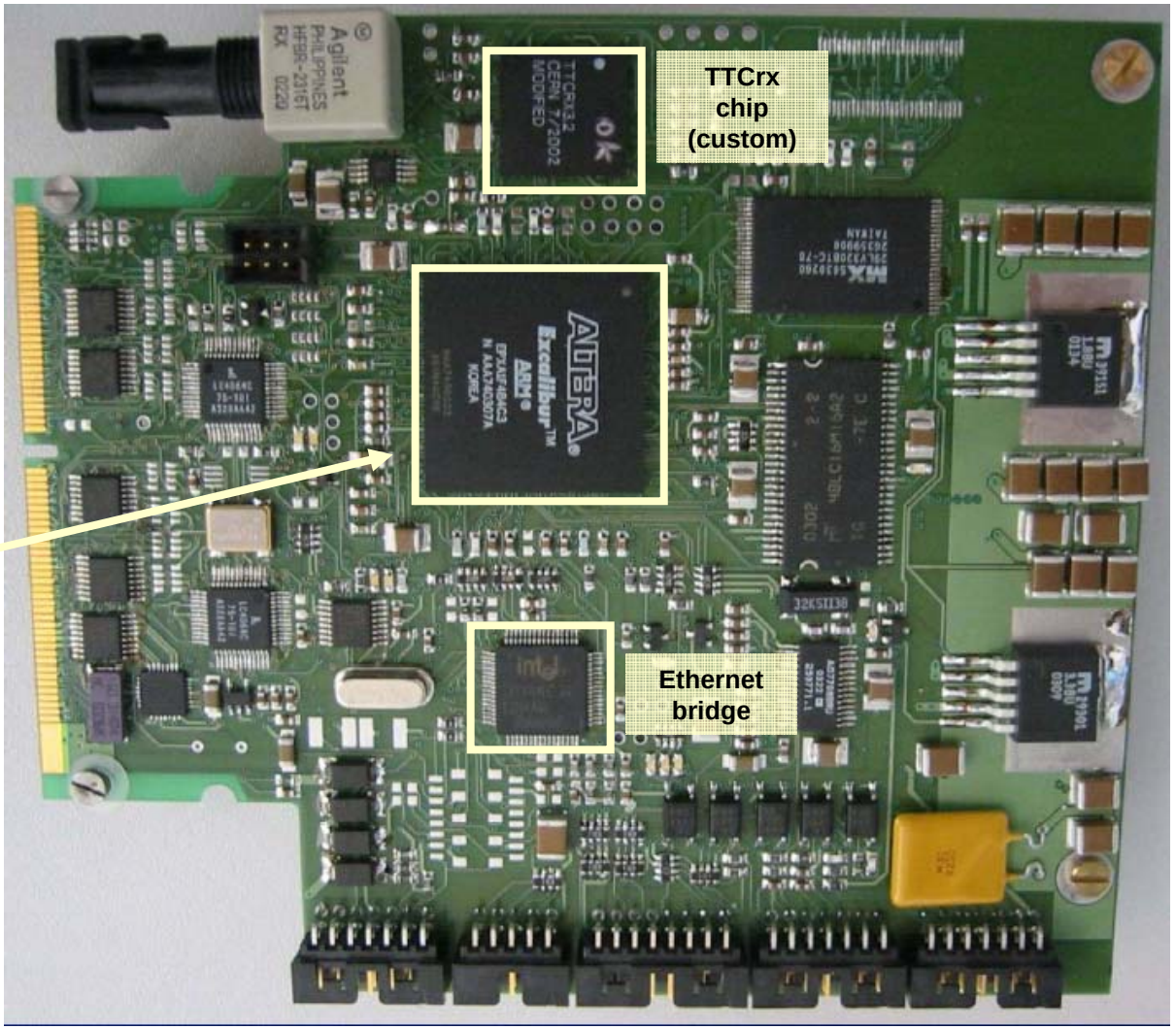
# RCU Motherboard - Top view



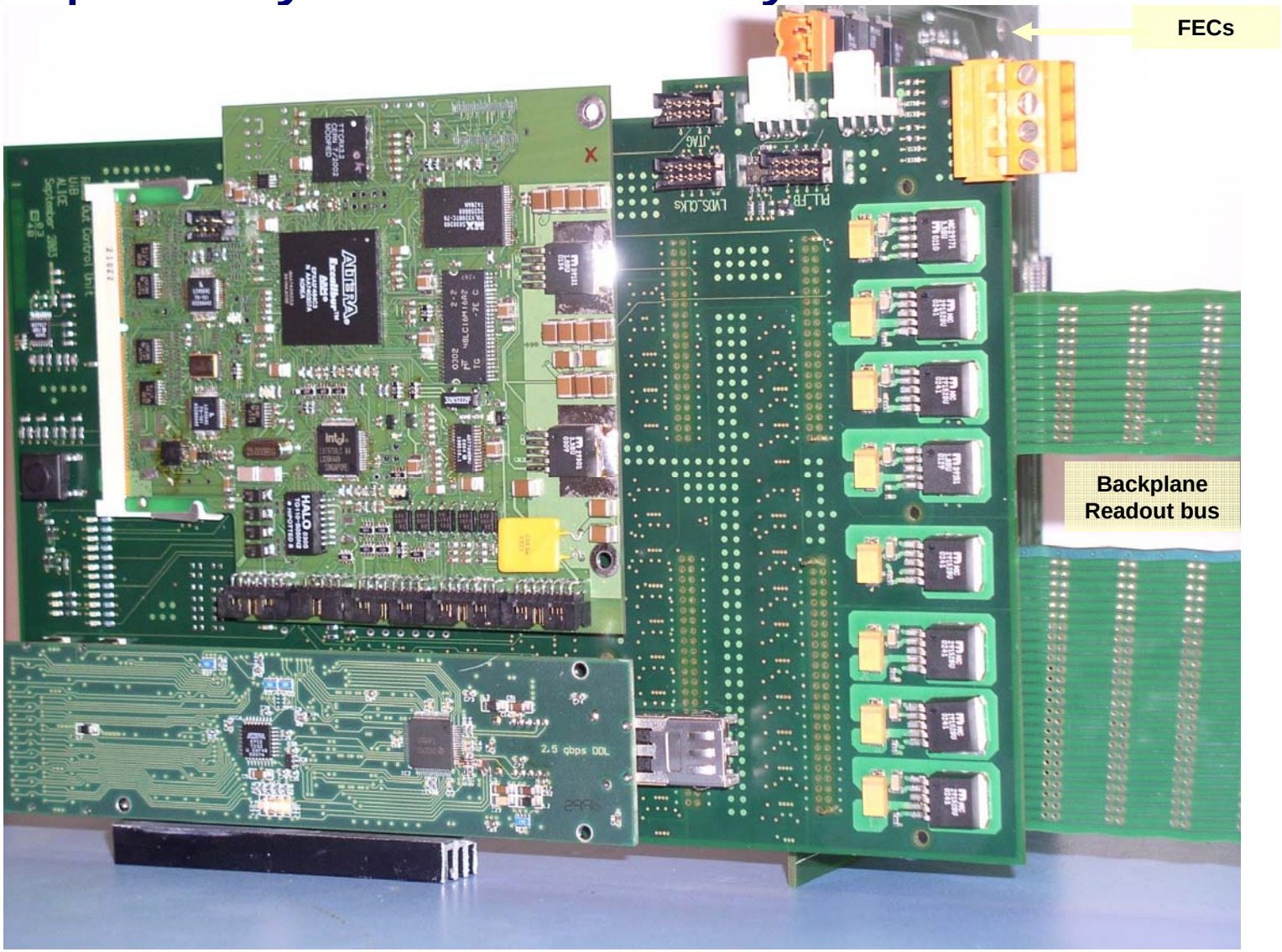
# TTC and DCS mezzanine card

- Tasks:
  - Configuration
    - RCU
    - FEC
  - monitoring / controlling the FEE
  - configuration/readout of the TTCrx
  - distributing the L1 and L2

- ALTERA Excalibur:
  - FPGA EP20K100
  - ARM922T hardwired processor
  - running Linux stored in a flash memory



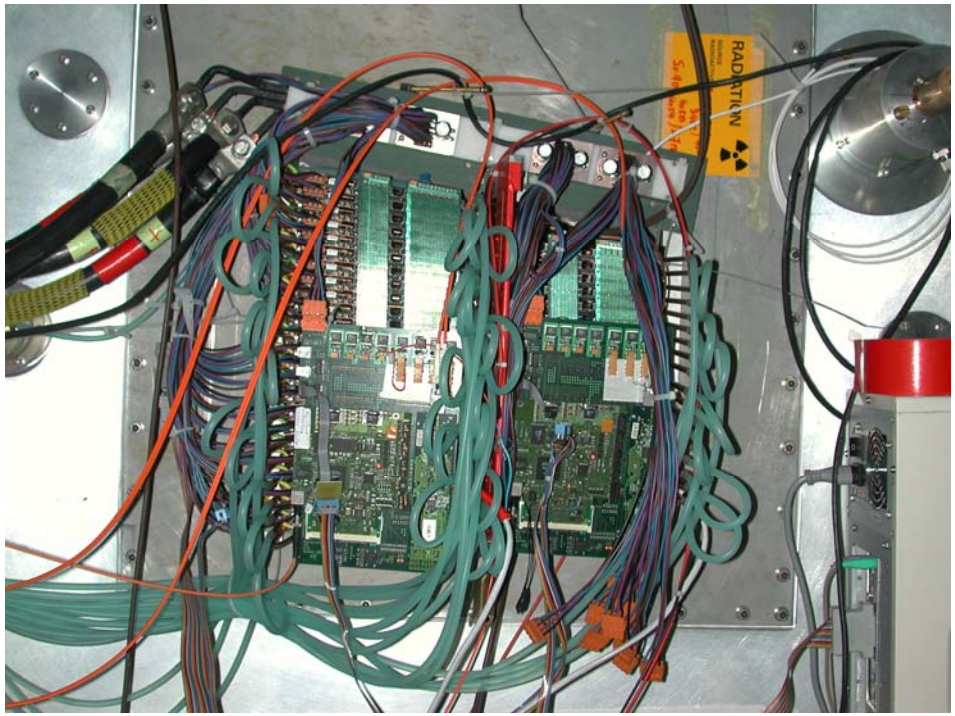
# Complete system Assembly

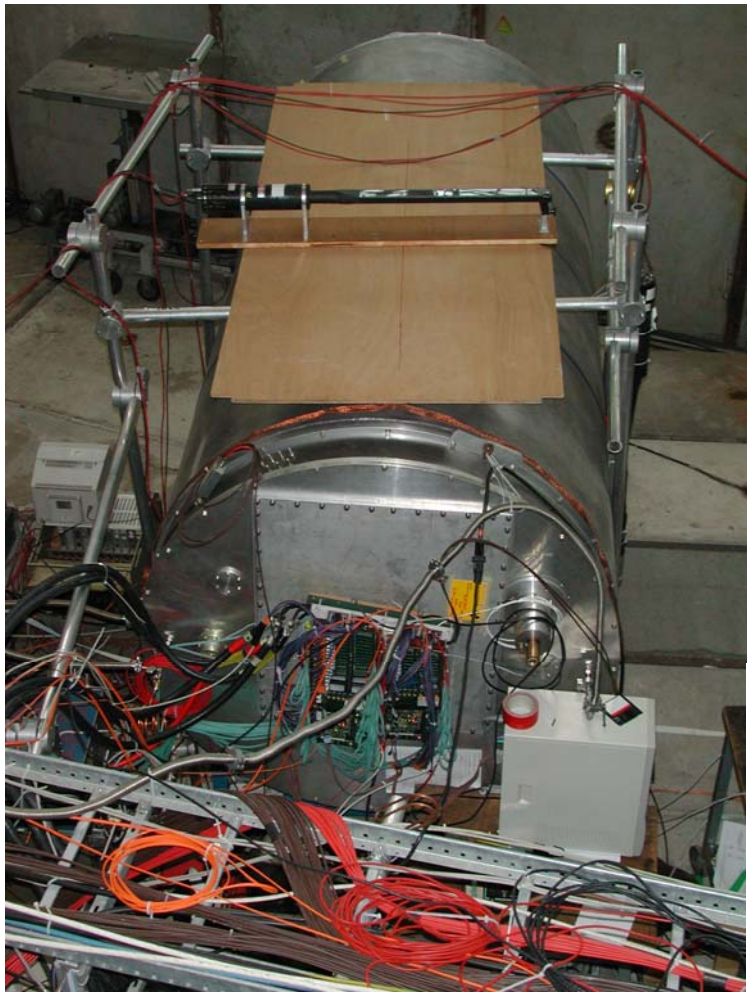


# FEE integration with other detector components

**Configuration for the May 2004 Test-Beam :**

IROC in Field Cage prototype readout with:
- 43 FECs ( 5500 channels , ~ 1 % of Alice TPC )
- connected to 2 RCUs by
- 4 branches of ALTRO readout backplanes.
- 2 DCS boards interfaced to the RCUs and connected to the TTC,
- 2 SIUs for the DDL



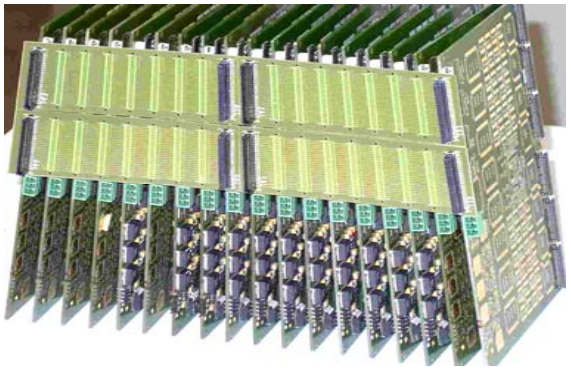
# Summary and Conclusions

- The FEE for the ALICE TPC, which consist of 570132 channels, produces a very large data volume
- The readout is organized in Front End Cards of 128 channels each
- 216 Readout Control Units (RCU) are interfaced to 4356 FECs
- The RCU configures the FECs, distributes the clock and trigger information, reads-out and transfers the data from the detector to the DAQ
- The full system has been successfully tested with others detector components during the test beam in May 2004

  (readout of a 5500 channels IROC in Field Cage prototype)

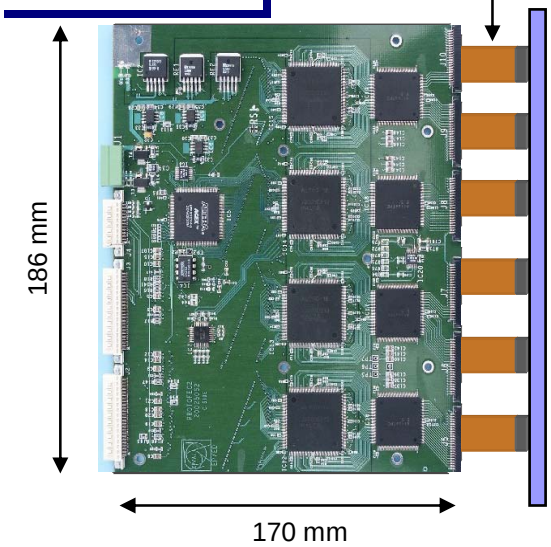
# End of presentation

# RCU – FEC Assembly



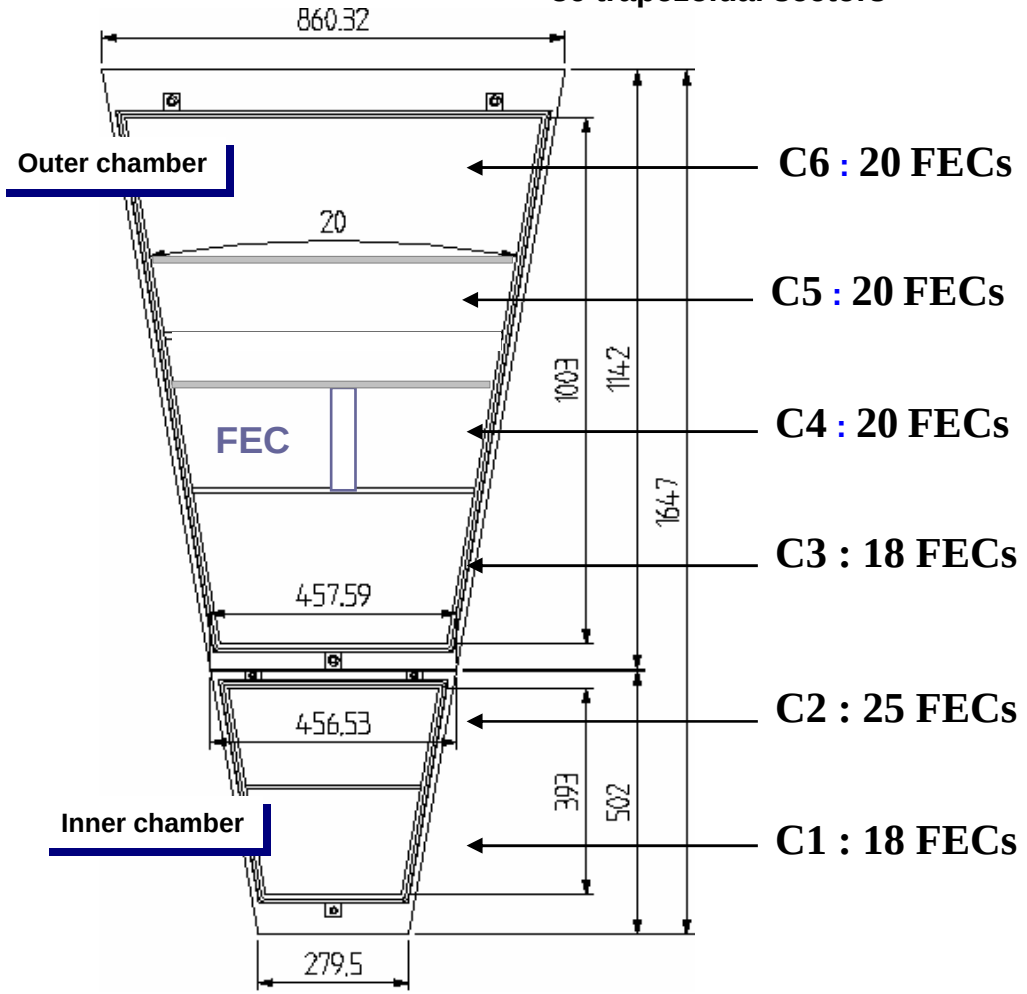
Kapton Cable

**SIDE VIEW**




**FRONT VIEW**

**36 trapezoidal sectors**



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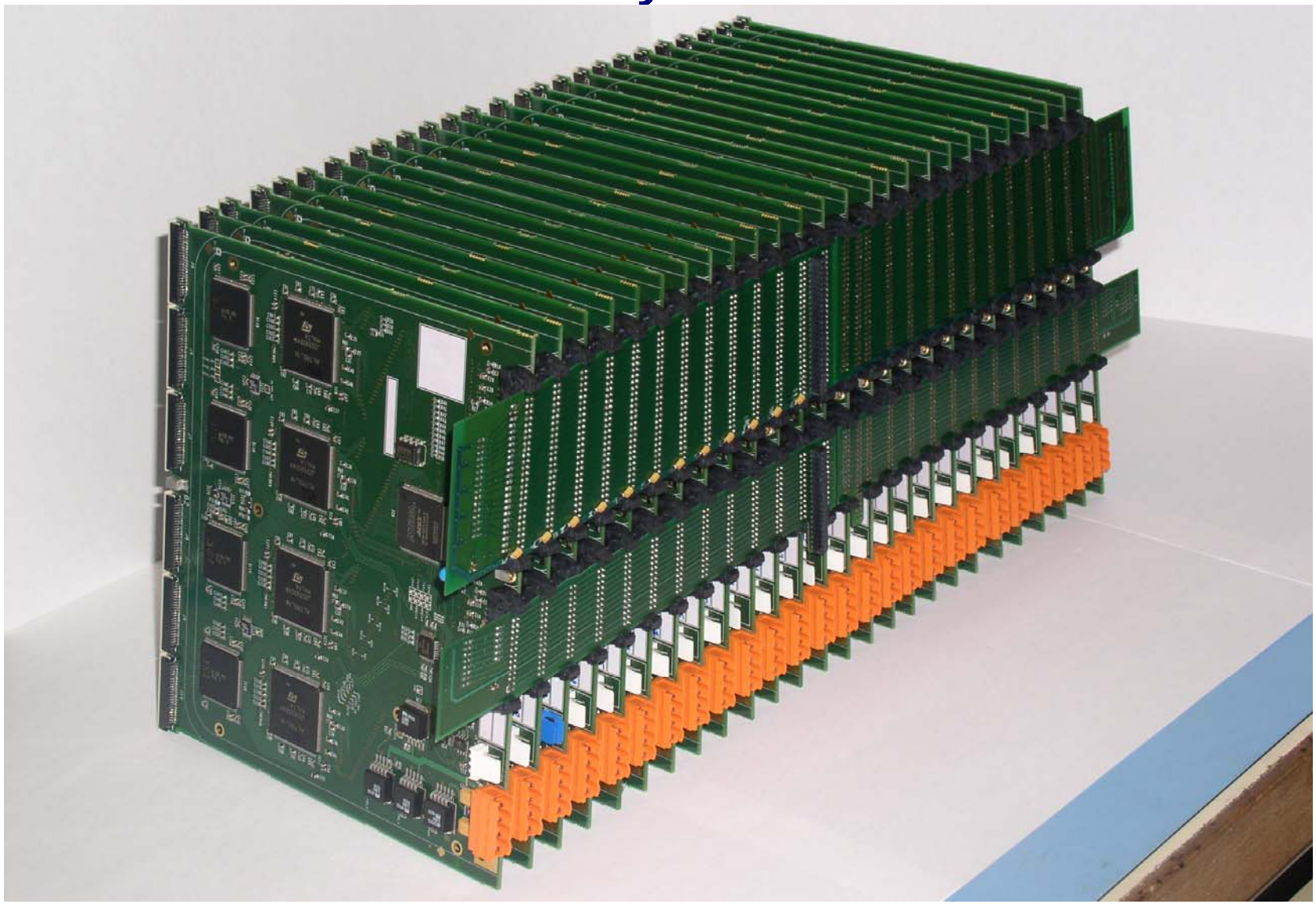
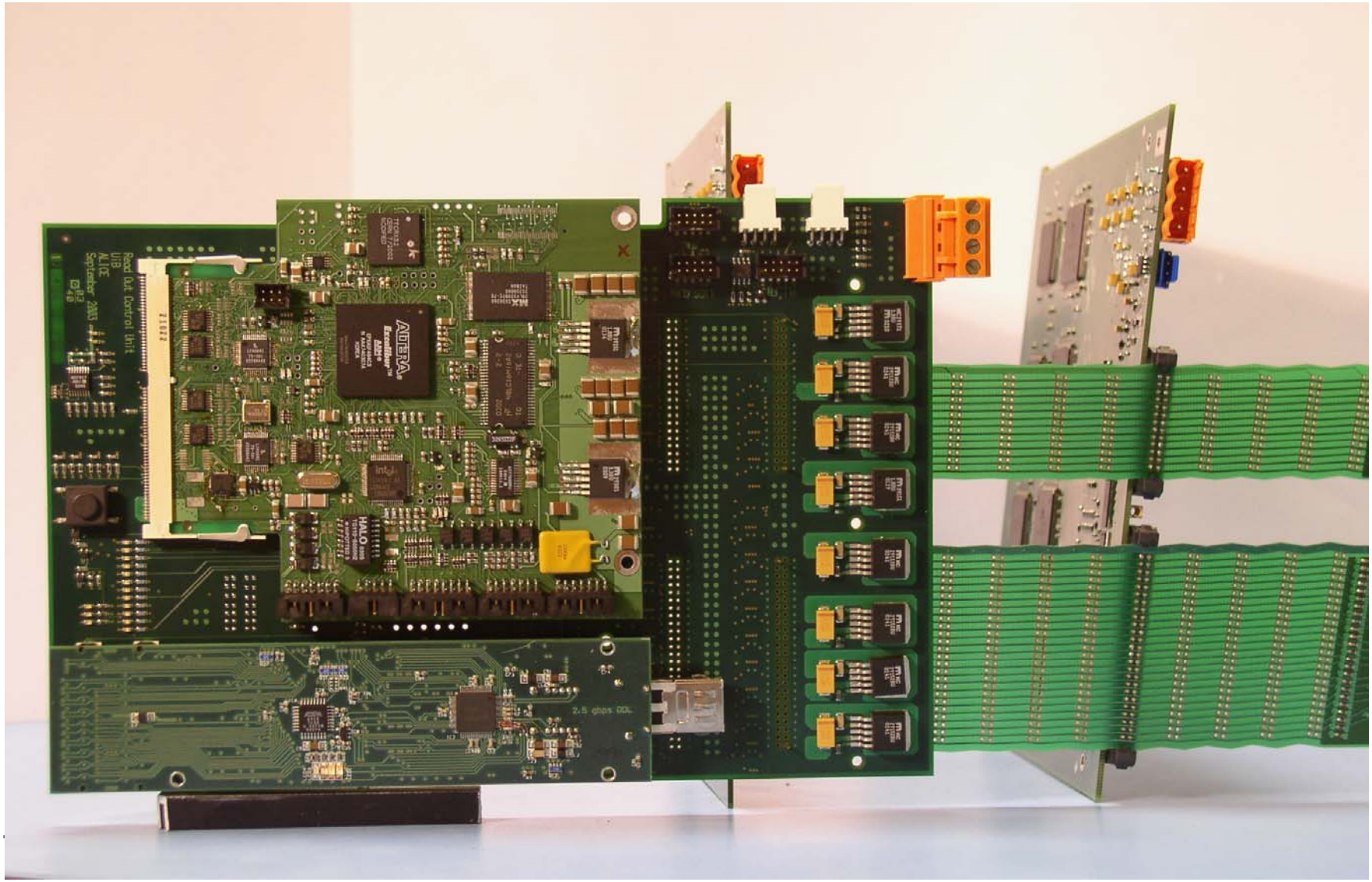
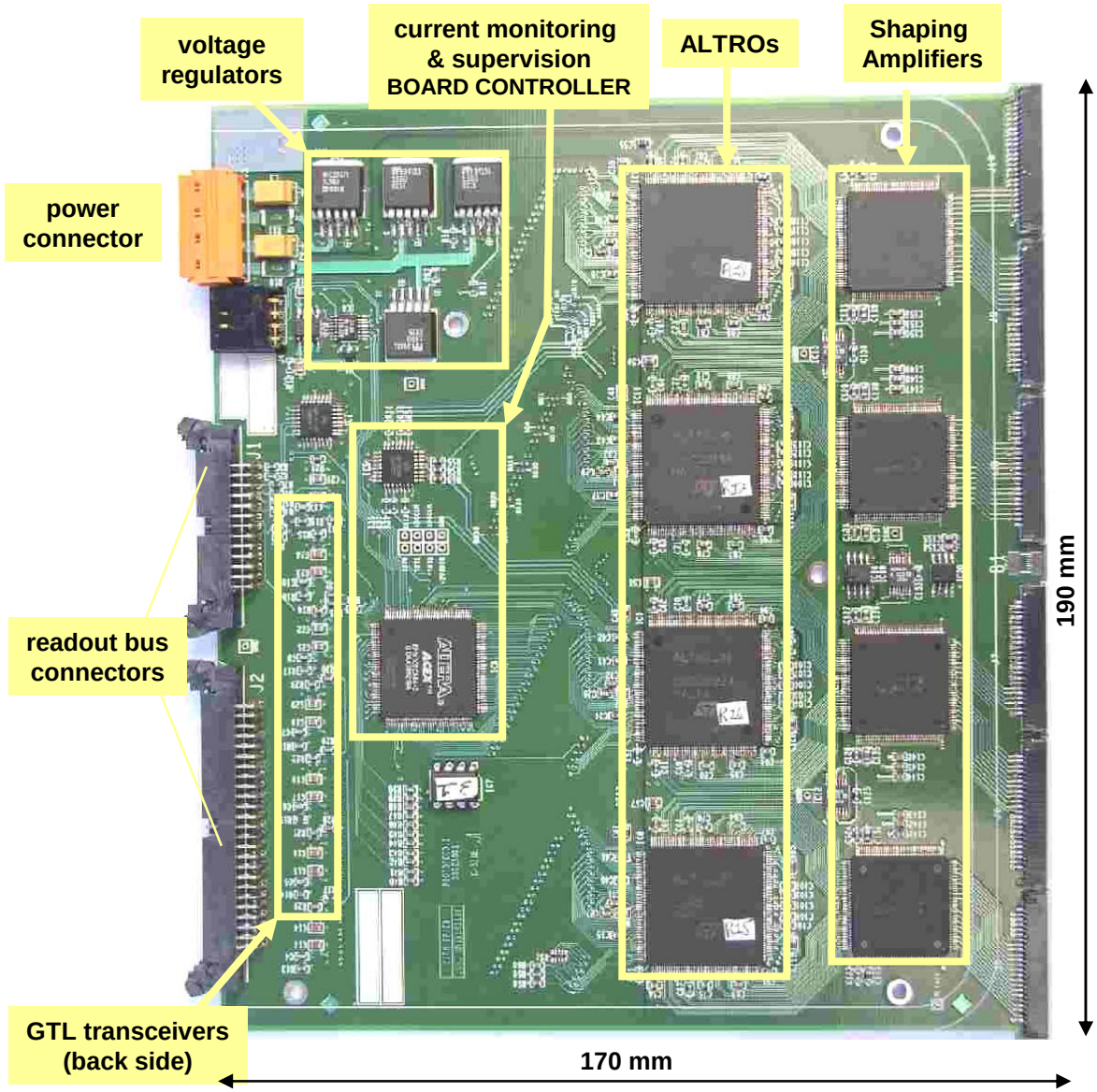


# RCU – FEC Assembly



# The 128 channels Front End Card (FEC)




- Commercial components
  - Power regulators
  - Power connectors
  - GTL transceivers
  - 4 channel ADC with a temp sensor
  - 1 FPGA (ALTERA ACEX1K) → BC
- Custom ICs
  - 8 ALTROs per FEC
  - 8 PASA per FEC