FEE Planning Update

OUTLINE

- Milestones Review
- Remaining work

TPC FEE MILESTONES

Milestone	Baseline	Status / New date		
□ PASA (40 000 chips)				
 End Prototyping: Engineering run (Start prod.): End production: End of production test: 	Jan '02 Oct '02 Mar '03 Dec '03	done (Mar '02) done (May '03) Jan '04 Jul '04 (6wks/lot)		
 ALTRO (40 000 chips) End Prototyping: Engineering run (Start prod.): End production: End of production test: 	Jan '02 May '02 Jan '03 Dec '03	done (Mar '02) done done (Dec '02) on schedule		
 FEC (4500 boards) End Prototyping: Production: Production test: 	Dec '02 Jan '03 - Jan '04 Mar '03 - Feb '04	done (but optimiz. cont.) Nov '03 – Aug '04 Apr '04 – Nov '04		

TPC FEE MILESTONES

Milestone Baseline Status / New date ☐ Readout Bus (216 units) Sep '01 done End Prototyping: New Design: **Dec '02** done Production: Jan '03 – Jul '03 Oct '03 – Mar '04 **□ RCU** (216 boards) Jun '03 Mar '04 End Prototyping: • RCU-I (PLDa-based RCU) Mar '02 done • RCU-II delivery Sep '02 done (Jan '03) • Final design Feb '03 Sep '03 Production: Jul '03 – Oct '03 **Apr '04 – Jul '04** Nov '03 – **May '04** Aug '04 – Mar '05 Test:

remaining work

PASA

Production

Manufacturing of full-sheet wafer (AMS): Jun-Aug '03
 (re-submission 27 May '03)

Delivery of ER samples:
Aug '03 (20 chips)

Sep '03 (500 chips)

Test of ER samples (Heidelberg - Darmstadt - CERN)
 Sep '03

■ Series Lot Production (25 + 10 wafers) Oct '03 – Jan '04

■ Series Production Test (4 lots of ~ 10,000 chips) Feb '04 – Jul '04

(3mm cont.)

☐ Automatic Test Equipment (ATE)

by Aug '03

Design and construction of ATE (Darmstadt): well advanced

• Validation of ATE (Darmstadt – Heidelberg): in progress

■ Test Software (Darmstadt): in progress

remaining work

ALTRO

☐ Test Equipment

Design and construction of ATE (Lund):

by end of June (Pick&Place tool missing)

Validation of ATE (Lund):

• Software of ATE (Lund):

in progress

done

☐ Mass Production Test (Lund)

Jul-Dec '03 (3 mm conting.)

remaining work

FEC

- ☐ Irradiation tests
 - TID, SEL and SEU effects studies completed for all components
 - Measurement of the critical charge for FPGAs to be done by Aug '03 (Uppsala, PSI)
- \square New small-series production (15 + 35 boards) (Lund CERN)
 - 15 FEC loaded with all components but PASAs Jun '03
 - 15 FEC fully loaded Sep-Oct '03
- ☐ Call for Tenders (Lund) Jul Sep '03
- Mass Production (Lund) Nov '03 Aug '04
- Mass Production Tests (Frankfurt) Apr '04 Nov '04

-		
ramai	nin	ork
remai		\mathbf{O}

FEC

		•
Automatic '	Cost H	auunmant
Automatic		uunninent
		9 27 2 77 77 7

Desi	gn and construction of ATE (Frankfurt):	by Oct '03
------------------------	---	------------

- Preliminary Version of Test Software (Frankfurt):
 by Oct '03
- Validation of ATE (Frankfurt):by Dec '03

RCU

\Box S	pecification Do	ocument for the	final design	(Bergen-CERN) done
					,

- ☐ Engineering design of RCU (Bergen Heidelberg) Jun '03
- ☐ Firmware (Bergen CERN Heidelberg) Sep '03
- □ Prototype ready for test Sep '03
- Qualification of final design (Bergen CERN) Oct '03 Mar '04
- ☐ Production (CERN) Apr Jul '04
- ☐ Mass Production test (CERN) Aug '04 Mar '05

28 January 2003 Luciano Musa

FEE Planning Update

