The ALTRO Chip: A 16-Channel A/D Converter and Digital Processor for Gas Detectors

R. Esteve Bosch, A. Jiménez de Parga, B. Mota, and L. Musa

***Abstract*—The ALTRO (ALICE TPC Read Out) chip is a mixed-signal integrated circuit designed to be one of the building blocks of the readout electronics for gas detectors. Originally conceived and optimized for the time projection chamber (TPC) of the ALICE experiment at the CERN LHC, its architecture and programmability make it suitable for the readout of a wider class of detectors. In one single chip, the analog signals from 16 channels are digitised, processed, compressed, and stored in a multi-acquisition memory. The analog-to-digital converters embedded in the chip have a 10-bit dynamic range and a maximum sampling rate in the range of 20–. After digitization, a pipelined Data Processor is able to remove from the input signal a wide range of perturbations, related to the nonideal behavior of the detector, temperature variation of the electronics, environmental noise, etc. Moreover, the Data Processor is able to suppress the pulse tail within 1 μs after the peak with 1‰ accuracy, thus narrowing the pulses to improve their identification. The signal is then compressed by removing all data below a programmable threshold, except for a specified number of pre- and post-samples around each peak. This produces nonzero data packets. Eventually, each data packet is marked with its time stamp and size – so that the original data can be reconstructed afterwards – and stored in the multi-acquisition memory that has a readout bandwidth of 300 Mbyte/s. This paper addresses the algorithms of the implemented digital functions and the performance of the ALTRO chip.**

***Index Terms*—Analog-digital conversion, CMOS mixed analog-digital integrated circuit, data processing, digital filter, gas detector.**

I. INTRODUCTION

THE ALICE [1] (A Large Ion Collider Experiment) at the CERN LHC, which is currently in preparation for initial operation in 2007, is dedicated to the study of the collisions of several species of ions. The experimental apparatus to study the high number of particles (up to 3×10^4) produced in each collision is a multicomponent detector. The ALICE time projection chamber [2] (TPC) plays a central role in the detector, and it provides a three-dimensional reconstruction of the particle trajectories. The ALICE TPC consists of a cylindrical gas volume of about 90 m^3 under a uniform electrostatic field. Charged particles traversing the TPC volume ionize the gas along their path, liberating electrons that drift toward the chamber endplates. At the endplates, as sketched in Fig. 1, conventional multiwire proportional chambers (MWPCs) provide the charge amplification and readout by means of a cathode plane segmented in about 6×10^5 pads. For every pad, the charge is integrated and subsequently shaped by a shaping amplifier. The pulse height spectrum over the TPC maximal drift length (88 μs) is converted in digital data, compressed, and stored in a memory. In an MWPC, the signal released on the pads is characterized by a fast rise time (less than 1 ns) and a long tail. The shape of the signal tail is rather complex and depends on the details of the chamber and pad geometry. This tail can cause pile-up effects in high rate environments, setting the main limitation to the maximum track density at which a MWPC can be exposed. Therefore, an accurate tail cancellation and baseline restoration of the detector signal are fundamental requirements for the front-end electronics design, especially if data compression has to be performed on-line before shipping the data off-detector. The readout electronics for the ALICE TPC has to satisfy many other constraints while meeting the required performance specifications. Mainly, it needs to fit into the overall detector structure and, in particular, into the available space, which is inaccessible while the experiment is running. This has important consequences in terms of integration density, long-term reliability, and power. In particular, the requirements for electronics with minimal dimensions, power, and cost drive the integration density as high as possible. Although the ALICE TPC front-end electronics will be exposed to a low radiation load (300 rad $\oplus 10^{11}$ neutrons/cm^2 over 10 years), some special care should be taken to protect the system against severe errors caused by single event upset (SEU) effects.

The unavailability of commercial components that integrate a high number of A/D converters and the need to combine them with a custom data processor have driven the design of the ALTRO (ALICE TPC Read Out) chip. ALTRO integrates 16 channels, each of them consisting of a 10-bit ADC, a pipelined Data Processor, and a multi-acquisition data memory. Fig. 2 shows a simplified block diagram of the chip.

Although originally designed and optimized for a TPC, the ALTRO chip finds application in other types of detectors. For example, ALICE is currently considering to use the ALTRO chip for the readout of the PHOton Spectrometer (PHOS), which is an electromagnetic calorimeter based on lead-tungstate crystals coupled with avalanche pin diodes, and the Forward Multiplicity Detector (FMD), which is based on silicon strips.

Manuscript received December 2, 2002; revised July 2, 2002.

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Digital Object Identifier 10.1109/TNS.2003.820629

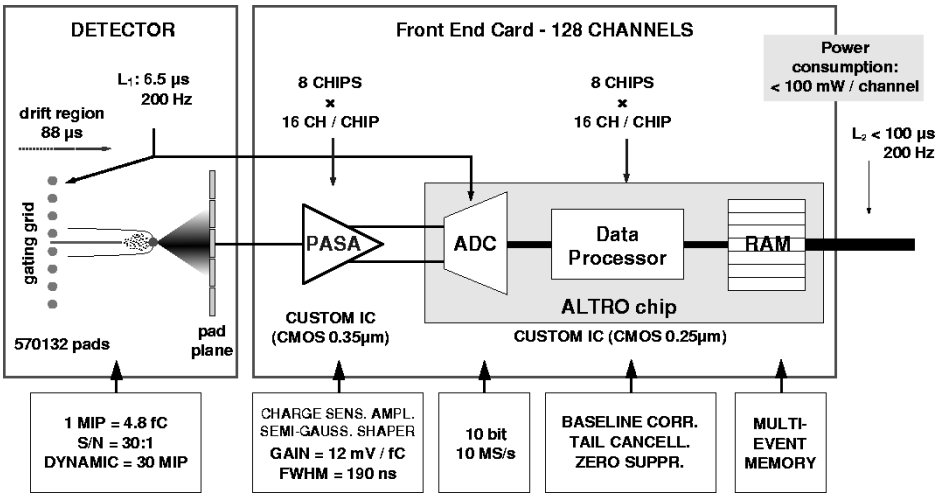

Fig. 1. ALICE TPC front-end electronics and requirements.

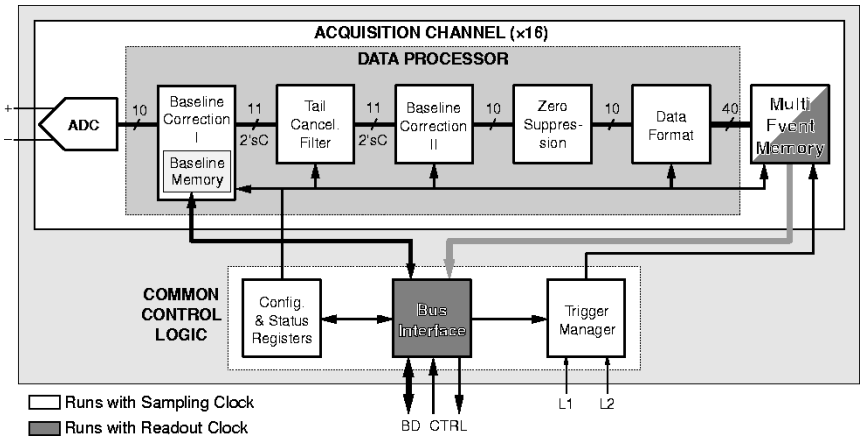

Fig. 2. ALTRO chip block diagram.

II. Circuit Description

A. Overview

ALTRO is a mixed-signal custom integrated circuit containing 16 channels operating concurrently and continuously on the analog signals coming from 16 independent inputs.

It is designed to process a train of pulses sitting on a common baseline. When a Level-1 (L1) trigger is received, a predefined number of samples is processed and temporarily stored in a data memory (*acquisition*). This *acquisition* is frozen if a Level-2 (L2) trigger is received; otherwise, it is overwritten by the next acquisition.

The Data Processor implements algorithms in several stages of circuitry to condition the signal. The first stage is the Baseline Correction I. Its main task is to prepare the signal for the tail cancellation by removing low-frequency perturbations and systematic effects. The next processing block is a Tail Cancellation Filter. The filter is able to suppress the tail of the pulses within 1 μs after the peak, with the accuracy of 1 LSB. As the filter coefficients for each channel are fully programmable and re-configurable, the circuit is able to cancel a wide range of signal tail shapes. This also allows maintaining a constant quality of the output signal regardless of aging effects on the detector and/or channel-to-channel fluctuations. The subsequent processing block, the Baseline Correction II, applies a baseline correction scheme based on a moving average filter. This scheme removes nonsystematic perturbations of the baseline that are superimposed to the signal. At the output of this block, the signal baseline is constant with an accuracy of 1 LSB. Such accuracy allows an efficient signal compression using a Zero-Suppression procedure, which discards all data below a programmable threshold. In the data format, each data packet is formatted with its time stamp and size information in a way that reconstruction is possible afterward. The output of the Data Processor is sent to a 5 Kbyte data memory able to store up to eight *acquisitions*.

Data can be read out from the chip at a maximum speed of 60 MHz through a 40-bit wide bus, yielding a total bandwidth of 300 Mbyte/s. The readout speed and the ADC sampling frequency are independent.

A more detailed description of these blocks is given hereafter.

B. Analog-to-Digital Conversion

The analog to digital conversion is based on the ST Microelectronics TSA1001 [3], a CMOS 10-bit pipelined ADC. The block diagram of this ADC is presented in Fig. 3. The conversion pipeline consists of nine stages, the first eight with a resolution of 1.5 bits and the last one with a resolution of 1 bit.

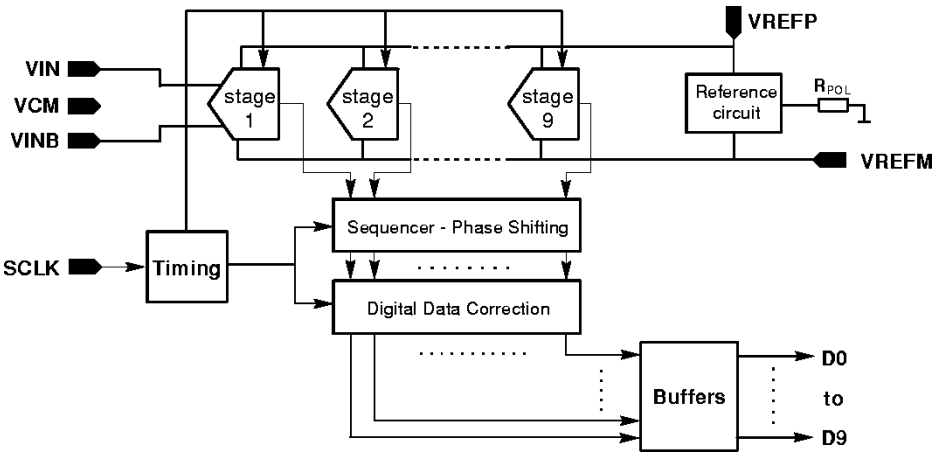

Fig. 3. Block diagram of the ALTRO ADC.

Within each pipeline stage the conversion is performed on both the rising and falling edges of the clock. A phase correction circuit aligns the output of the different stages to build a parallel data word, which is fed to a digital correction circuit that removes the redundant bits and provides a clean 10-bit word. The overall conversion has a latency of 5.5 clock cycles.

The internal construction of the ADC is fully differential, and it allows up to 2 V differential swing. It follows that one LSB corresponds to 2 mV. The range of the input signals is defined by three voltages: the common mode (V_{CM}) and the top and bottom references (V_{REFP} and V_{REFM}). These reference voltages allow interfacing of the ADC to a wide variety of devices.

For the particular case of the ALICE TPC, the connection of the ALTRO ADC to the pre-amplifier/shaping amplifier (PASA) is as shown in Fig. 4.

A polarization current, provided for each channel by an internal resistor, defines the ADC bandwidth and power consumption. The polarization resistor is divided in multiple taps such that only one metal layer has to be changed, in order to optimize the power consumption to the required bandwidth. To the purpose of measuring the resolution and power consumption of the ADC as function of the polarization current, one ALTRO prototype was modified by means of a Focused Ion Beam machine. The modification consisted in connecting one of the ADC channels to an external polarization resistor. The measurements results are shown in Fig. 5.

Two versions of the ALTRO chip have been produced with maximum rates of 25 MSPS and 40 MSPS and power consumption of 12.5 mW and 43 mW, respectively.

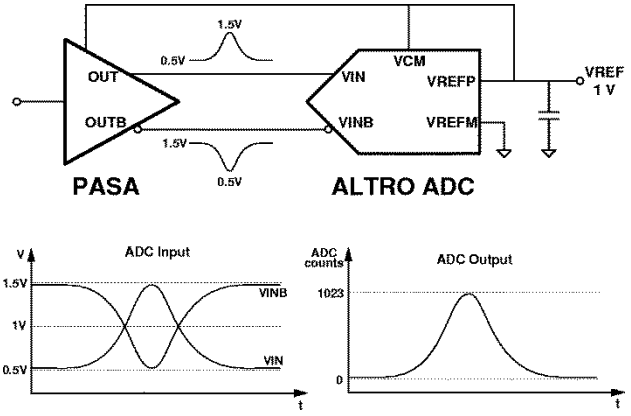

Fig. 4. Connection of the ALTRO ADC to the PASA.

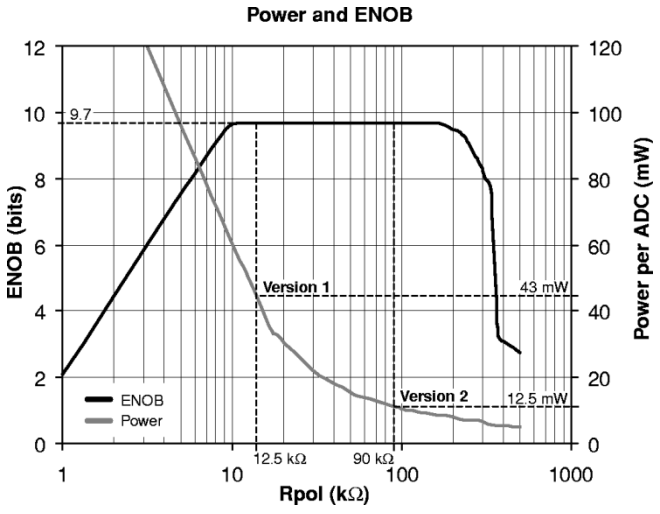

Fig. 5. Effective number of bits (ENOB) and power consumption as a function of the polarization resistor, for a sampling frequency of 10 MSPS.

C. Baseline Correction I

This first stage is able to perform several operations on the input signal: channel-to-channel gain equalization, nonlinearity correction, baseline drift compensation, offset removal (fpd), and the subtraction of systematic spurious signals using a pattern stored in a dedicated memory. It is also possible to change the polarity of the input signal. This stage is composed of two main units:

- A self-calibration circuit. It tracks continuously the signal outside the acquisition time, computing its cumulative average (vpd). Upon arrival of a first level trigger, its last value is used as self-calibrated offset to be subtracted to all the samples during the acquisition time. This allows correcting for slow baseline perturbations such as temperature drifts.
- A pattern memory (Baseline Memory, 1 k $\times$ 10 bits). On every *acquisition*, the values stored in a memory can be

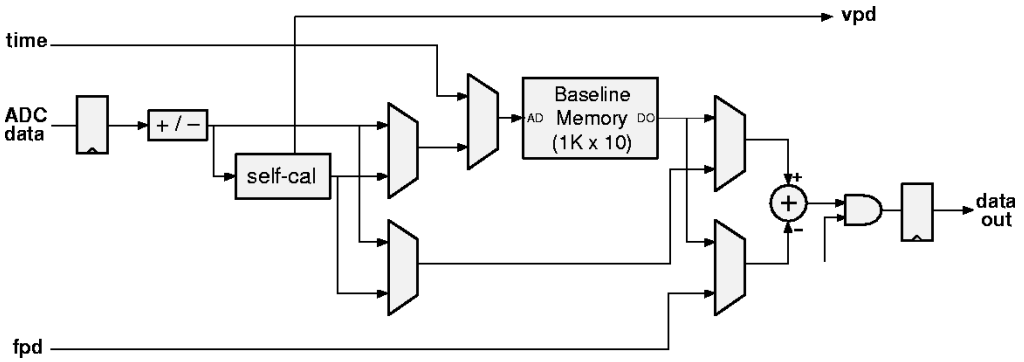

Fig. 6. Baseline Correction I block diagram.

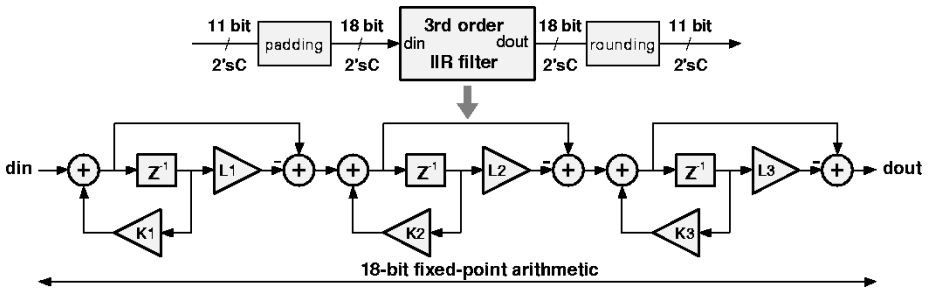

Fig. 7. Tail Cancellation Filter block diagram.

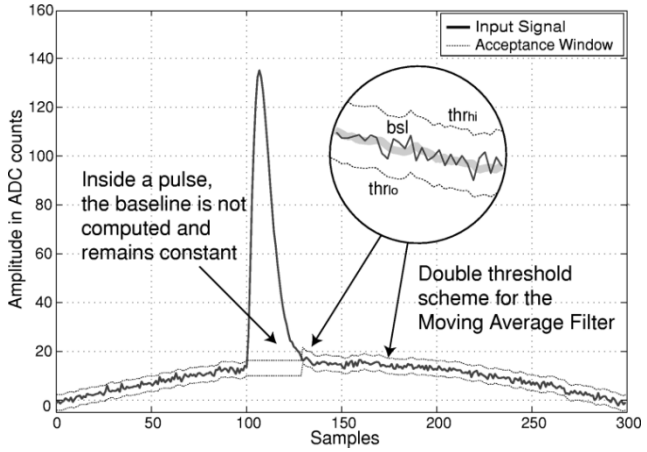

Fig. 8. Baseline Correction II operation principle.

subtracted from the input signal, thus removing systematic perturbations. Alternatively, the pattern memory can be used as a lookup table (LUT) to perform dynamic conversion or to equalize the response across different channels. Also, for test purposes, this memory can inject a pattern in the processing chain to allow the testing of all the logic downstream without the need of an external analog signal.

When the memory is used as an LUT to perform dynamic conversion, it is accessed continuously, inside and outside the *acquisition*. For applications requiring low power, LUT operation can be stopped outside *acquisition* if the power-save feature is enabled. In this mode, the output of this stage is gated, driving 0's to the subsequent stages.

A complete block of the Baseline Correction I is depicted in Fig. 6.

D. Tail Cancellation Filter

In order to minimize pile-up effects, the ALTRO chip incorporates a digital filter, whose functions are described in detail in [4], for the cancellation of the signal tail.

As it is shown in Fig. 7, the filter is an 18-bit, fixed-point, 3rd order IIR digital filter acting in the time domain. It is composed of 3 first-order filters in cascade. The input and output of the filter are in 11-bit 2's complement format. The operation of the filter is flexible by changing six fully programmable coefficients, K1, K2, K3, L1, L2, and L3.

E. Baseline Correction II

This unit performs a second baseline correction, removing signal perturbations created by nonsystematic effects, e.g., pickup noise.

The principle of operation of this unit is depicted in Fig. 8. Given a value of the baseline (bsl), an acceptance window is defined by two thresholds above ($\mathrm{thr_{hi}}$) and below it ($\mathrm{thr_{lo}}$). The baseline is updated based on the average of the last eight samples that fall inside that window. When there is a fast variation in the signal, like a pulse, the samples are out of the acceptance window and therefore excluded from the baseline calculation. The value of each sample is corrected using the last value calculated by the moving average filter. At this point, the signal is sitting on zero, and anything below this value will be clipped to zero. If there were effects to be observed below the baseline, a discretionary offset can be added.

As depicted in Fig. 9, the Baseline Correction II unit is based on two main blocks, a double threshold scheme and a moving average filter. The moving average filter is based on an 8-tap 11-bit FIR structure with an accumulator. The control logic allows a selectable number of pre-samples and post-samples

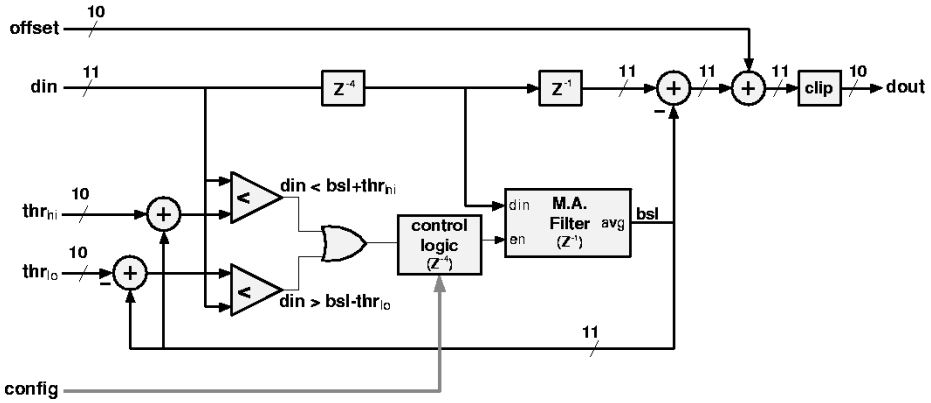

Fig. 9. Baseline Correction II block diagram.

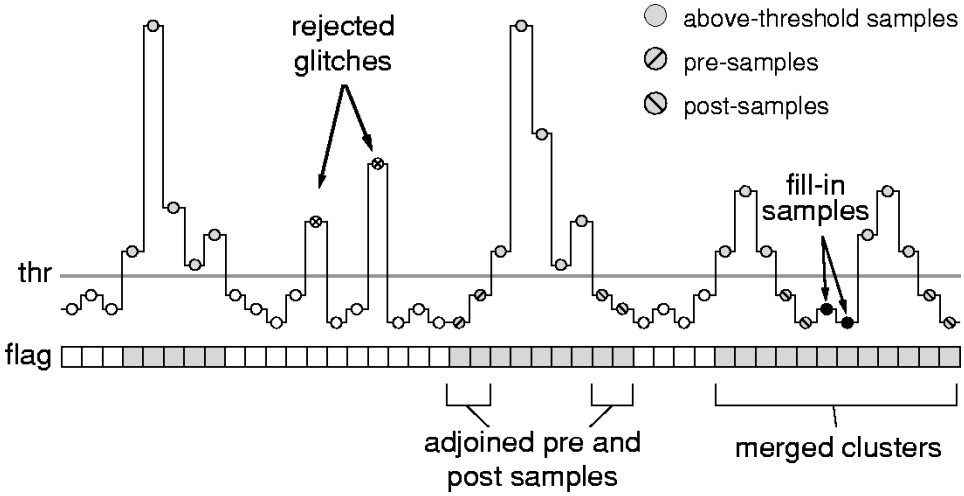

Fig. 10. Zero Suppression scheme.

around each pulse to be excluded from the baseline calculation. In addition, this logic forces the quick convergence of the baseline at start-up before applying the exclusion criterion.

F. Zero Suppression

Once the perturbations of the signal have been removed, it is safe to apply a fixed threshold (see Fig. 10). The Zero Suppression mechanism allows compressing the data stream by removing samples that are under a given threshold. If the flatness of the baseline is guaranteed, the threshold can be as low as the peak noise level, thus maximizing the amount of pulses detected and stored.

This unit also implements other additional features, described hereafter.

- Glitch filter. This circuit checks for a consecutive number of samples above the threshold, confirming the existence of a real pulse, and thus reducing the impulsive noise sensitivity.
- Extraction features. In order to keep enough information for further extraction, the complete pulse shape must be recorded. Therefore, the possibility to record pre and post-samples is provided.
- Cluster merger. As it is described in next section, two extra words are needed for every new set of data. Therefore, the merging of two consecutive sets that are closer than three samples is performed.

G. Data Format

This block performs two operations: cluster labeling and data packing.

Cluster labeling. Each identified and isolated set of data (cluster) must be tagged with two words, its time stamp and its size, in order to be able to reconstruct the *acquisition* afterward. The time information added to each set during the formatting phase corresponds to the time-stamp of the last sample in the set. The size represents the number of 10-bit words in the set, including the data samples, time stamp, and itself.

Data packing. Since readout is done through a 40-bit-wide bus, the 10-bit words must be formatted into 40-bit words. At the end of the *acquisition*, stuffing is provided if needed to build a complete 40-bit word. Then, a special 40-bit trailer word is appended. This word contains essential information to unpack the formatted data: the total number of 10-bit words in the packet and the channel and chip addresses. The latter represents a sort of geographical address and is used to identify unambiguously the channel to which the data packet corresponds. The resulting data block has a back-linked structure; i.e., the decoding must be done starting from the end.

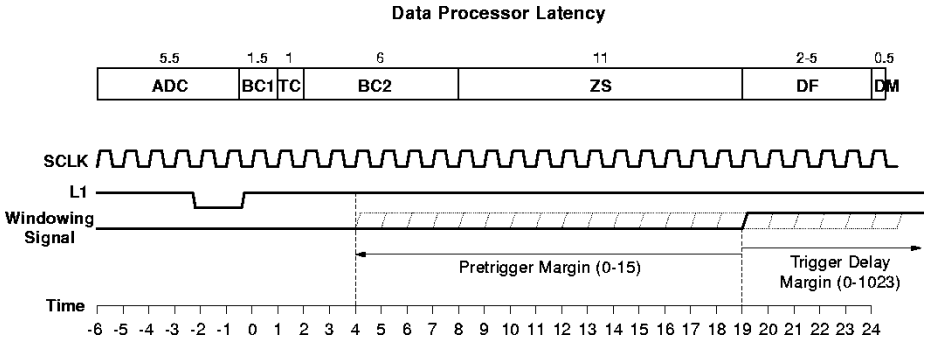

Fig. 11. Trigger and *acquisition* control. (BC1, BC2, TC, ZS, DF, and DM stand for Baseline Correction I and II, Tail Cancellation Filter, Zero Suppression, Data Format, and Data Memory, respectively.)

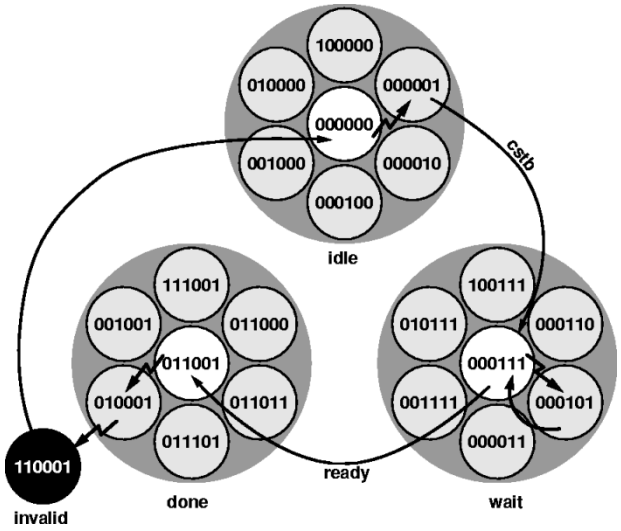

Fig. 12. The Hamming-based protection scheme for state machines.

H. Multi-Event Memory

The ALTRO data memory (1024×40 bits) is partitioned in either four or eight buffers. The size of the memory allows storing four complete 1000-sample *acquisitions* with nonzero-suppressed data. If the Data Processor is configured to process less than 512 samples, the 8-buffer partitioning can be used.

Due to the 10-to-40-bit data formatting done in the previous stage, the writing of the memory is performed at a very low rate; one word every four sampling clock cycles, at most. The readout, on the other side, is a fast synchronous block transfer running on the faster readout clock.

A central memory manager handles the assignment and disposal of buffers and controls the readout of the memories.

The way the data blocks are stored and retrieved from the memory is completely transparent to the user. Each data block will be stored in the next available memory buffer. When all the memory buffers are occupied, a full signal is generated to ignore further triggers.

In order to reduce the noise and the dead time, the basic principle of operation is that all bus activity should be stopped during the acquisition time. For this reason, the data memory manager interrupts the readout when a trigger is received and resumes when the *acquisition* is finished.

I. Trigger Manager

The purpose of the Trigger Manager is to generate a windowing signal that controls the writing of the data to the memory. The Data Format block uses this signal to enable the writing and to finalize the data block. A proper alignment of this signal is generated based on the parameters described hereafter.

The Trigger Manager does not take into account the latency of the ADC, the first sample of the *acquisition* being the one output by the ADC following the trigger pulse (see Fig. 11). The latency of the Data Processor is 18 clock cycles. This allows taking a selectable number of up to 15 pre-trigger samples. The chip also implements a trigger delay feature that allows adapting the acquisition window to the acceptance of the detector.

J. Protection of Finite State Machines Against SEU

For the ALTRO chip, errors induced by SEU can be classified according to three severity levels.

- Data-path errors. These are the least severe errors. The bit flip occurs in a circuit that is periodically overwritten with new incoming data: the ADC, the Data Processor, or the data memory. The effect of the error remains within one event.
- Configuration space errors. The bit flip occurs in the configuration registers or the pedestal memory. This change will affect the behavior of the Data Processor for many events, until the configuration is rewritten.
- Control errors. These are the most severe errors. The bit flip occurs in a state machine that controls the access to the bus or the allocation of the data memory. In the first case, the error can induce an electrical conflict in the bus and damage the chip transceivers, whereas in the second case, it can cause serious data loss or misalignment. To avoid these effects, some state machines are protected with an error-correcting circuit.

At the particle fluency estimated for the ALICE TPC, data-path and configuration space errors result in a bit error rate (BER) below $10^{-15}/\mathrm{s}$. For this reason, there is no special mechanism to protect the ADC, the data processing circuit, and the configuration registers. Taking into account the fact that the control state machines of the chip make up less than 1% of the logic, the probability of having an SEU in these circuits is very small. But it is also very small the overhead of adding the error

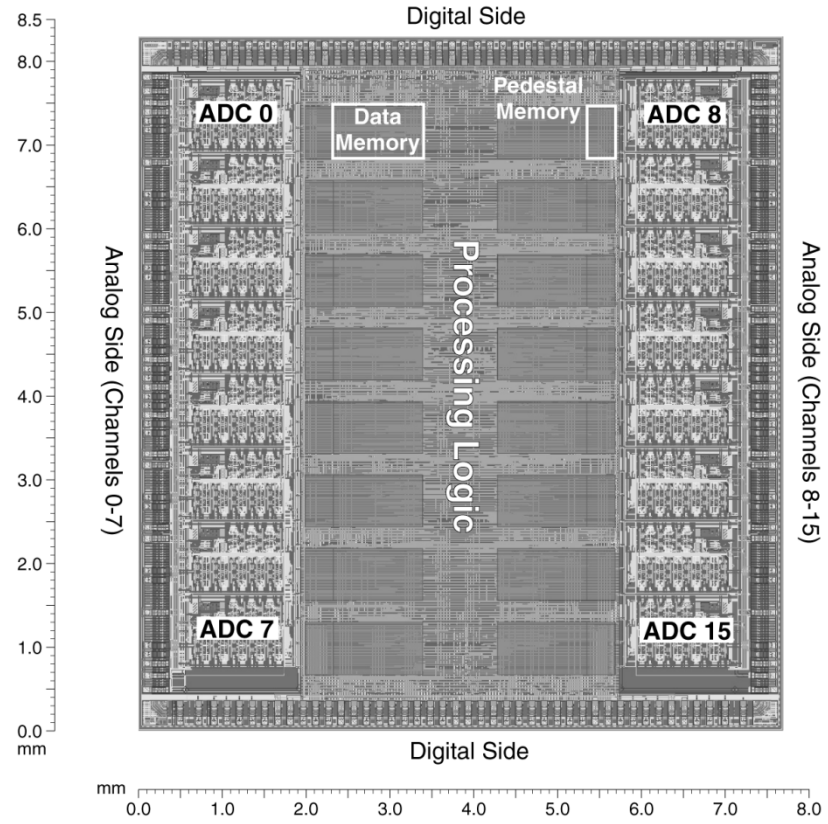

Fig. 13. ALTRO chip layout.

correction circuit, while it makes the control machines almost invulnerable to errors.

The design of the error-correcting state machines uses Hamming encoding to code the states. According to [5], a code that has single-error correcting and double-error detecting capabilities must verify: $2^k \geq m + k + 1$, where m is the number of digits actually coding the state and k is the number of check digits. The Hamming distance is defined as the number of bits changing between two given codes.

In a Hamming-protected state machine, we define three types of states.

- Coding states. The codes assigned to these states are considered free of error. The Hamming distance between them is three.
- Derived states. These states are considered erroneous but recoverable. Around each coding state, there is a cloud of states with a Hamming distance of one, called derived states. A group of derived states is an image of its related coding state, producing exactly the same outputs.
- Invalid states. These states are also considered erroneous, and the Hamming distance from a coding state is two. These states are not associated with a coding state, so the error is detected but cannot be corrected.

Fig. 12 shows the working principle. The spiky arrows represent bit-flips caused by an SEU effect. The smooth arrows represent a natural state change following a clock edge. If, while being in a coding state, a bit flip happens, the machine is forced into a derived state. The recovery action takes place in the next clock cycle. If a change of state is required according to the value of the inputs, the machine will jump directly to the next coding state, maintaining the natural course of action. If no state change is required, the machine will jump back to the original coding state. If a double bit-flip occurs, the circuit may jump to an invalid state. Since this state is not associated to any coding

TABLE I
ALTRO PHYSICAL CHARACTERISTICS

Process	ST HCMOS-7 (0.25 μm)
Area	64 mm^2
Dimensions	7.70 × 8.35 mm^2
Transistors	6 Million
Embedded Memory	800-Kbit
Supply Voltage	2.5V
Package	TQFP-176

TABLE II
ALTRO KEY PERFORMANCE FIGURES

Power Consumption	320mW [1]
Max. Readout Bandwidth	300 MB/s [2]
ADC Resolution	10 bits
ENOB	9.7 bits [1,3]
N_{rms} (rms Noise)	0.35 LSB rms
DNL	< 0.2 LSB rms. [1,3]
INL	< 0.8 LSB abs. [1,3]
SFDR	78 dB [1,3]
Crosstalk	0.05 LSB rms [1,4]

[1] f_s=10MHz, R_{pol}=90kΩ, internal; [2] f_{RDO}=60MHz; [3] f_{in}=960kHz, 1V_{pp}; [4] aggressor: f_{in} = 960 kHz, 1 V_{pp}; victim: closed to 100 Ω

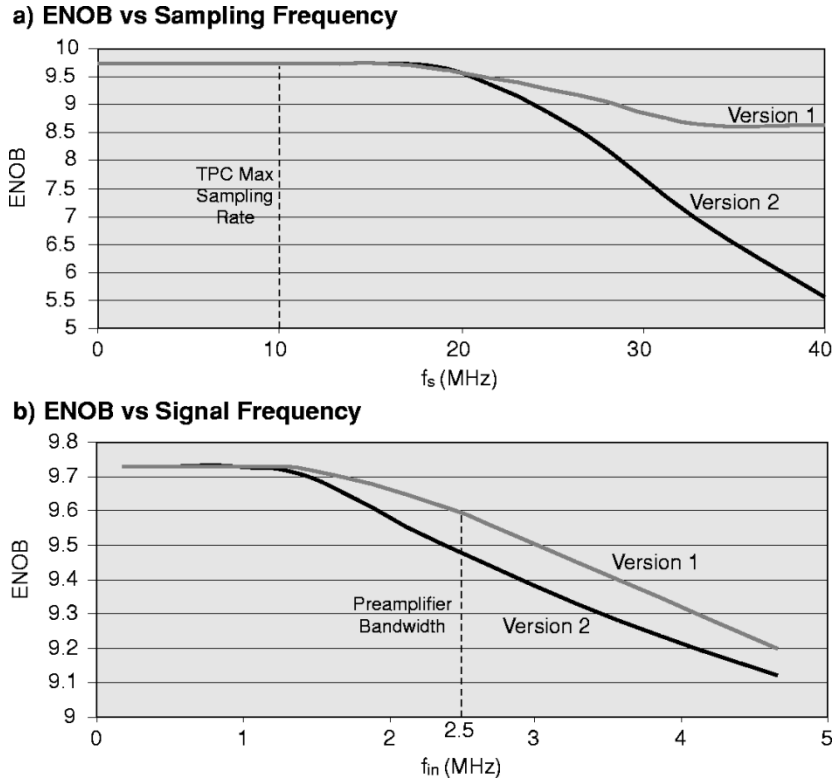

Fig. 14. Performance comparison of the two existing versions of the ALTRO.

state, the only possible solution is aborting the course of action and returning to the idle state. Single and double bit-flips are detected and reported in a Status register.

III. Physical Implementation

The ALTRO chip is manufactured in the ST Microelectronics CMOS 0.25 μm (HCMOS-7) technology with six metal and three polysilicon layers. The integration of the ADC imposes certain restrictions to the layout and the pin-out of the chip in order to guarantee a good performance in terms of noise and conversion reliability. The 16 ADCs are arranged in two octal-ADC macros. The pedestal memories are placed close to the macros on the left and right side, as shown in Fig. 13. The data memories are placed toward the center of the chip, distant from the ADCs macros. The placement of the memories reflects the regular structure of the 16 concurrent processing channels. The processing logic is distributed in the remaining space.

To reduce the effect of digital noise on the ADC, the following strategy was applied during the layout phase. As 95% of the logic works on the sampling clock, the phase of the clock signal distributed to all the flip-flops can be adjusted such that the switching of all digital nodes occurs outside the aperture time of the ADC. Each ADC block contains a passive clock tree balanced with the accuracy of 1 ps.

From the input pad, the clock signal is first split in two branches. One is manually routed to the two ADC blocks to ensure a skew of less than 5 ps. The second one is distributed to all the processing logic. Given the greater depth of the digital clock tree, the clock edge reaches first the ADCs and then the digital logic. A margin of some 600 ps, considering the worst-case figure for temperature and process variations, was taken. As the aperture time of the ADC is 5 ps, by the time the digital switching noise starts, the sampling is already done.

Additionally, a P^+ substrate tied down guard ring was inserted around each ADC and between the ADCs and the digital circuit. This guard ring creates a low-impedance path between the substrate and ground, thus reducing surface noise between adjacent ADCs and digital noise propagated through the substrate.

The location of the digital pads was selected based on noise and ground plane considerations, but also taking into account the routing requirements of the PCB. All the digital pads are placed on the top and bottom sides, while the analog pads are sitting on the left and right sides. In order to prevent noise propagating through the supply or the ground, the analog and digital power supplies and grounds are separated. The output drivers are based on the CMOS 2.5 V family.

The key figures of the layout are depicted in Table I.

IV. Performance

According to the requirements of the ALICE TPC, 48.000 chips have been fabricated, with a production yield of 84%. A set of tests was implemented so as to assess the performance of the chip. Effective number of bits (ENOB), differential nonlinearity (DNL), and integral nonlinearity (INL) aimed at proving the correct ADC behavior. The frequency spectrum showed the nature of the noise and the spurious-free dynamic range (SFDR). A set of digital tests exercised every block of the Data Processor

and the common logic at different sampling and readout frequencies. More details on these tests are presented in [6] and summarized in Table II.

Two different versions of the ALTRO chip have been tested. Version 1 has a polarization resistor value of 12.5 $\mathrm{k}\Omega$, which gives the maximum performance of the ADC. Version 2 has a resistor value of 90 $\mathrm{k}\Omega$, optimized for the ALICE TPC application. A comparison of the performance of each version is presented in Fig. 14. Fig. 14(a) shows the ENOB of each version versus the sampling frequency. The version with the higher polarization current keeps above 8.5 bits up to 40 MSPS. Fig. 14(b) depicts the variation of the ENOB as a function of the frequency of the input signal (full-scale sine wave). The slope is due to the jitter of the quartz used for the measurements, which becomes more relevant as frequency increases. The offset between the two curves is caused by the difference in polarization current; a lower current provokes more harmonic distortion that degrades the ENOB.

The final test was to inject a real analog signal using a synthesized waveform generator to evaluate the performance of the overall processing chain. The input signal was artificially generated, using real measured pulses combined according to the expected distribution for the amplitude and arrival time of the pulses in the ALICE TPC. Pile-up appears at this point when a pulse sits on the tail of a previous pulse.

Several disturbing effects were added on purpose, as shown in Fig. 15(a). These perturbations are magnified replicas of those observed in the operation of previous large-size TPCs: systematic effects (first oscillation), nonsystematic effects (second bump), and slow baseline drifts. Fig. 15(b) depicts the signal after the Baseline Correction I unit. The systematic effect and the offset are removed by subtracting the content of the baseline memory. However, the presence of pile-up and nonsystematic effects prevents performing a zero suppression based on a fixed threshold at this stage. The tail cancellation filter can remove pile-up effects by filtering the cluster tails, as shown in Fig. 15(c). This figure also shows the acceptance window used by the Baseline Correction II. Anything falling within this window is averaged to calculate the next baseline value, which is then subtracted from the signal. Fig. 15(d) shows the output of this block, which provides a signal sitting on a flat baseline, which is now suitable for a zero suppression based on a fixed threshold.

Besides the protection of the finite state machines against the SEU, no special layout technique was adopted to harden the design at the device or gate level.

The ALTRO chip was tested under radiation, at the Centre de Recherches du Cyclotron (CRC), Louvain-la-Neuve, Belgium, with 60 MeV protons. Several samples of the ALTRO chip were irradiated up to 300 Krad and $10^{12}\ \mathrm{protons/cm^2}$. During the irradiation, the number of SEU in memories, registers, and state machines were monitored, as well as the current consumption. Although several SEUs were detected in the Hamming encoded state machines, none of them led to any failure. Moreover, no single event latchup effects were observed in any of the irradiated samples. The main figures of the test are reported in Table III.

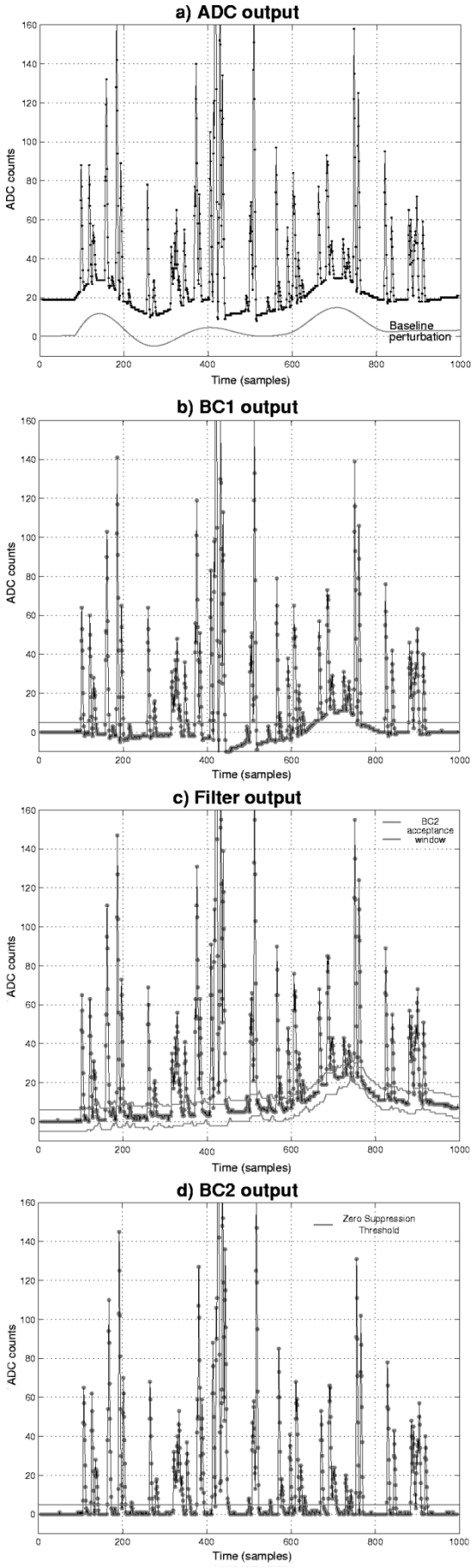

Fig. 15. Signal at the different stages of the Data Processor.

TABLE III
SUMMARY OF THE RADIATION TEST OF THE ALTRO CHIP

Beam Energy	60MeV
Fluency	$2.23 \cdot 10^{12} cm^{-2}$
Dose	300Krad
Error Cross Section per memory bit	$5.5 \cdot 10^{-14} cm^2$
Error Cross Section per flip-flop	$7.7 \cdot 10^{-14} cm^2$
Power consumption increase	38% [1]

[1] After annealing at room temperature for three weeks, the power consumption returned to normal

A sizeable number of ALTRO chips totaling 1024 channels have been characterized in a test that incorporates a prototype of the ALICE TPC as well as many other components of the final setup. The tests show that the system meets all ALICE TPC design requirements. The detection of events is produced by large showers of cosmic rays, allowed to test the performance of the tail cancellation and baseline correction circuits. Indeed, a few events were characterized by the same signal occupancy (about 50%) predicted for the relativistic collisions of heavy ions in ALICE. These measurements show that the ALTRO chip performs a good cancellation of the signal tail (0.1% of the signal amplitude within 1 μs) and the restoration of the baseline (within 1 ADC count), even for very high signal occupancy.

V. CONCLUSION

The ALTRO chip, developed for the ALICE experiment at the CERN LHC, responds to the demands of the new HEP experiments to embed in a single chip the circuit to digitize, process, compress, and store the information of a high number of channels. The chip, which is implemented in a 0.25 μm CMOS technology, has an area of 64 mm^2 and a power consumption of 320 mW when the 16 channels are acquiring at a 10 MHz rate. The measurements show a resolution better than 9.5 ENOB on all channels and a channel-to-channel cross talk below -65 dB. Although optimized for the ALICE TPC requirements, its architecture and the programmability of its processing blocks make it suitable for a wider class of applications. At the architectural level, the detector-amplified analog signals are immediately digitised with an ADC per channel, which is a novelty in the domain of readout electronics for large-size TPCs. ALTRO is one of the first successful examples of a chip that incorporates 16 high-speed (20 to 40 MSPS) high-resolution (10-bit) A/D converters with a complex digital circuit. The performance of the ALTRO shows that the techniques adopted, both at the system and layout level, to reduce the effect of digital noise on the ADC resolution are successful. The ALTRO chip integrates a set of innovative algorithms implemented in a form of a digital processor able to condition detector signals to an accuracy of the per mile level.

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