ALTRO Production Acceptance Test

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1 Introduction

This document mainly deals with the system and procedures employed for the mass production test of the ALTRO chip. The purpose of the production acceptance tests is to sort out and qualify the ALTRO chips that comply with the *Alice TPC Readout Chip Technical Specifications* [1].

In testing a large quantity of chips it is of primary importance to minimize the testing per chip, to produce results which are clear and precise, and minimise the risk of human errors and damages to the chips under test. These requirements have driven the design of the test system for the ALTRO chip.

The architecture and the main components of the ALICE TPC front-end electronics are described in [2]. A detailed description of the ALTRO chip can be found in [1]. As far as the test is concerned, we can consider the ALTRO chip as consisting of two main blocks: the analogue part, comprising 16 analogue-to-digital converters (ADCs), and the digital part, containing the Data Processor and the Multi-Acquisition Memory for 16 channels. The functions of the analogue part can be tested independently by operating the ALTRO chip in *Test Mode*. The functions of the digital part can be tested either by a direct write/read access, e.g. the *Pedestal Memories* and all *Configuration and Status Registers* (CSRs), or by using the *Pedestal Memories* to generate a data pattern which is injected in the *Data Processor*, and reading the corresponding results from the *Data Memories*.

Section 2 describes the test system, section 3 deals with the test algorithms, and section 4 focuses on the control, readout and analysis software. At last, section 5 describes the precautions adopted in handling the chips, and section 6 presents the results obtained in the mass production tests of the ALTRO chips for the ALICE TPC.

2 Test System

Figures 1 and 2 show respectively a schematic diagram and a photograph of the system for the mass test of the ALTRO chip. The main components of the test system are: the *Chip Tester*, the *Robot*, a *Control PC*, a *Database PC*, an oven and a pen-plotter.

The *Chip Tester* is the circuit that hosts the chip under test, stimulates all input signals and measures its response by acquiring all output signals. The *Chip Tester* operates under the control of a LabWindows test program running in a PC (*Control PC*) operating under Windows 98. The input signals for the ADCs are generated by a commercial (HP 8165) sine-wave generator and distributed by the *Chip Tester* to the ALTRO chip.

The trays containing the chips to be tested and a number of empty trays are disposed on the test bench by the (human) operator. From then on, the handling of the chips is completely operated by the *Robot*: it picks up the chips from the source tray, places them into the *Chip Tester* and, according to the test results, it separates functional from not working chips, by disposing them into different destination trays. The robot is equipped with a *Controller* that steers all motions of its arm. The *Controller* receives the high level commands, e.g. the coordinates of the next chip to be tested, from the same PC that controls the *Chip Tester.*

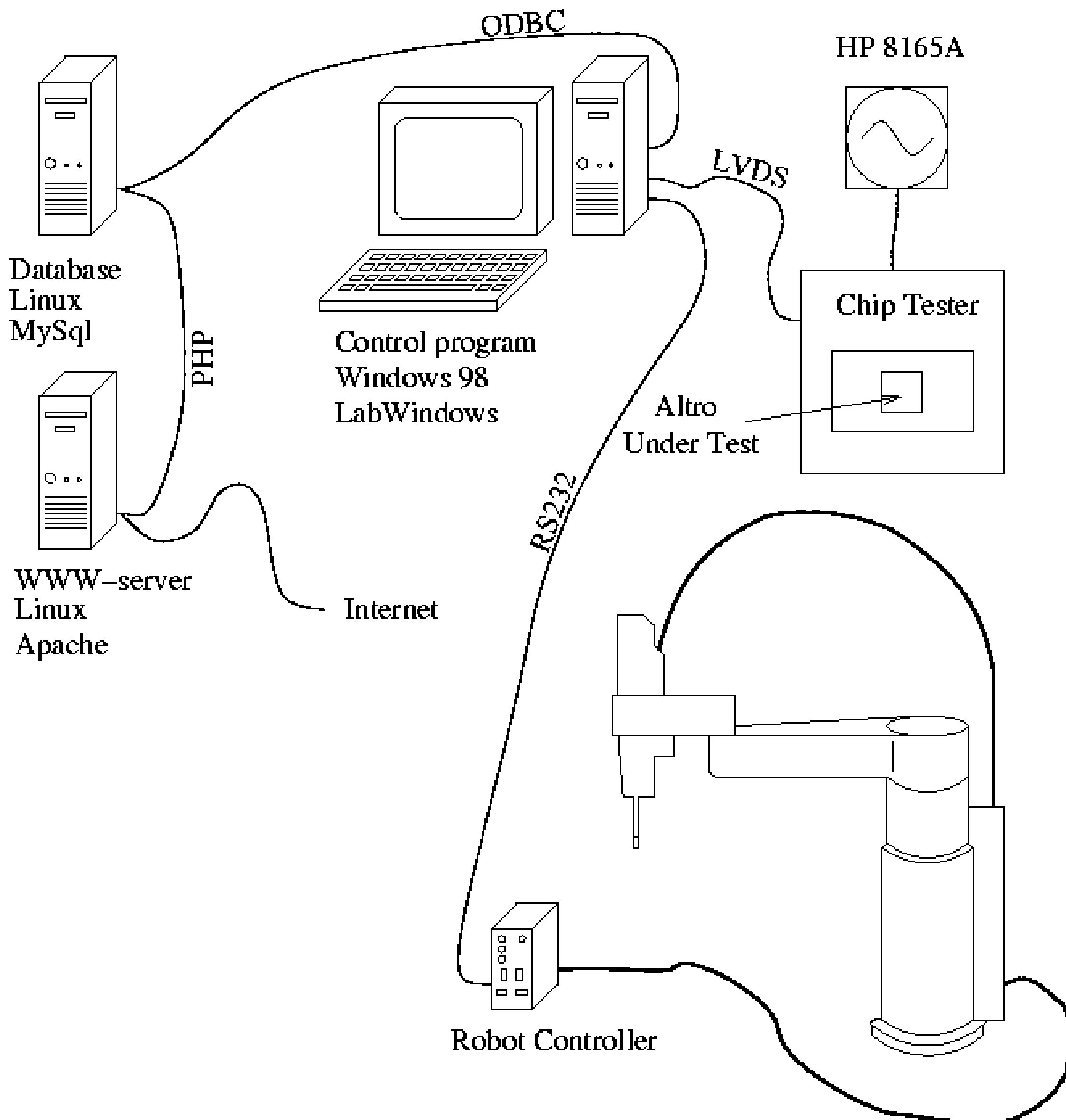

Figure 1. Schematic diagram of the Test System.

The summary results of the test together with the chip serial number are written into a database (MySql), which resides in a PC (*Database PC*) operating under Linux. The complete information for each tested chip is recorded in a set of files for further analysis. For example, if a chip contains a defect, the typology and location of the defect are stored in a file. The position of all tested chips is also stored in a database. Most of the database information is accessible through a web-interface.

Figure 2. Photograph of the Test System.

The Test System includes two other apparatuses. The first one is an oven, which is used for the burn-in of the chips. The other is a modified pen-plotter that is used to write a serial number on each chip.

2.1 Test strategy

The post-fabrication tests are performed to detect the small percentage of devices that are faulty, as a result of various defect mechanisms present in the fabrication and packaging process. This involves identifying the correctly functioning devices, but not characterising their dynamic performance. As already mentioned, the acceptance test applies a set of test vectors and measurements. These verify the input-to-output transfer of the chip under test, and check its static specifications such as input and output cell parameters. The generation of a set of test vectors with high fault coverage is of primary importance in order to reduce the probability that a defective chip passes the test. In the case of the ALTRO chip this problem was tackled during the design phase and led, as shortly described hereunder, to a number of features and auxiliary circuits that improve its testability.

The ALTRO chip has two modes of operation (see [1], Section 2.8): *Test Mode* and *Run Mode*. The *Test Mode* was conceived to allow a direct test of the ADCs. The output of 4 ADCs is the bi-directional output bus BD [39:0]. There are two selection lines, ADC_ADD0 and ADC_ADD1, which define which set of 4 ADCs among the 16 are

connected to the output port.

The *Pedestal* and *Data Memories*, which count for about 65 % of the total number of gates in the chip, are fully accessible in read and write mode. The *Baseline Correction I* circuit allows the injection of test patterns into the *Data Processor* or directly into the *Data Memory*. The possibility of activating selectively the different blocks of the *Data Processor* allows performing the test of the various blocks separately.

2.2 The Chip Tester

The *Chip Tester* has been conceived and designed to be general purpose. A simplified block diagram of the tester is shown in figure 3. The real apparatus contains additional blocks that implement functions that are not used for testing the ALTRO chips.

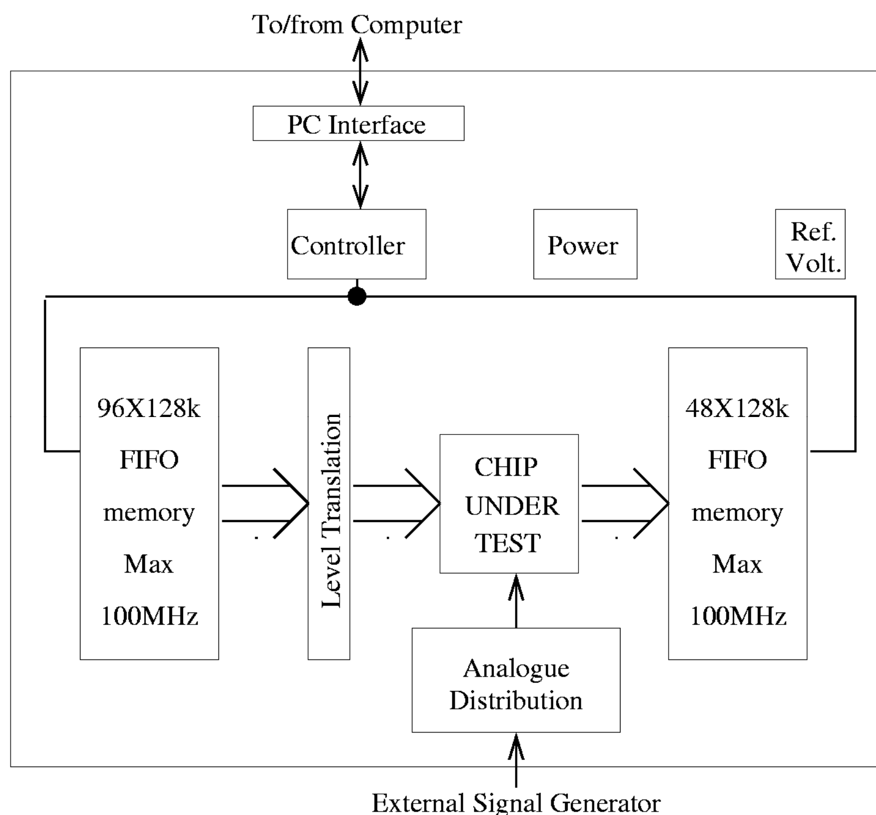

Figure 3. Simplified block diagram of the Chip Tester.

FIFO Memories

For the test of the digital part of the ALTRO chip, the test pattern is first downloaded into the out-FIFOs. During the execution of the test, the FIFO memories output progressively their content stimulating the chip under test. Concurrently the output signals of the chip under test are acquired in the in-FIFOs. It should be noticed that the out-FIFO and in-FIFO memories can both be addressed at a rate (100MHz) 2.5 times higher than the nominal frequency of the ALTRO master clock (40MHz). This simple mechanism, which is illustrated in figure 4, allows an easy and fast generation of any test

pattern, and a precise measurement of the response of the circuit.

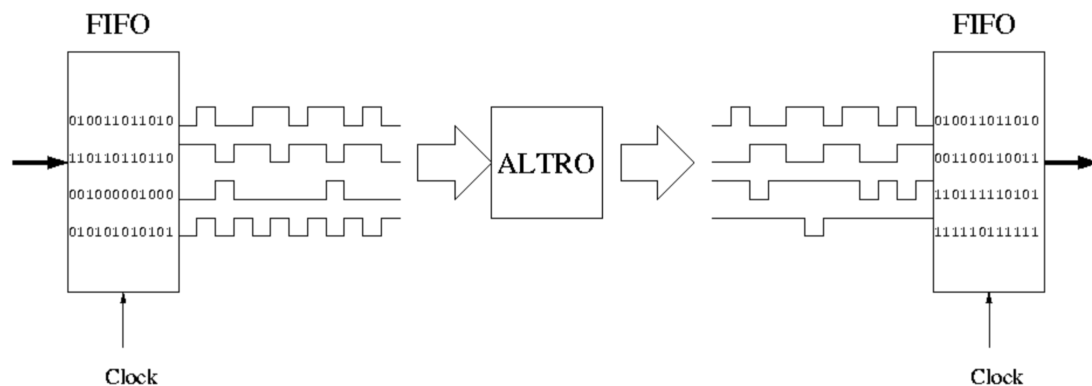

Figure 4. Scheme for the generation of the test pattern and measurement of the circuit's response.

For all digital tests, the result of the measurement, which is contained in the in-FIFOs, is compared with the expected pattern. Any mismatch leads to the identification of a fault. For the test of the ADCs only the in-FIFOs are used. In this case, the content of the memories is not treated as digital pattern, but as set of samples (see below).

Level Translators

The FIFO memories, as most of the other circuits in the Chip Tester, generate CMOS 3.3V output signals, but are also compatible with CMOS 2.5V input signals. On the other hand, the ALTRO's input/output are CMOS 2.5V signals. Therefore, the output signals of the out-FIFO need to be converted by a level translation circuit (74ALVC164245).

Reference voltage

The ALTRO chip requires two reference voltages, V_t (top reference voltage) and V_b (bottom reference voltage), which define the dynamic range and the conversion gain of the ADCs, and should be set to 1V and 0V respectively. V_b is simply connected to the analogue ground, while V_t is derived from a 2.5V band gap reference generator. The 2.5V reference is divided, adjusted and then buffered by a unity gain amplifier.

PC Interface

The *Chip Tester* is interfaced to the PC via a special link and a PCI card with a PCI-controller, PLX9050, and LVDS transceivers. This link has many similarities with the SCSI interface. The signals have the same level and are transported via the same type of connectors, cables and terminators as for the SCSI bus. However, the protocol is different and much simpler. It implements a master/slave configuration where the PCI-controller is the master and the *Chip Tester* the slave. There are 16 bi-directional data lines, 7 address lines, and a few control lines (read, write, reset and interrupt). All transactions are initiated by the PC.

Power Regulation and Current Sensing

The *Chip Tester* distributes the supply voltages to the chip under test and the interface circuits, through three programmable voltage regulators. One of the regulators supplies

the analogue part of the ALTRO chip, the second regulator supplies the digital part, and the third one supplies the digital buffers that are interfaced to the chip under test. The current drawn by the voltage regulators is continuously sensed and measured by dedicated ADCs. In this way it is possible to read the current drawn by the analogue and digital part separately. It is also possible to run the chip on nominal supply voltages and set the input signals to a lower voltage. The possibility to have a fast measurement of the supply currents is also very important to prevent any damage to the test equipment, as it could happen, for instance, in the case of a chip with an internal short circuit. Both the analogue and digital supply voltages can be disabled by a relay.

Analogue interface

The differential input signals of the ADCs are driven by a mezzanine card, which can be plugged into the Chip Tester as daughter card. This card has a single input that is fan-out and converted into 16 differential output signals. The distribution of the input signal to the output buffers can be controlled singly for each channel. The conversion from single-ended to differential signals is done by a low distortion high-speed driver [3]. The common-mode level of the differential output pair is also adjustable. The output impedance has been set to the value of the PASA output impedance, in order to reproduce the same conditions under which the ALTRO chip is operated in the ALICE TPC Front End Card.

The Control Unit

The Control Unit is responsible for interpreting the high-level commands issued by the PC. It also distributes various timing signals to the chip under test and to other test circuits like the FIFOs. A schematic diagram of the controller and its interplay with the other main circuits is shown in figure 5

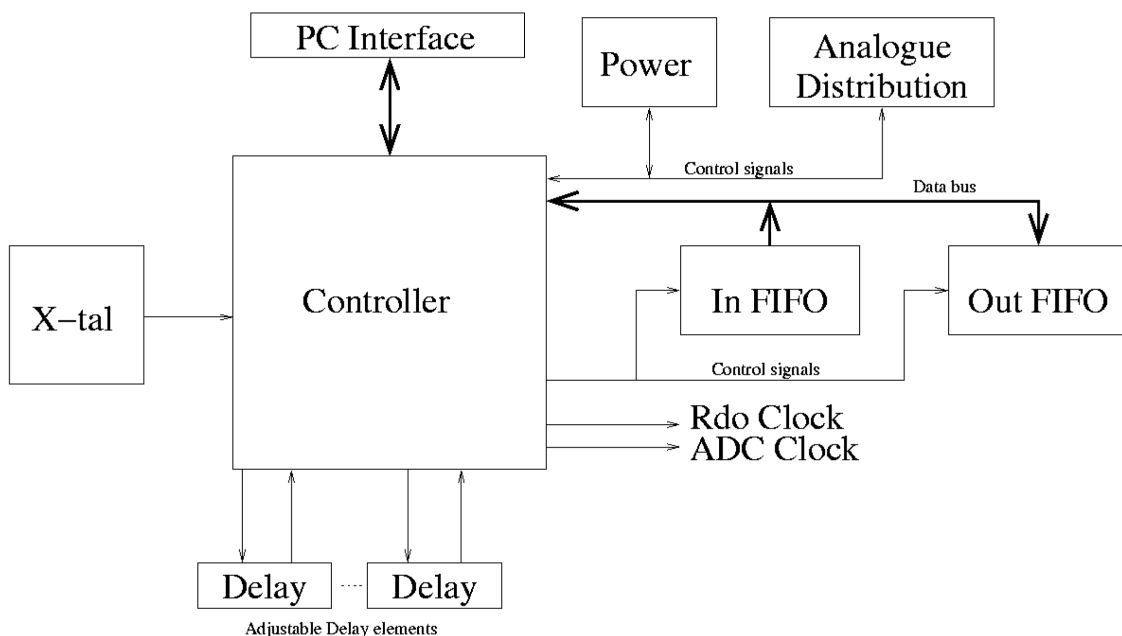

Figure 5. Schematic view of the controller.

From the master (PC) point of view, the tester is seen as a set of registers and memories. The modules for the distribution of the supply voltages and the distribution of the analogue signals are both controlled via a local SPI bus (serial line). The Control Unit converts the PC commands and data into the SPI serial data.

The Readout Clock (RCLK) and Sampling Clock (SCLK) for the ALTRO chip and the read and write signals for the out-FIFOs and in-FIFOs are all derived from the same master clock signal generated by a quartz oscillator. The phase of these signals can be singly adjusted by means of a set of programmable delay units.

3 Test procedure

The test of the ALTRO chip comprises four phases: 1) the burn-in; 2) marking; 3) power test; 4) functional test. This section describes these four phases.

3.1 Burn-in

The chips are delivered by the manufacturer in plastic trays, each containing 40 chips. Prior to any electrical or functional test, all chips undergo a thermal stress cycle inside an oven. The procedure consists in placing the chips in an oven, without removing them from their trays, rising the temperature till 120°C, keeping this temperature for a period of 12 hours and lowering the temperature again to 25°C. This temperature cycle is executed twice. It should be noticed that the chips are not removed from the trays and are not powered. According to the manufacturer of the ALTRO chip (STMicroelectronics), this procedure makes visible the large majority of the manufacturing defects that otherwise would appear after a long continuous operation of the device.

3.2 Marking

After the burn-in the chips are marked with a serial number. During this operation, which is executed by a modified pen-plotter, the chips are still kept in the carrier trays. The chips trays themselves are also marked with a serial number. In the database, the chip serial number, the tray serial number and the position of the chip in the tray are recorded. In this way, we can always trace back the production lot and wafer to which the chip belongs, the tray in which the chip is stored and its location in the tray. Conversely, given a tray number we can produce the list of chips that it contains, and their status. An example is shown in figure 6.

3.2 Power test

After the marking, the acceptance test starts with the verification of the power consumption of the chip. The two supply currents, respectively the digital current I_d for the Data Processor and the analogue current I_a for the ADCs, are measured with and without readout clock (RCLK) and sampling clock (SCLK).

If the value of the supply currents is out of the acceptance ranges listed in table 1, the chip is considered defective and rejected.

Supply Currents	Mode of operation	Min (mA)	Max (mA)
Analogue	Standby	70	100
	Running Clocks		
Digital	Standby	5	25
	Running Clocks	15	40

Table 1. Range of acceptance for the supply currents of the ALTRO chip.

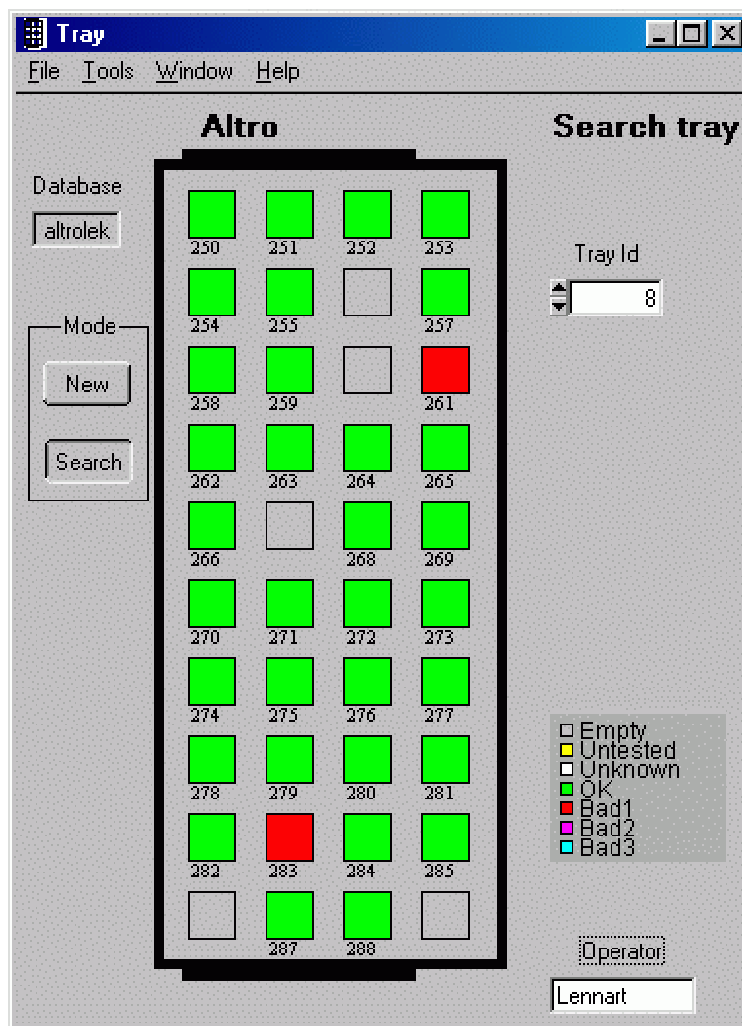

Figure 6. Display of the status of the chips contained in a tray

3.3 Functional Test

After the power test, the chips undergo a series of functional tests, each dedicated to the verification of one of the chip's internal blocks: Configuration and Status Registers, Pedestal Memories, Digital Processing Chain, Data Memories, ADCs.

3.3.1 Verification of the Configuration and Status Registers

All Configuration and Status Registers (CSRs), which can be accessed in write and read mode, are verified by writing and reading back several test patterns. For example a 10-bit register is tested with the following patterns: 10'h000, 10'h3FF, 10'h155 and 10'h'2AA. The read-only registers - status registers and counters - are indirectly verified by performing a set of tests that cause a predictable modification of their values. The content of these registers is then read back and compared with the expected values. The verification of the address decoder is performed by writing and reading back all registers with different values. Moreover, the chip hardware address, which is defined by 4 dedicated input pins (HADD[3:0]), is also tested by applying different patterns and reading back the value of the register ADEVL (see [1] section 2.3). If any of the registers is not working properly the chip is rejected.

3.3.2 Verification of the Pedestal Memories

The Pedestal Memories can be accessed through the registers PMADD and PMDTA (see [1], section 2.3). Through these registers all locations of the pedestal memories are verified with 5 different test patterns. Each test pattern, which consists of 1024 10-bit words, is first written to all pedestal memories and then read back channel by channel. The first 4 patterns consist of the following 4 words: 10'h000, 10'h3FF, 10'h155 and 10'h'2AA. The fifth pattern consists of 1024 10-bit words with incremental values from 0 to 1023 (ramp).

3.3.3 Verification of the Data Memories

The Data Memories can not be directly accessed. Therefore, the verification of the Data Memories is done by operating the *BCI* circuit as pattern generator (see [1], section 1.3). In *test mode* the BCI circuit can be used to generate a pattern to be injected in the processing chain, replacing the input signals samples. If all functions of the processing chain are disabled, upon arrival of a L1 trigger this pattern will be transferred unmodified to the data memories. By issuing to the chip the appropriate sequence of commands, WPINC, CHRDO and RPINC (see [1], section 2.3), this pattern can be read back from the 40-bit output port.

The multi-acquisition data memories can be partitioned (see [1], section 1.8) in either 4 buffers, each consisting of 256 40-bit words, or in 8 buffers, each consisting of 128 40-bit words. Most of the tests of the data memories are executed with the 4-buffer partition. These tests are performed by initializing the pedestal memories with the first four of the 5 test patterns described in section 3.3.2. Each time four L1 triggers are issued to fill up all buffers before reading them back. Once verified that all memory cells are free of defects, the 8-buffer configuration is tested by injecting short sequences of different patterns in each buffer. It should be noted that any error in the pedestal memory or in the processing chain would also appear as an error in the data memories. However, a detailed analysis of the test result allows a rather easy differentiation between them.

3.3.4 Verification of the Processing Chain

A set of tests, corresponding to different configurations of the Processing Chain, are performed by operating the *BCI* circuit in *test mode*. After the initialization of the pedestal memories and the Processing Chain, a trigger is issued starting the processing and acquisition of the test pattern in the data memories. The resulting data block is then readout and compared with the expected result. This procedure is repeated for a number of different patterns and configurations of the processing chain. The test patterns and the configuration have been defined to have the maximum fault coverage. The test program does not contain any specific diagnostic package to identify the precise location of the defective gate. Any error is considered a fatal error and the chip is rejected.

3.4 Test of the A/D converters

There are many reasons why an ADC with N bits does not perform like an ideal N-bit converter under dynamic operating conditions. Several parameters are universally used to define these different sources of errors: Differential Non Linearity (DNL), Integral Non Linearity (INL), offset error, gain error, Total Harmonic Distortion (THD), aperture jitter, aperture delay, etc. The values of these parameters characterize the ADC and give an in-depth knowledge of the ADC behaviour. There are several techniques to access these parameters. They are generally classified in two main categories, Static Tests and Dynamic Tests, according to whether the input test stimulus is respectively a static or dynamic signal. All tests performed on the ADCs for the acceptance of the ALTRO chips are Dynamic and make use of sine waves as stimuli. Sine waves are chosen because are easy to generate at the frequencies of interest with adequate fidelity, and their simple mathematical model simplifies the algorithms used for the data analysis. Two dynamic tests are applied to the ADCs: the Histogram test and the Curve Fitting. For both tests, a sine wave is supplied to the ADCs and data is acquired and analysed in the PC. These tests are used to identify specific error typologies. A set of figures assesses the performance of the ADCs. Effective Number Of Bits (ENOB), Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) aimed at proving the correct ADC behaviour. The frequency spectrum shows the nature of the noise and the Spurious-Free Dynamic Range (SFDR).

3.4.1 Histogram test

This test allows the measurement of: 1) the DNL and in particular the identification of missing codes; 2) the gain error; 3) the offset error. The histogram test also yields the best information about individual code bin size at an arbitrary frequency.

A statistically significant number of samples of the input sinusoid are taken and stored. The frequency of code occurrence in the record is then plotted as a function of code, and compared with the shape of the plot given by an ideal ADC. This plot is the Probability Density Function (PDF) of a sine wave provided that the input and sample frequency are relatively independent.

In the formula given in figure 7, A is the sine wave amplitude and V is the independent variable, the voltage. The sine wave is programmed to exceed the upper and lower decision levels by a fairly wide margin to make sure that the sine wave passes through all the codes in order to get a histogram of all code widths.

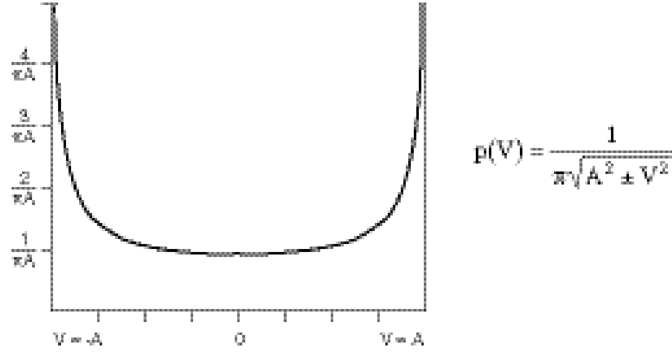

Figure 7. Sine wave probability function.

This test can be performed as a process of sampling the input signal and sorting the digitised samples into bins. Each bin represents a single output code and collects samples whose values fall in a specific range. The number of samples collected in each bin varies according to the input signal. If N is the number of ADC bits, there are 2^N bins. Ideally, if B is the full-scale range of the ADC in volts, each bin corresponds to a range of sample sizes covering $B/2^N$ volts. For a real ADC, fewer or greater than the expected number of occurrences for a given code bin indicates that the effective code bin width is smaller or larger respectively than ideal.

The exact offset and amplitude of the sinusoidal input waveform is not known, but the number of collected samples at the upper and lower codes can be used to calculate them. The equations that relate the number of collected samples for these codes to the offset and the amplitude of the sine wave expressed in terms of LSBs are:

$$\text{offset} = \left(\frac{C_2 - C_1}{C_2 + C_1}\right)\left(2^{N-1} - 1\right); \quad \text{peak} = \frac{2^{N-1} - 1 - \text{offset}}{C_1};$$
$$\text{with} \quad C_1 = \cos\left(\pi \frac{H\left(2^N - 1\right)}{N_S}\right); \quad C_2 = \cos\left(\pi \frac{H(0)}{N_S}\right) \tag{1}$$

where $H(2^N\text{-}1)$ and $H(0)$ are the number of samples collected in the upper and the lower code respectively, and N_S is the total number of samples.

Now, it is possible to calculate the ideal sine wave distribution of collected samples that would expect from a perfect linear ADC excited by a sinusoid. This corresponds to the integral of the probability density function of a sinusoid over the bin (Ideal Probability):

$$P(i) = \frac{N_S}{\pi}\left[\sin^{-1}\left(\frac{i + 1 - 2^{N-1} - offset}{peak}\right) - \sin^{-1}\left(\frac{i - 2^{N-1} - offset}{peak}\right)\right] \qquad i = \left[1, 2^N - 2\right] \tag{2}$$

To calculate the real probability for each code in the measured data record, the number of occurrences for each code is divided by the number of samples in the record

(Measured Probability).

The parameter of greatest interest that can be calculated using the histogram test is the DNL. It is a measure of the width of each code bin in units of LSB, i.e. of how varies each code bin in size with respect to the ideal:

$$DNL(i) = \frac{Measured\ \Pr obability\ (i)}{Ideal\ \Pr obability\ (i)} - 1 \qquad i = \left[1, 2^N - 2\right] \tag{3}$$

Chips that have a DNL outside the acceptance range ±0.7 will be rejected as defective.

3.4.2 Curve fitting

This test provides a description of the ADC dynamic performance. The result of this test is a figure of merit called ENOB. It is a measure of the inaccuracy of the ADC at a given frequency. Several factors contribute to this inaccuracy, as harmonic distortion, noise and aperture uncertainty. Gain, offset, and phase errors do not affect the results since they are ignored in this test.

This measurement is obtained by analysing a record of data taken from a sine wave source. The analysis consists in calculating the sine wave that is the best fit of the data record. The sine wave is of the form $A sin(2\pi f + B) + C$ where A, f, B and C are the parameter selected for a best fit. The rms of the residuals determines the ENOB, according to the following equation:

$$\mathrm{ENOB} = \mathrm{N} - \log_2\left(\frac{\text{actual rms error}}{\text{ideal rms error}}\right) \tag{4}$$

where N is the number obits.

In an ideal sampling system, the sampled analogue signal is fee of noise source and distortions. The only limitation to the system accuracy is the quantization error. The quantization error occurs whenever an analogue signal is sampled and its value is represented by a finite number. The quantization error defines a base noise level, which limits the system ability to resolve small signals. The rms value of the quantization error, which corresponds to the ideal rms error, is:

$$ideal\ rms\ error = \frac{Q}{\sqrt{12}} \tag{5}$$

where Q is the ideal code bin width. The actual rms error is simply the square root of the sum of the squared errors of the measured data record.

Chips that have a DNL below 9.5 bits will be rejected as defective.

3.4.3 Verification of the error detection function

The ALTRO chip contains a number of circuits that have the function of detecting several error conditions (see [1], section 2.4, p. 40, 41). This test includes:

- Writing to a register with wrong parity;
- Writing to a read-only register;
- Reading from a register in broadcast mode;
- Reading out an event when the multi-event buffer is empty;
- Issuing a new trigger while the chip is busy processing the previous trigger.

After each test, both the ERROR signal and the ERROR register are examined, and appropriately cleared.

3.5 Recording of information

For each chip tested, the following information is recorded in a database based on MySQL:

- The location of the chip (tray, row, column);
- Status (*untested* / *functional* / *not-functional*);
- Date and time of the test;
- Name of the test operator;
- Summary of the test results: Supply currents values (analogue and digital, with and without clock signals), DNL, ENOB, gain and offset of all channels;

The information recorded in the database can also be output in an ASCII file.

In addition to the information recorded in the database, for each *non-functional* chip the complete measurement data, as produced by the chip tester, is recorded in a binary file. This data can always be retrieved by using the *Auxiliary Analysis Program* tools (see section 4.3).

4 Software

The operation of the tests and the analysis of the results are preformed under the control of a LabWindow based test program.

The API consists of four packages. A first package (Test Opeation Program) controls the execution of the test, i.e. the operation of the Chip Tester and the Waveform Generator, and the analysis of the results. A second package (Robot Control Program) controls the motion of the robot and the sorting of the chips according to the test results. A third package (Auxiliary Analysis Program) contains a number of auxiliary programs that allow a detailed analysis of the test results. The fourth package (Database Access Program), which controls the access to the database, is used to record, retrieve and update the test results and some statistical information. Most of the routines of these four packages are written in C and then embedded in the LabWindows application.

4.1 Test Operation Program

This program controls the operation of the Chip Tester and the Waveform Generator, and performs the analysis of the measurements producing the test results. This program is interfaced to the Robot Control Program and to the Database Access Program. In the automatic test procedure, the Operation Program receives from the Robot Control Program the command to execute the test of a chip, which has been already placed on the Chip Tester. After the test, the Test Operation Program passes the results to the Robot Control Program.

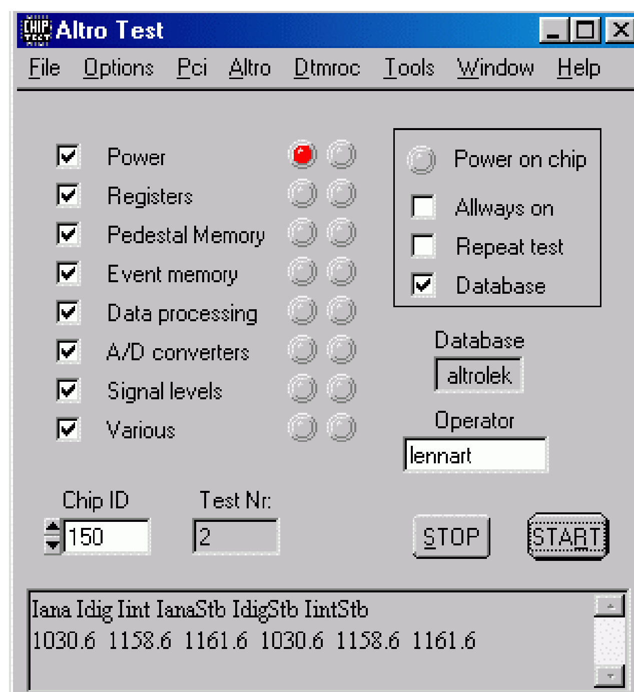

Figure 8. Control Panel of the Test Operation Program.

Figure 8 shows the control panel of the Test Operation Program. This control panel can be used to run the Operation Test Program in standalone mode. It is possible to

select/deselect groups of tests. It is also possible to run the test in loop mode; in this case, unless aborted, the test will be continuously repeated till the occurrence of a failure. It is also possible to enable/disable the recording of the test results in the database.

4.2 The Robot Control Program

The Robot Control Program controls all motions of the robot. Figure 9 shows the control panel. In this panel the operator has to enter the serial numbers of the chips trays that are currently on the test bench. The program makes a request to the Database Access Program to retrieve from the database the information related to the status of the chips. Unless defined by the operator, the Robot Control Program will also define, according to the test results, the location of the chip in one of the destination trays.

When the test is launched the program selects the first untested chip and issues to the robot controller the command to move the chip into the Chip Tester. The execution of this operation is acknowledged by the Robot controller. The Robot Control Program communicates the chip serial number and the command to start the execution of the test to the Test Operation Program. Once the test has been accomplished, the Robot Control Program sends to the robot controller the command to move the chip into the appropriate tray, according to the test results. Eventually, the Robot Control Program updates the test summary results and the new position of the chip.

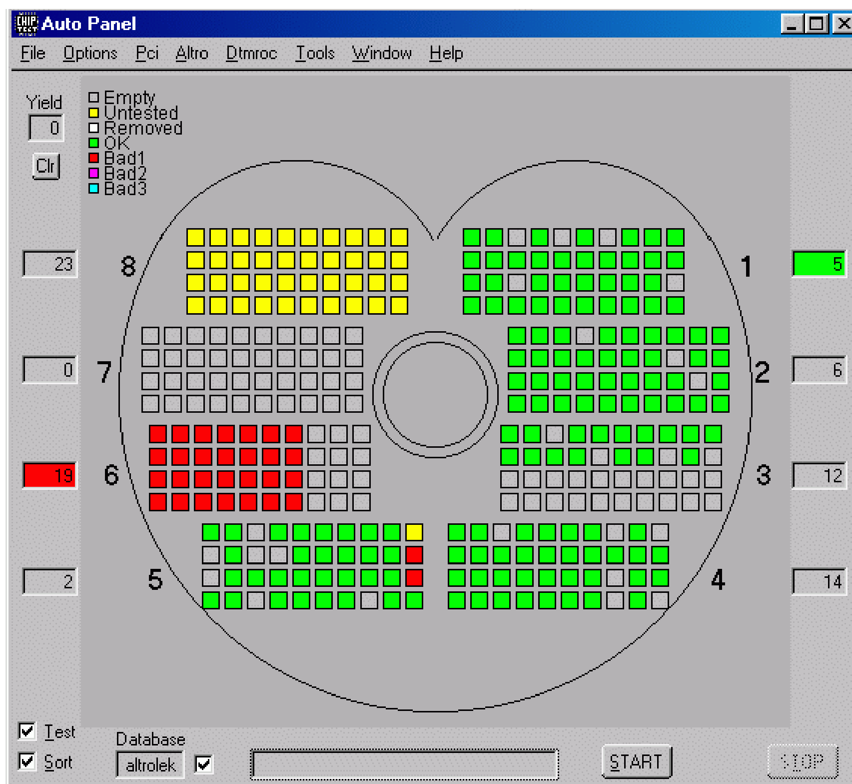

Figure 9. The control panel of the Robot Control Program.

It is also possible to run the Robot Control Program without sorting the chips

according to the test results. In this case the chips are placed back in their original position. Conversely, it is also possible to sort the chips without performing any tests.

4.3 Auxiliary Analysis Program

4.3.1 Visualization of the test vectors

As show in figure 10, this program displays the input test vectors, the actual response of the chip under test and the expected results. Any mismatch is marked with the * character at the end of the line.

Figure 10. Digital test analyse program.

4.3.2 Analogue Test Analyse Program

As for the digital tests, for the test of the ADCs exist a number of auxiliary programs that allow to display the measurements and the results of the analysis. Some examples are shown in figures 11, 12 and 13.

Figure 11. Display of the measurement of the ADC output signals.

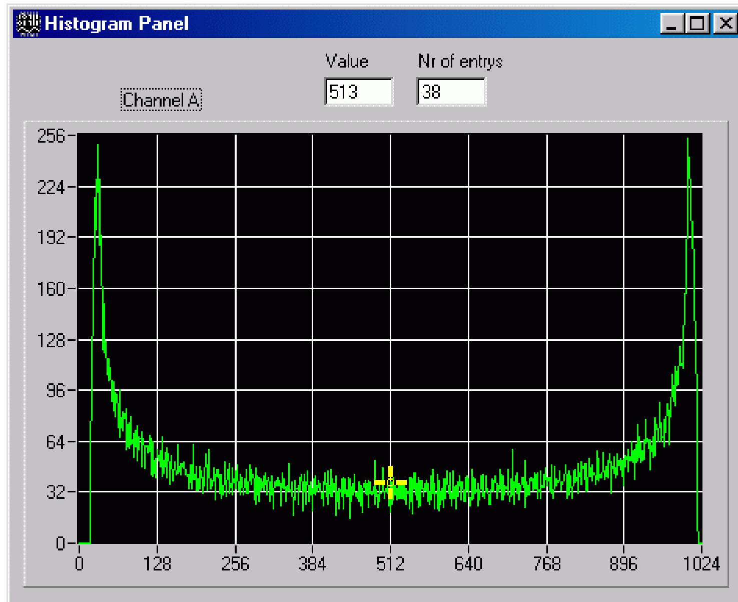

Figure 12. Histogram of the samples from a sine-wave

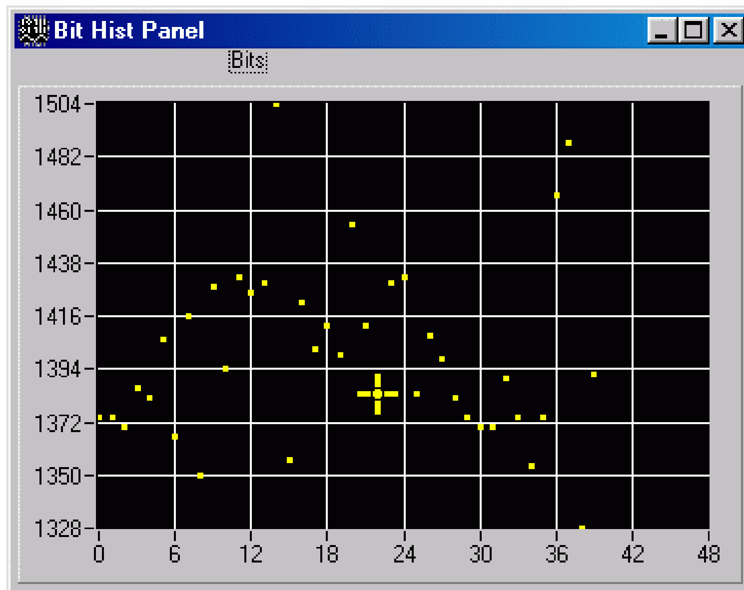

Figure 13. Histogram of the bits of the 40-bit data bus.

5 Handling of the chips

In order to avoid damaging the chips, a few important precautions are adopted for the execution of the tests. Since the chips are already packaged, it is not required to perform the test in a controlled clean room. However, in order to avoid an excessive production of dust, the laboratory which hosts the test facility is subject to restricted access. No other work unrelated to the tests is allowed in the test room. Moreover, the test benches, the test equipment, and the operators are all furnished with the installations for ESD protection. The chips are delivered in trays each containing 40 devices. Normally the chips are never removed by the trays, except during the test. Manual handling is in general avoided. In the rare occasions the operator needs to manually adjust the position of a chip in the carrier tray, this operation is executed with a special pick-up tool.

6 Test results

In this section we summarize the results obtained in the mass production test of the ALTRO chips for the ALICE TPC. The chips have been produced in two runs: one engineering run, consisting of 1 lot of 6 wafers, followed, after the approval of the engineering samples, by a production run consisting of 5 lots (125 wafers). The whole production - wafer manufacturing, dicing and packaging - yielded 49127 chips.

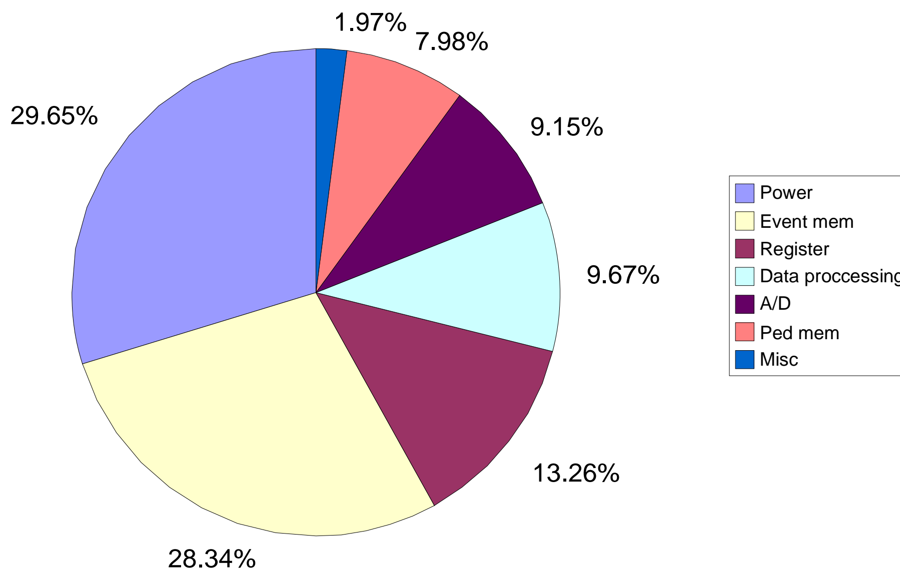

Figure 14. Failure analysis of the ALTRO chips for the ALICE TPC. The pie chart, which is relative to the 16% of the chips that have not passed the acceptance test, shows the occurrence of the different failure mechanisms.

Out of the 49127 tested chips, 41297 have passed the test without any error, which corresponds to 84% yield, and 7830 chips have failed the test. As detailed in fig. 14, about 30% of the faulty chips have shown excessive power dissipation. Faults (single/bit

stuck) in the configuration/status registers are also quite common and count for about 13% of the failing chips. It should be noticed however, that chips that have shown multiple faults, were sorted in the class configuration/status register error, simply because in the test sequence, the registers are tested first. About 36% of the faulty chips have one or more bit-stuck in the memories, either the data memories (28%) or the pedestal memories (8%). The ration between the number of faults in the pedestal memories and in the data memories is consistent with the ratio between their sizes, i.e. their respective number of cells.

An error in the pedestal memories generates also an error in the data memories test. This is due to the fact that in the data memory test, the pedestal memories are used as pattern generator for the data memories. However, in our classification, an error was identified as data memory error only in the case the corresponding bit of the pedestal memory does not contain any fault. The processing chain contributes for about 10% of the errors. As in the case of the data memories, an error in the pedestal memories or in the data memories could be wrongly identified also as errors in the processing chain. Therefore, have been classified as “processing chain” errors only those shown by chips with all memories free of defects. The ADCs count for about 9% of the total number of errors.

7 References

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