THE FRONT-END CARD

1. Overview

The Front-End Card (FEC) contains the complete read-out chain for amplifying, shaping, digitising, processing and buffering the TPC signals. The FEC must handle the signal dynamic range of about 10 bits with minimal degradation of precision, store the signals during the Level-2 trigger latency. The design provides 128 channels per FEC, with an estimated maximum power consumption of approximately 6 W.

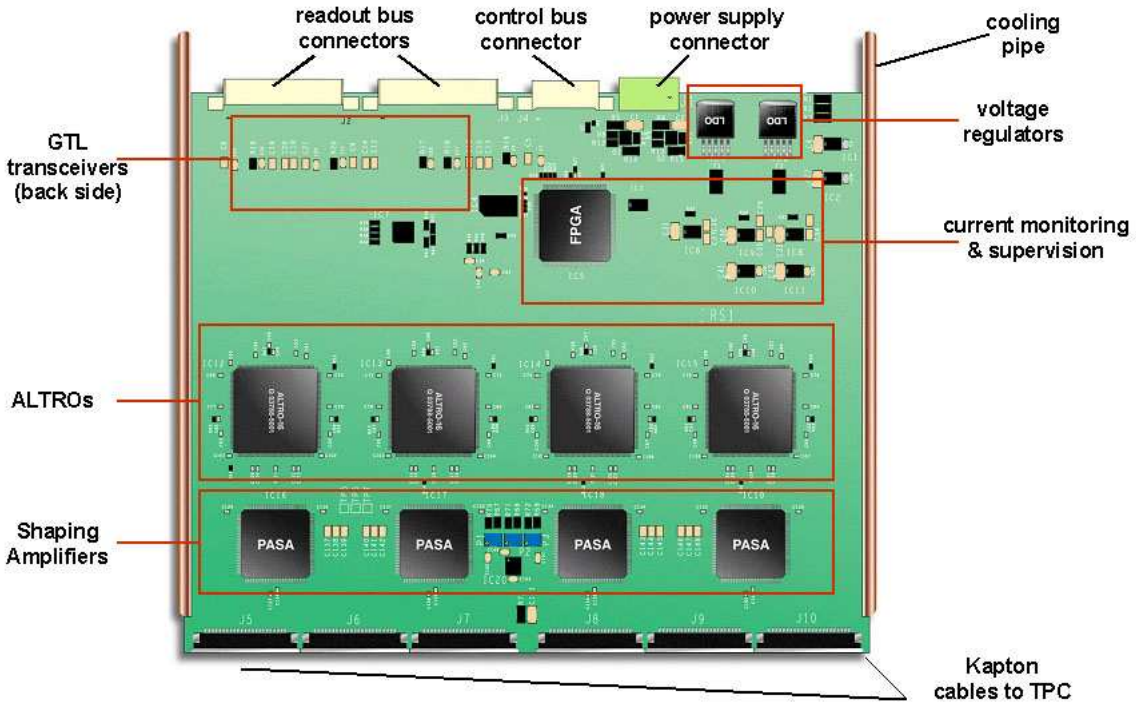


Fig. 1. FEC layout. The components are mounted on both sides of the board. The figure shows the board topside with 4PASAs, 4 ALTROs, 1FPGA the voltage regulators and other minor components. On the bottom side of the board are symmetrically mounted other 4 PASAs and 4 ALTRO and, close to the readout bus connectors, the GTL transceivers.

The layout of the FEC is shown in fig 1 and has the following flow. The FEC receives 128 analogue signals through 6 flexible cables and the corresponding connectors as shown in the figure. The input signals are very fast, with a rise time of less than 1ns. Therefore, to minimise the channel-to-channel crosstalk, the PASA circuits have to be very close to the input connectors. The signals are first amplified and then processed by a pass-band filter. The latter operation is done to limit the bandwidth of the ADC input signal and to reduce the signal-to-noise ratio. A 16-channel chip (PASA) contains the circuits to implement these analogue functions. Each FEC contains therefore 8 PASA chips. The analogue to digital conversion and the digital processing are done inside the ALTRO chips that incorporate 16 channels each.

Inside the ALTRO chip, the digitised signals are processed and stored in a memory, where they wait for a 2nd level trigger, to be either read-out or discarded. In the former case, the buffer will be frozen and protected against overwriting until the data is

transferred to the Readout Control Unit (RCU). The details of the data transmission protocol are discussed in [1]. In the latter case, the buffer is made available to store a new data set.

The FEC channels are multiplexed, at the board level, via a LVCMOS (low-voltage CMOS) bus. It features an asynchronous VME-like protocol, which is enhanced by a "clocked block-transfer" (CBT) that provides a bandwidth of up to 300Mbytes/sec. The FEC is interfaced to the RCU through a 40-bit bus that is based on the GTL (gunning transistor logic) standard. At the board output the bus signals are translated from LVCMOS level to GTL level by bi-directional transceivers. The configuration, readout and test of the board are done via the GTL bus. However the FEC contains a circuit, named Board Controller (BC), implemented in a FPGA, which provides to the RCU an independent access to the FEC via a field-bus. This secondary access is normally used to control the state of the voltage regulators and monitor the board activity, power supplies and temperature.

The board offers a number of test facilities. As an example a data pattern can be written in the ALTRO chip and readout back exercising the complete readout chain. The Board Controller allows verifying the bus activities, the presence of the clock and the number of triggers received.

The ALTRO chips and the BC work synchronously under the master clock frequency of 40 MHz. The ALTRO circuits usually perform the same operations simultaneously under the control of the RCU, which can also control a single channel at a time. This is performed in the configuration phase and for test purposes. The RCU broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via the GTL bus.

The board layout can be seen as partitioned in 4 different sections: 1) the first section (PASA) contains the 8 PASAs; 2) the second section contains the ADCs part of the ALTRO chips; 3) the third section contains the digital part of the ALTRO chips; the last part contains the LVCMOS to GTL transceivers and the BC. As detailed in section 2 the FEC is powered by means of 4 power cables bearing 2 supply voltages (+4.3V, +2.5V) and their corresponding ground signals. From the 2 main supply voltages, 3 supply voltages are derived and distributed (+2.5V for the ALTROs, +2.5V for the FPGA and the GLT transceivers and +3.3V for the PASAs). The last section is powered independently with +3.3V. The voltage regulators feature power-mode that is remotely controllable. The ON/OFF pin of the voltage regulators related to the same section are controlled via the BC, which monitors the current supplied by each voltage regulator. It can be programmed to power-down the sections where the monitored quantities exceed an upper limit.

The photographs of the top and bottom side of the front-end card are shown in figs.2 and 3.

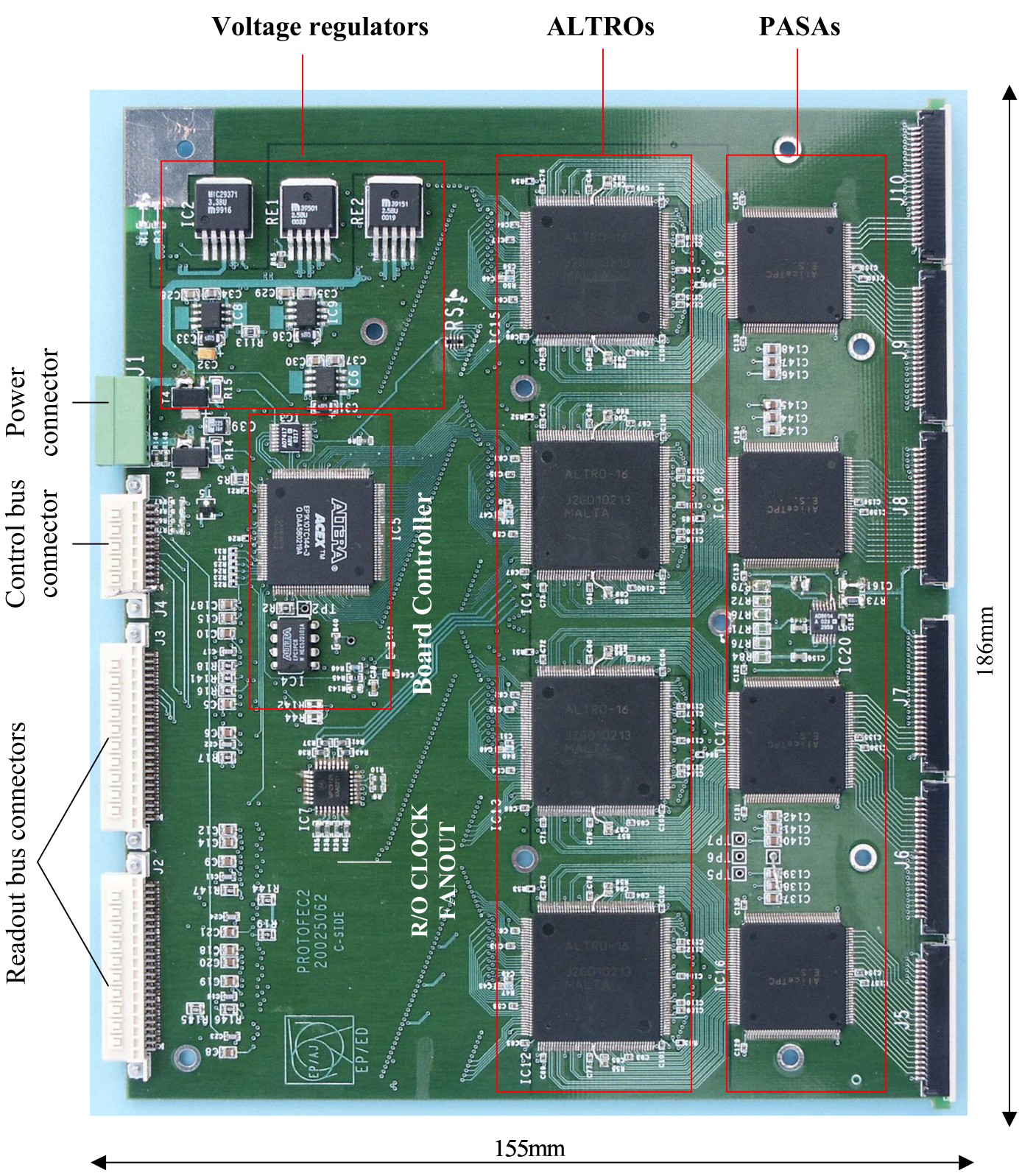


Fig 2. Photograph of the FEC topside.

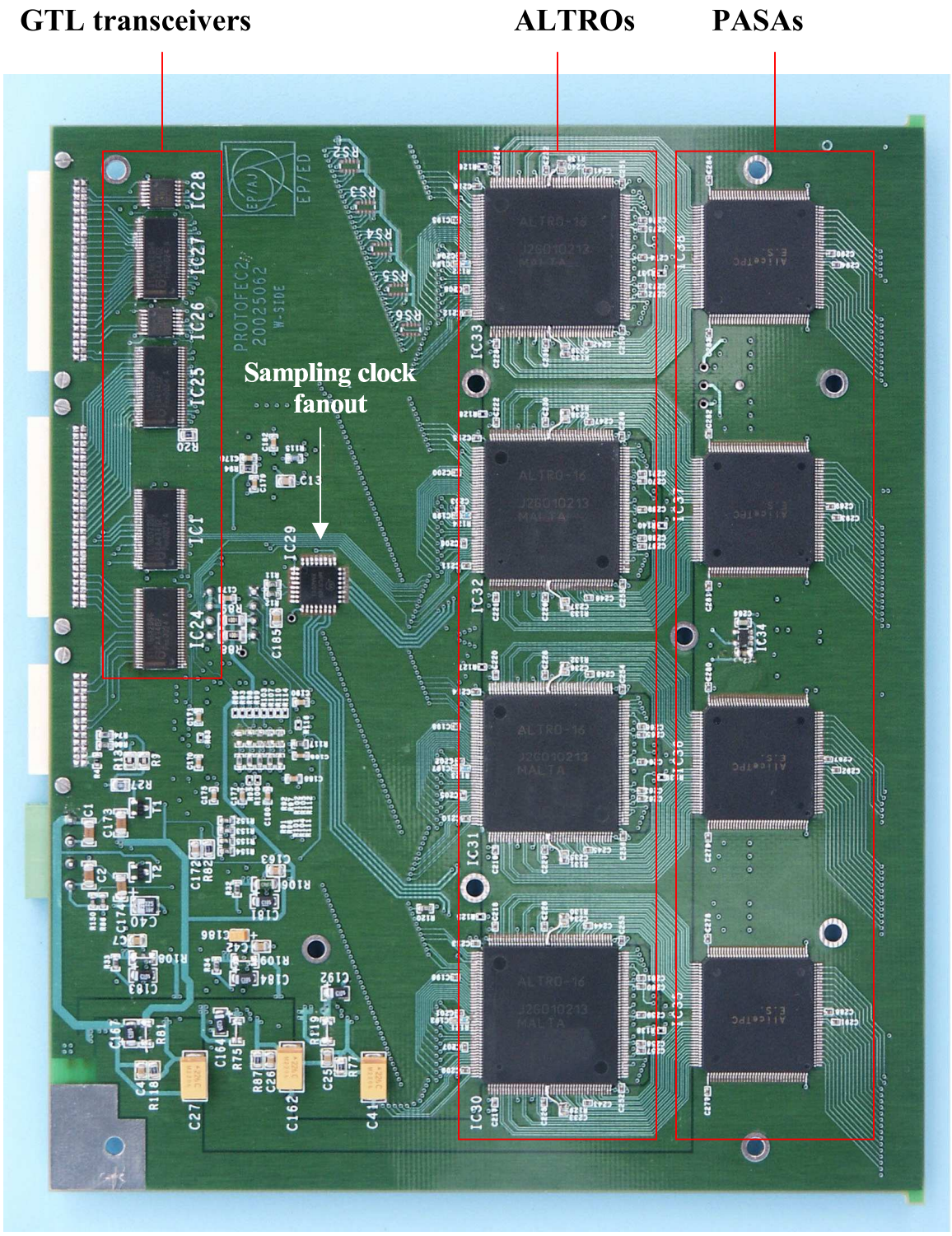


Fig.3. Photograph of the FEC bottom side.

2. Circuital description

This section describes the FEC from the circuital point of view. We will refer to the schematic diagrams reported in section 6 (figs.13-18) and to the FEC photographs in figs2-3.

2.1 Front End Connectors

The signals form 128 pads are transported to the FEC via 6 flexible kapton cables and input into the board via 6 connectors (Harwin F10-2802306), which are soldered on the board as shown in fig.2 (right side of the picture).

Each connector has 23 contacts, which are used in 2 different connection schemes: 4 of them have 2 ground lines and 21 signal lines, while the other 2 connectors have 1 ground line and 22 signal lines. The signals are directly routed to the PASA without ground interleaving.

2.2 PASA chips

At the board level, the PASA chips require a single supply voltage (3.3 V, GND) and three reference voltages: *top* (VRT)*, bottom* (VRB) *and common mode* (VCM), which define the steady state level of the differential output signals. These three reference voltages are common to the 8 PASAs and generated by an on board polarization circuit described hereafter (see also DRAWING 1 in fig.13).

A reference voltage of 2.048V (~0.1% accuracy), generated by a *Precision Micropower Low Dropout Voltage Referenc*e chip (LM4120), is split in the three reference voltages (VRB=0.529V, VRT=1.471V and VCM=1.024V) by a network based on high precision resistors (0.1% accuracy). The three reference voltages are eventually buffered by a quad high precision CMOS Operational Amplifier (AD8604) before being distributed to the PASAs.

It should be noted that VCM is also distributed to the VRT and VCM pins of the ALTRO chips. Inside the ALTRO chip this reference voltage is used to define the common mode of the input differential signals pair and the dynamic range of the ADCs.

The differential interconnection between the PASA and the ALTRO provides a good immunity to the board common mode noise, in particular the one generated by the sampling and readout clock signals distributed over the board.

2.3 ALTRO chips

As detailed in [2] the ALTRO chips are controlled by means of a 52-bit bus (ALTRO readout bus), 2 clock signals (sampling clock and readout clock), 8 hardware address lines that specify the chip address, and 4 test pins. The ALTRO read out bus consists of 40 data lines (bi-directional) and 12 lines for the control signals (uni-directional).

As for the PASAs, also the ALTRO chips are symmetrically mounted, 4 on the top and 4 on the bottom side of the board. As it can be seen in fig. 22 showing the layout of one of the PCB internal layers, each pair of mirrored chips accesses the bus signals through a common via and a bus stub.

As shown in fig 21, the bus backbone crosses the FEC over the full width. To preserve the signal integrity the bus is implemented with controlled-impedance lines buried between two power layers. The control lines are active low and, therefore, are terminated with pull-up resistors. All the bus lines are accessible, for test purposes, via test pads.

2.4 GTL Transceivers

The ALTRO chip is supplied at 2.5V and has to be interfaced with 2.5V LVCMOS signals. In the FEC the ALTRO chips are interfaced to the bus transceivers, the GTL16612 (18-bit GTL/GTL+ to LVTTL bi-directional universal translator) and the GTL2005 (Quad GTL/GTL+ to LVTTL bi-directional translator) from Philips Semiconductors. These devices are designed and qualified by the manufacturer to work with a power supply in the range 3.0V to 3.6V. For this reason, an exhaustive test of the selected devices was conducted to verify their behaviour and long-term reliability, when operated with a supply voltage of 2.5V. As shown in section 5, these tests have shown a good behaviour with a power supply as low as 1.9V up to a frequency of 100MHz (the GTL transceivers will run in the ALICE TPC application at the maximum frequency of 40MHz).

2.5 Board Controller

The Board Controller (BC) is implemented in a FPGA (ALTERA ACEX EP1K10TC144-3). The choice of a programmable device is motivated by the need of changing the BC's functions according to the system needs that might change in the future. The FPGA uploads its configuration program from an EPROM (EPC1441). However different configuration schemes are being evaluated in case the EPROM would turn out to be sensitive to the radiation levels predicted for the ALICE TPC.

The BC functions are mainly the monitoring and diagnostic of the behaviour of the FEC. Besides, it has to control the GTL transceivers and the voltage regulators, and monitor the board temperature, the two main input voltages (+4.3V and 3.3V) and the corresponding currents. The latter functions are implemented by reading a 4-channel 10-bit ADC with an embedded temperature sensor (AD7417 from Analog Devices). The circuit that implements the measurement of the voltage and currents is sketched in fig.16 (DRAWING 4).

2.6 Power Supply

As mentioned in section 1, the FEC is powered by means of 4 power cables bearing 2 supply voltages (+4.3V, +3.3V) and their corresponding ground signals. From the 2 main supply voltages, 5 supply voltages are derived and distributed: 1) +3.3V for the PASAs (MIC29371-3.3BU); 2) +2.5V for the ADCs of the ALTRO chips (MIC29151-2.5BU); 3) +2.5V for the digital circuits of the ALTROs chips (MIC29301/501-2.5BU); 4) +2.5V for the FPGA, the GLT transceivers and the clock drivers (MIC1265); 5) +3.3V for the FPGA configuration EPROM and the ADC dedicated to the board monitoring (MIC1173).

All the voltage regulators feature a power-mode that is remotely controllable. The on/off pins of the voltage regulators are controlled via the BC, which monitors the current supplied by each voltage regulator. It can be programmed to power-down the sections

where the monitored quantities exceed a given upper limit. It should be noticed that the voltage regulators automatically switch off if any of the following conditions occurs: over temperature, low voltage in input or excessive load in output.

The RCU has also the possibility to control the on/off state of each of the FEC voltage regulators through the BC. However in case a failure occurs in the BC itself, the RCU has the possibility to control the on/off state of the FEC by means of a dedicated point-to-point line connected to an on board power switch (*Main Switch*). As it can be seen in fig.16 (DRAWING 4), the FEC *Main Switch* is mainly based on 2 monolithic transistors with a low saturation voltage (FZT1149A from Zetex).

2.7 Clock Distribution

The FEC runs with two independent clock signals: the sampling clock (SCLK) and the readout clock (RCLK). The SCLK, which has a frequency in the range 5-10MHz, is distributed to the ALTRO chips and, for monitoring purposes, to the BC. The RCLK, which can run up to 60MHz, is distributed to the ALTRO chips and the BC and synchronizes all the communications between the FEC and the RCU. Both clock signals, which are distributed to the FECs by the RCU, have to be internally distributed preserving the signal integrity and without introducing a significant jitter. In this concern the SCLK, which affects directly the ADC resolution, calls for more stringent requirements with a maximum allowed jitter of about 100ps.

The sampling clock is distributed to the FECs with a point-to-point connection by a single-ended low-impedance transmission line. The signal is input into the FEC via a LEMO connector and terminated to ground at the input of a clock driver chip (MPC940L/MPC9109FA). The clock driver chip fans out the signal to the 8 ALTROs and to the BC through individual 50Ω impedance lines with an AC-parallel termination to ground. Since the clock signal might be present even when the card is off, a diode is connected in series with the power supply of the chip to prevent the signal current to reach the board supply plane.

The RCLK is distributed to the FECs via the GTL bus. Inside the FEC the RCLK is distributed by the same type of clock driver used for the SCLK. However, the termination is done with a 22-Ω series resistor. This termination scheme allows reducing the power consumption, with respect to a parallel termination scheme, while preserving a signal quality that is sufficiently good for the RCLK.

3. Printed Circuit Board

In order to match the position of the connectors in the readout chambers the FEC has to have a width (W) of 186mm. Moreover, in order to fit into the available space, the FEC height (H) and thickness (T) should not exceed 300mm and 2mm respectively. These requirements are satisfied by the FEC final design, which features the following dimensions: W=186mm, H=155mm and T=1.68mm.

As sketched in fig.4, the PCB has 8 layers of copper interleaved with different dielectric materials (FR4 and Polyester) with different thickness. 4 layers are for the routing of the signals and the other 4 are dedicated to the distribution of the supply voltages (2 ground layers and 2 supply layers). The 4 power layers have essentially the same geometry. As an example we show in fig.20 the layout of one of the ground planes.

The duplication of the power and ground layers provides the following advantages: 1) it eases the implementation of the high number of controlled-impedance lines; 2) it reduces the voltage drop over the power layers; 3) it reduces the noise produced by the ground bouncing.

From the power supply point of view the board is divided in three main sections: the PASA section, the ALTRO/ADC section and the digital section. Therefore, as can be seen in fig.20, each power layer consists of three different power planes. The ALTRO/ADC power plane and the digital plane, which are supplied by the same input voltage (+3.3V), are closed together at the input of the voltage regulators. The ground layers have a similar geometry. However, in this case the three ground planes (PASA ground, ALTRO/ADC ground and digital ground) are closed together with a pad, which is located upstream the voltage regulators. A pin that puts the FEC ground in contact with the detector ground is soldered on the pad.

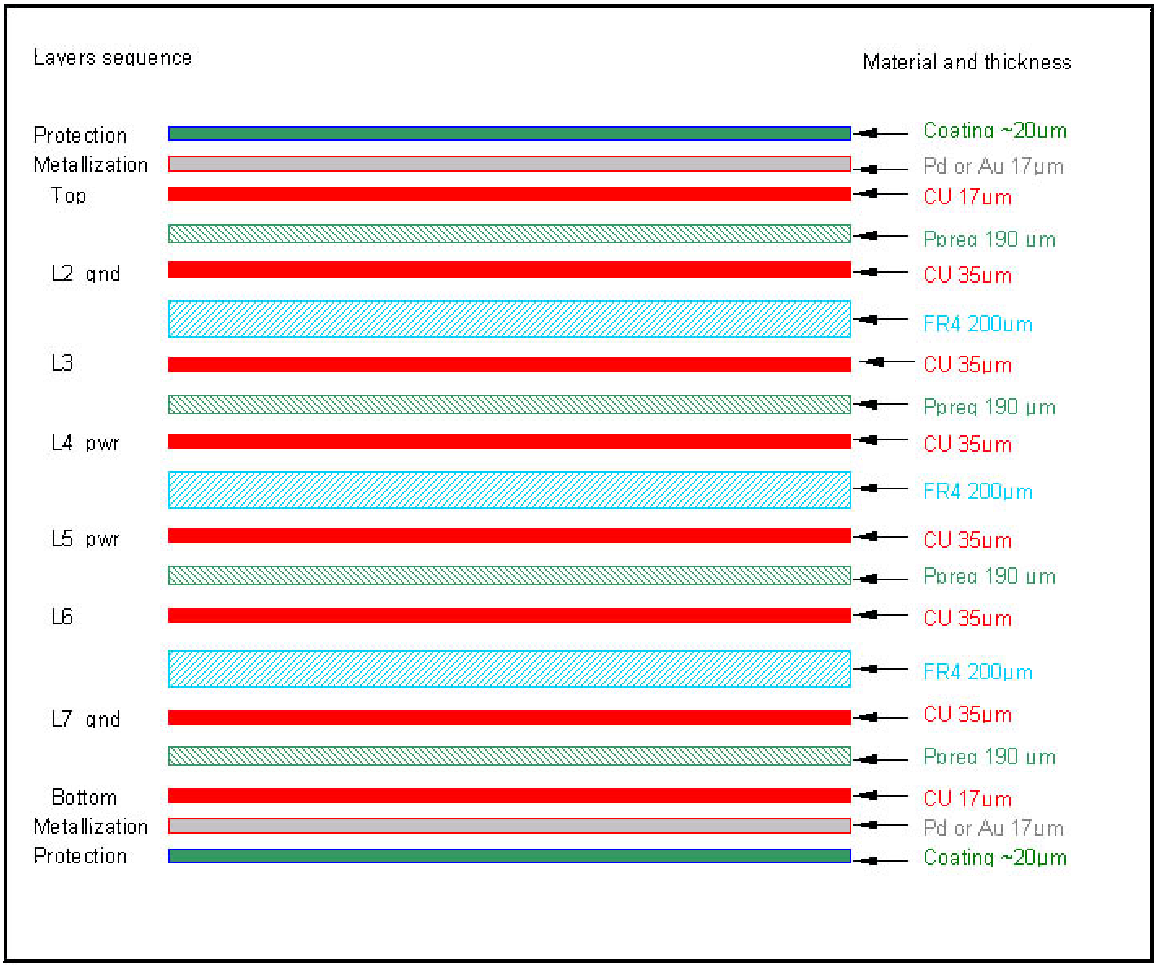


Fig.4. Cross section of the FEC printed circuit board. The PCB has a thickness of 1678µm and is the manufactured in class 5.

The connection lines between the PASA and the ALTRO chips are routed on the top and bottom layers (fig. 19 and 23), with each line always on the same layer. On the contrary, half of the connections between the front-end connectors and the PASAs are routed on two planes through vias, since the PASAs are placed on the top and bottom layers while the front-end connectors all on the top layer.

The 3rd layer of the PCB is dedicated mainly to the ALTRO bus signals: these are all implemented as 50Ω controlled-impedance lines (see fig.21). The bus stubs that connect the ALTRO chips and the GTL transceivers to the bus are routed in the 6th layer (fig.22).

4. Power consumption

While some of the FEC's components, e.g. the PASAs, have a constant power consumption, some other components, like the ALTROs, have a power consumption that varies according to their mode of operation. Therefore, in the power consumption estimates we will consider, hereafter, the average and peak values.

4.1 PASA

The PASA chips have a single supply voltage (+3.3V, GND) and a constant power consumption of 12mW/ch. The currents and power of the PASA chip are summarized in tab.1.

		CURRENT (mA)	POWER (mW)
ANALOGUE (+3.3Volts)	CHANNEL	3.64	12
	FEC (128 channels)	465	1536

Tab.1: current and power dissipated by the PASA chips.

4.2 ALTRO

The ALTRO chip requires two independent supply voltages, both with a value of 2.5V, and their corresponding ground lines: one for the 16 ADCs and the other one for the rest of the chip. Although imprecise, for simplicity, we will refer to these two power supplies as *analogue* and *digital* respectively.

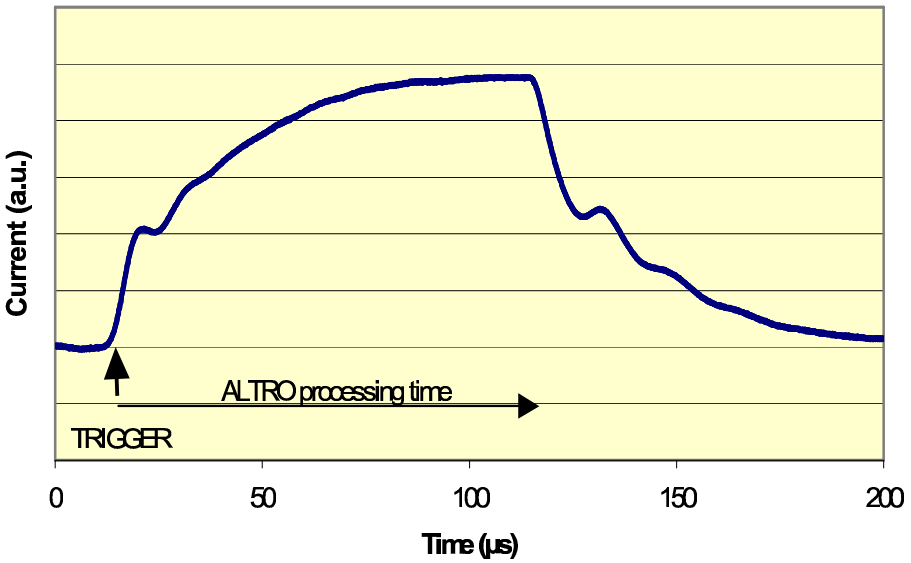


Fig.5 Time profile of the ALTRO power consumption during the signal processing.

Since the ADCs are continuously sampling, the *analogue* power consumption is constant and equal to 12mW/ch (for a sampling rate of 10MSPS).

On the contrary the *digital* power consumption depends on the mode of operation of the chip. It goes from a minimum, when the chip is in the idle state (standby), and reaches the maximum when, upon arrival of the trigger signal, it starts to process and store the input signals in the data memories. Fig. 5 shows the time profile of the ALTRO power consumption when the chip receives a trigger and starts processing a realistic signal. Tab.2 list the values of the *digital* power for the different modes of operation of the chip.

MODE OF OPERATION	POWER /CHANNEL (mW)
STANDBY Sampling clock 10MHZ, Readout clock 33MHz	3.8
PROCESSING MODE I Processing chain disabled Pedestal memory disabled	9.4
PROCESSING MODE II Pedestal memory enabled Filter enabled Zero suppression disabled Realistic pattern (50 occupancy)	14.8
PROCESSING MODE III Pedestal memory enabled Filter enabled Zero suppression disabled Worst case pattern (unrealistic)	20.3

Tab.2. *Digital* power consumption of the ALTRO chip for different modes of operation.

The *analogue* and *digital* currents and power for the ALTRO chip are summarized in Tab. 3.

		CURRENT /FEC (mA)	POWER/FEC (mW)
ANALOGUE (+2.5Volts)	AVERAGE	614.4	1536
	PEAK	614.4	1536
DIGITAL (+2.5Volts)	AVERAGE	256	<640
	PEAK	768	1920

Tab.3. Current and power dissipated by the ALTRO chips.

4.3 Polarization circuit

The circuit that provides the reference voltages to the PASA and ALTRO chips is supplied by the analogue power supply (+3.3V) and has a constant power consumption of 5.5mW.

4.4 Clock drivers

The clock drivers are supplied at 2.5V. This supply voltage is derived form the main digital supply voltage by a voltage regulator. The same regulator supplies also the FPGA (board controller). The current and power for the two clock driver chips are summarized in tab. 4.

	CURRENT (mA)	POWER (mW)
ADC CLOCK (10MHZ)	150	375
R/O CLOCK (40 MHz)	50	125

Tab.4. Current and power dissipated by the clock driver chips

It should be noted that the clock driver for the sampling clock (10MHz) dissipates more than the clock driver for the readout clock (40MHz) because of the different termination of the clock lines.

4.5 Bus transceivers

The GTL transceivers have a different power consumption depending on whether they are driving in the GTL-to-LVCMOS direction (*writing FEC*) or vice versa (*reading FEC*). Moreover, the power consumption is yet different when the GTL lines are not driven at all (*standby*). Part of the power is dissipated in the transceivers chips themselves and part in the termination of the bus lines. The current and power dissipated by the GTL transceivers in the three different states are summarized in tab. 5.

	MODE	CURRENT (mA)	POWER (mW)
TRANSCEIVERS	Standby	16.8	42
	Writing FEC	66.8	167
	Reading FEC	16.8	42
Bus termination	Not driven	0	0
	Driven to 0	30/line	45/line
	Driven to 0	227 / FEC	250 / FEC

Tab.5. Current and power dissipated by the GTL transceiver chips

4.6 EPC1441

The configuration EPROM for the FPGA, which implements the board controller, is supplied at 3.3V. This device together with the monitoring ADC has a power consumption of 4mW.

4.7 FEC total power consumption

For the calculation of the total power consumption the voltage drop across the regulators and the main switch has to be considered:

- Volt. Regulator for the 3.3 V: $V_{IN} - V_{OUT} = 450mV$
- Volt. Regulator for the 2.5V: $V_{IN} - V_{OUT} = 500mV$
- Main Switch: $V_{IN} - V_{OUT} = 100mV$

The overall FEC power consumption is summarized in tab.6, which lists the average and peak values for the currents and power, for the two supply voltages, and the total power consumption.

VOLTAGES	AVERAGE		PEAK	
	current (A)	power (W)	current (A)	power (W)
2.5 V	1.1	3.6	1.6	5.3
3.3 V	0.47	1.9	0.47	1.9
Total	1.6	**5.5**	2.1	**7.2**

Tab. 6. Average and peak values for the current and power of the FEC

5. Measurements

In this section we report some of the measurements done on the FEC. Figs 6 and 7 show the quality of the ALTRO bus signals. Fig 8 shows the quality of the SCLK and RCLK respectively. Fig. 9 shows the measurement of the impulse response function of the PASA embedded in the FEC. Figs 10 to 12 refer all to measurement done with the FEC connected to the TPC detector and to the rest of the readout chain. Fig. 10 shows the measurement of the pedestals. This measurement indicates that the overall noise of the FEC system is below 1 ADC count (r.m.s). Figs. 11 and 12 show clusters corresponding to a single ionisation point, as generated by the radioactive decay of the ^{83}Kr. The cluster in fig. 11 corresponds to the cluster produced by a MIP. Eventually tab. 7 summarizes the performance of the PASA embedded in the FEC. If compared with the performance of the standalone PASA, it shows that the FEC does not degrade the resolution.

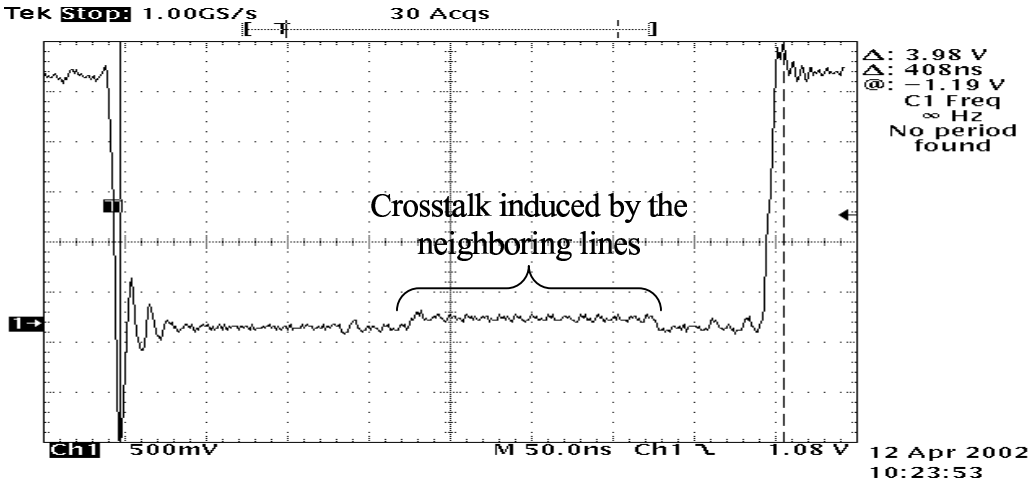


Fig. 6. Measurement of the signal in one of the FEC internal bus lines. The channel-to channel crosstalk is below 150mV.

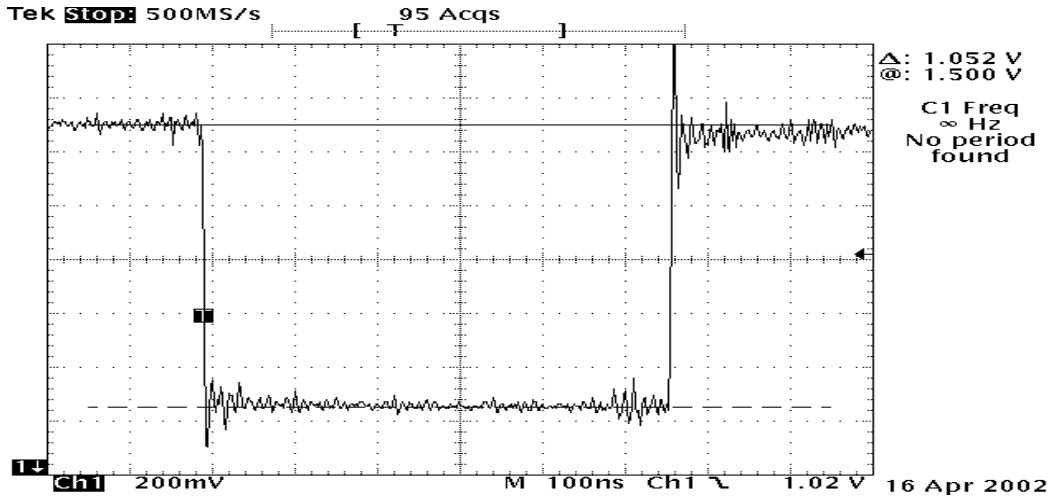


Fig.7. Measurement of the signal in one of the external GTL bus lines. The noise margin is higher than 500mV.

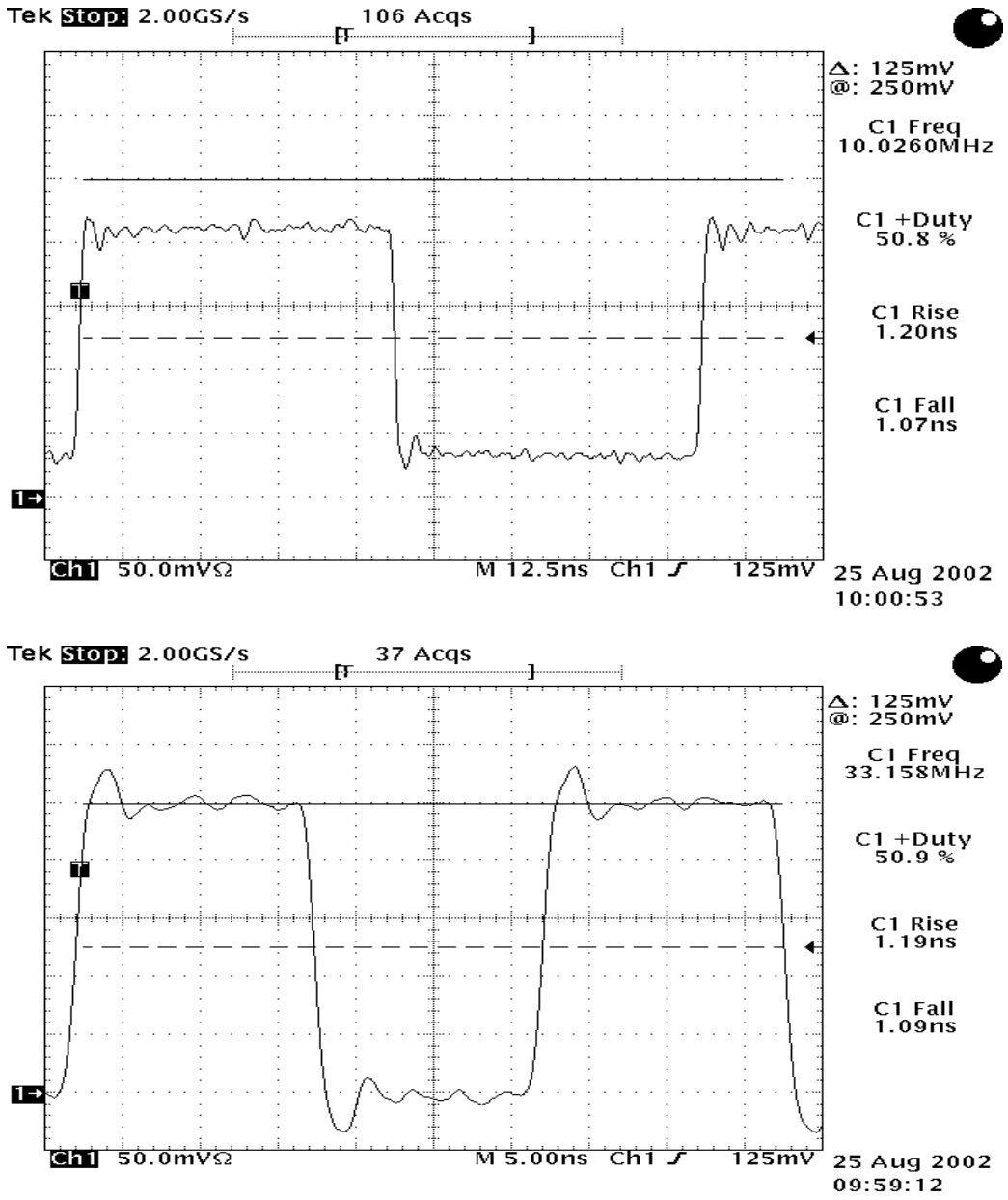


Fig. 8. Measurement of the clock signals at the input of the ALTRO chips. Sampling clock running at 10MHz (top). Readout clock running at 33MHz (bottom)

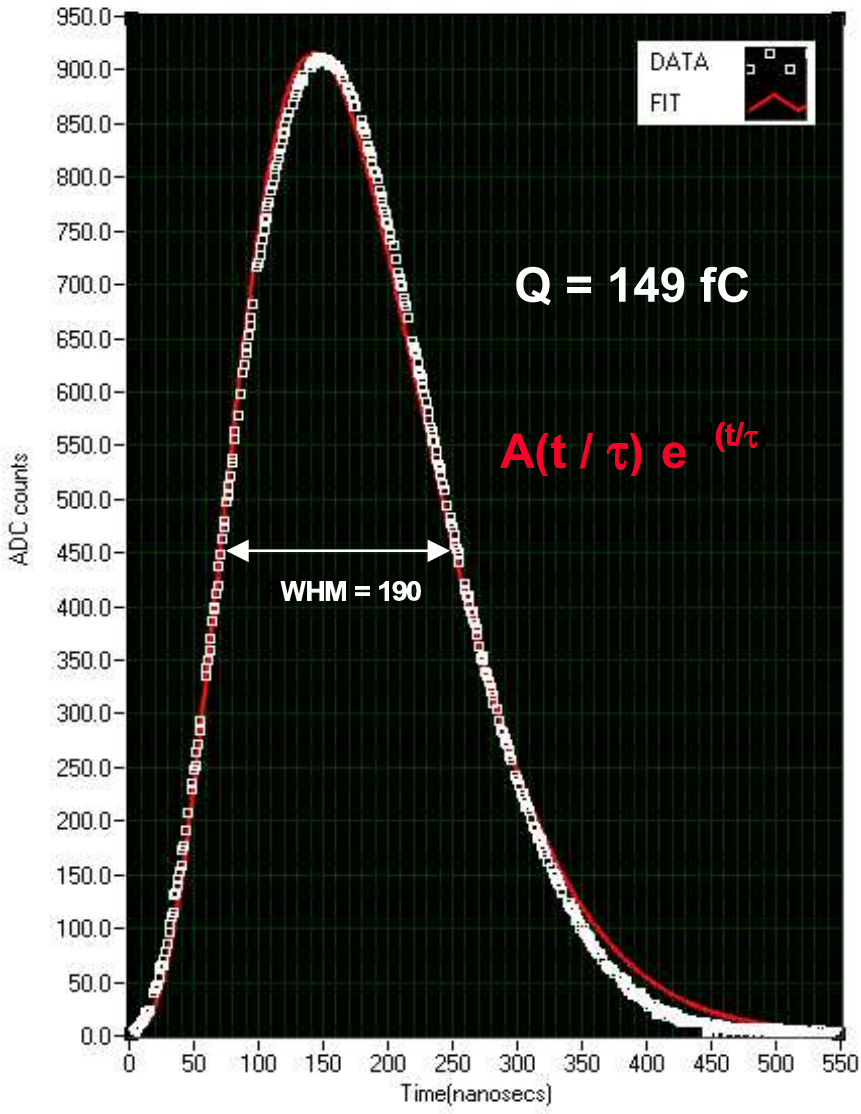


Fig. 9. Impulse response function of the PASA embedded in the FEC.

Parameter	Requirements	Measured
Noise	1000 e	(600 +23/pF) e
Conversion gain	12mV / fC	10.8 mV/fC
Shaping time	190 ns	190 ns
Linearity	<1%	<0.35%
Crosstalk	<0.3%	<0.4%

Tab. 7. Performance of the PASA embedded in the FEC.

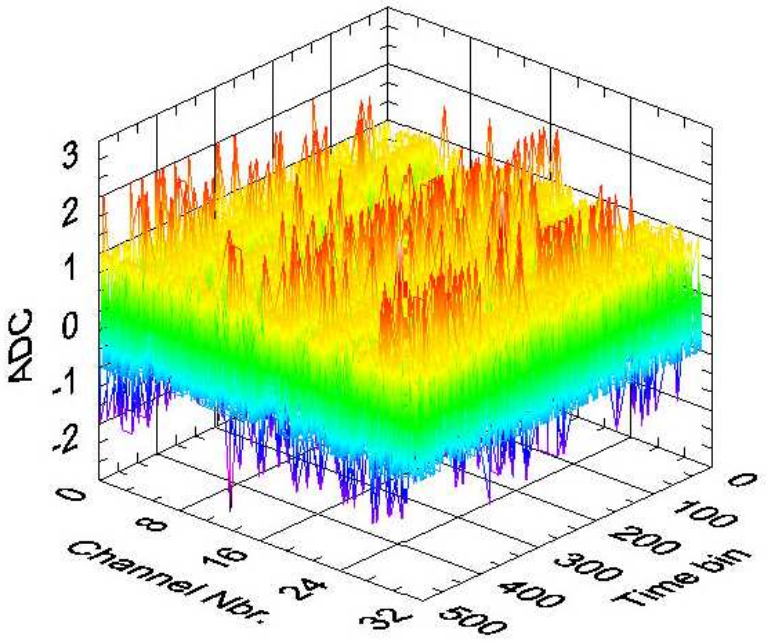


Fig. 10. Measurement of the pedestals. The plot shows the signals for 32 channels over a sampling window of 500 time bins (50μs). This measurement indicates a noise (rms) of 0.8 ADC count.

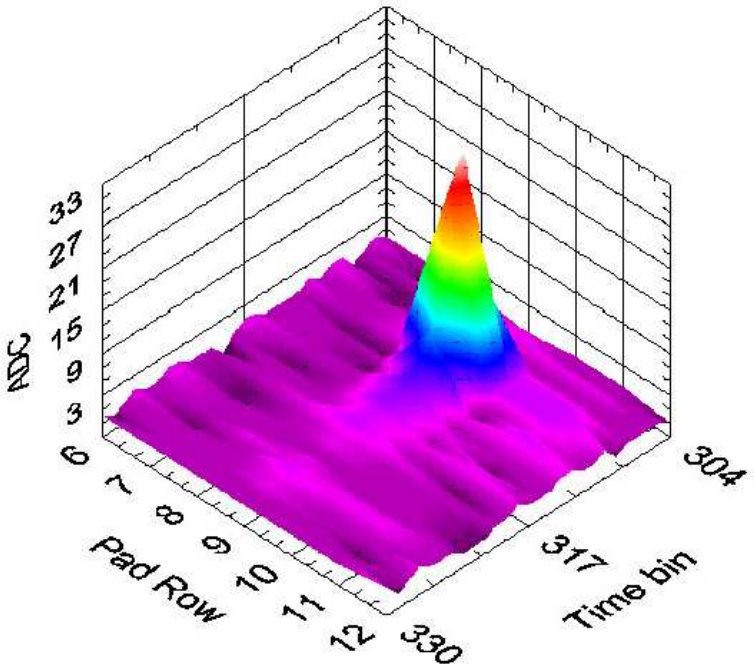


Fig. 11. Single ionisation point cluster generated by the radioactive decay of the ^{83}Kr. This cluster corresponds to a MIP.

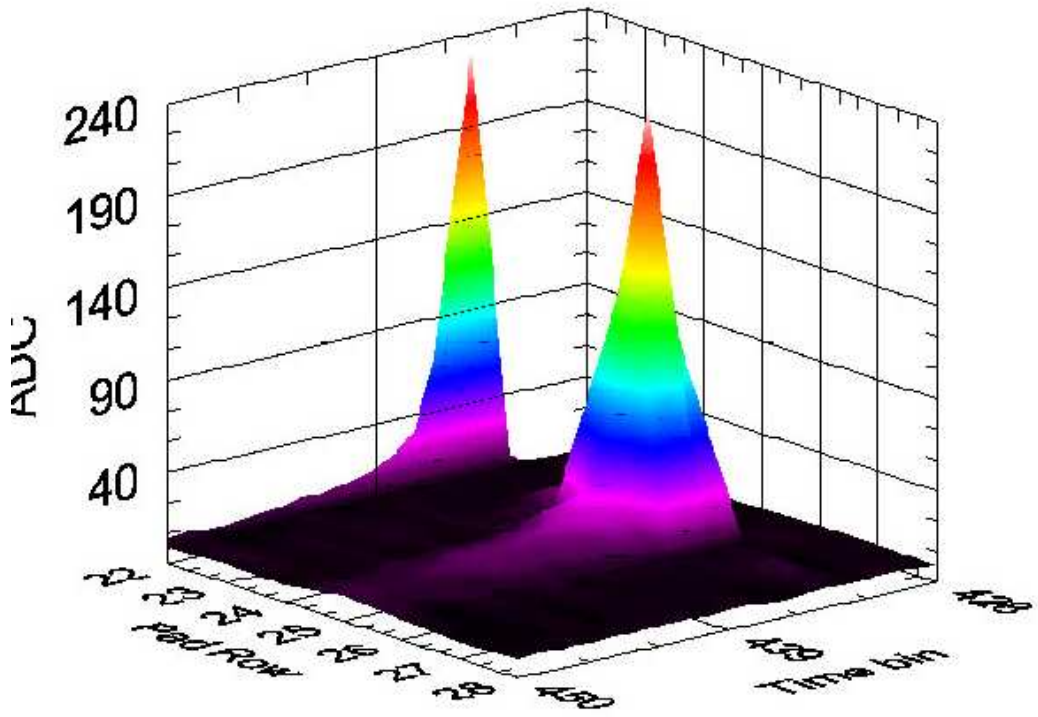


Fig. 12. Single ionisation point cluster generated by the radioactive decay of the ^{83}Kr**.**

6. Schematic Drawings and PCB layout

The figs 13-18 show the FEC schematic diagrams. The design is organized in a two-level hierarchy and implemented with the Concept, Schematic Editor of the Logic Workbench (Cadence) CAD tool.

Fig. 13 shows the design root. It contains: 1) the front-end connectors (top left); 2) the instance of the block that contains the power supplies (bottom left); 3) the instance block for the power control circuit (bottom left); 4) the 8 instances of a block that contains the ALTRO and PASA chips (middle); 5) the instance block for the board controller (middle); 6) the instance block for the transceivers (top middle); 7) the readout connectors (top right), pull-up resistors (bottom right) and a circuit that provides three reference voltages to the PASA and ALTRO chips (bottom right)

In fig.14 is the schematic diagram that contains the PASA and the ALTRO chip.

Fig.15 contains the FPGA (ACEX EP1K10-144 – ALTRA) that implements the Board Controller.

Fig.16 describes the circuit to measure the two supply voltages, their correposnding currents and the board temperature. .The circuit is based on the chip AD7417.

Fig. 17 is the schematic diagram for the voltage regulators.

In fig.18 is the schematic diagram that contains the GTL transceivers and the fan-out chips for the sampling and readout clocks.

Figs 19-23 show the layout of the 5 of the PCB layers: 4 signal layers and 1 power layer.

Fig. 13

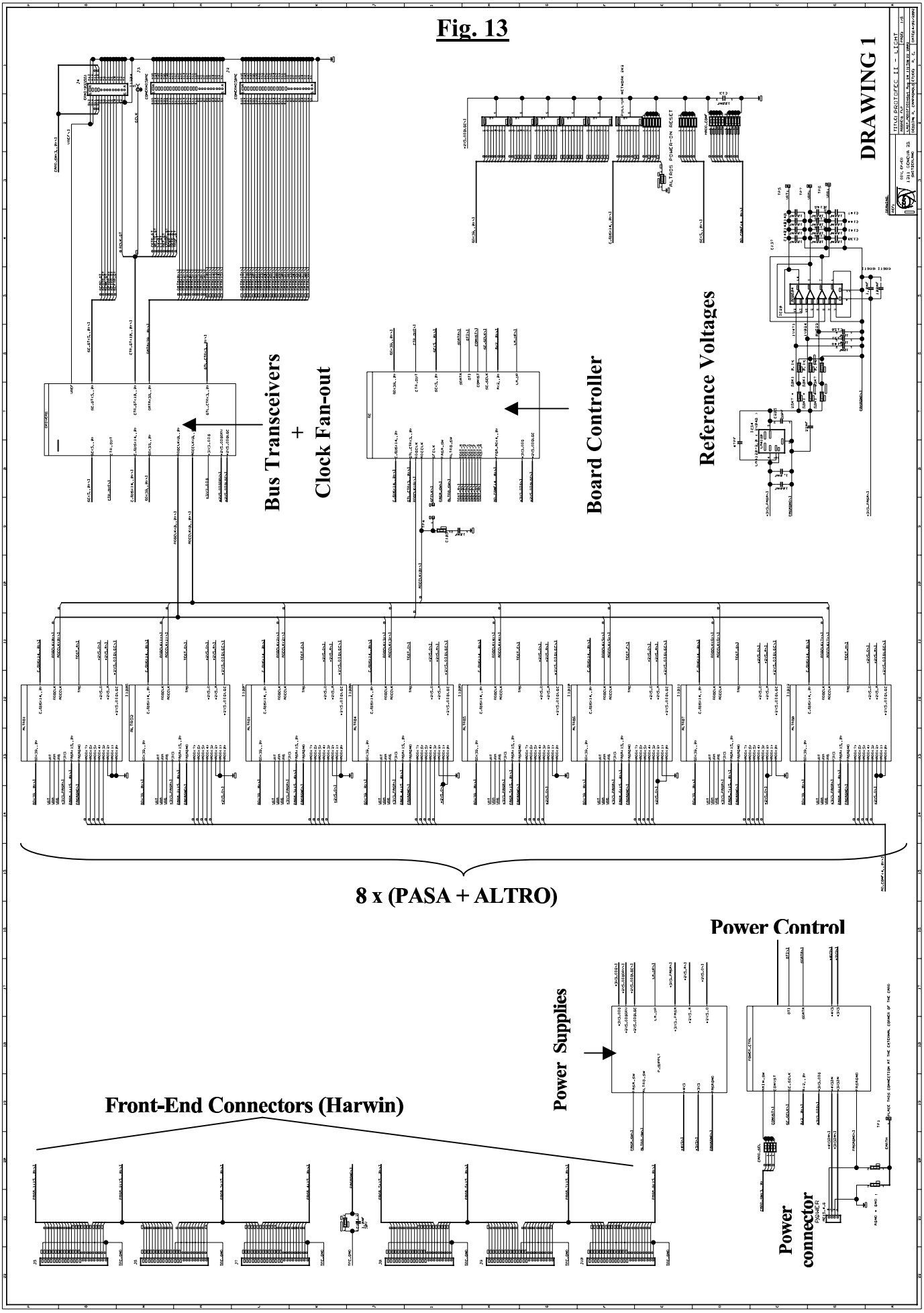

DRAWING 1
Bus Transceivers
+
Clock Fan-out
Board Controller
Reference Voltages
8 x (PASA + ALTRO)
Power Control
Power Supplies
Front-End Connectors (Harwin)
Power
connector

Fig. 14

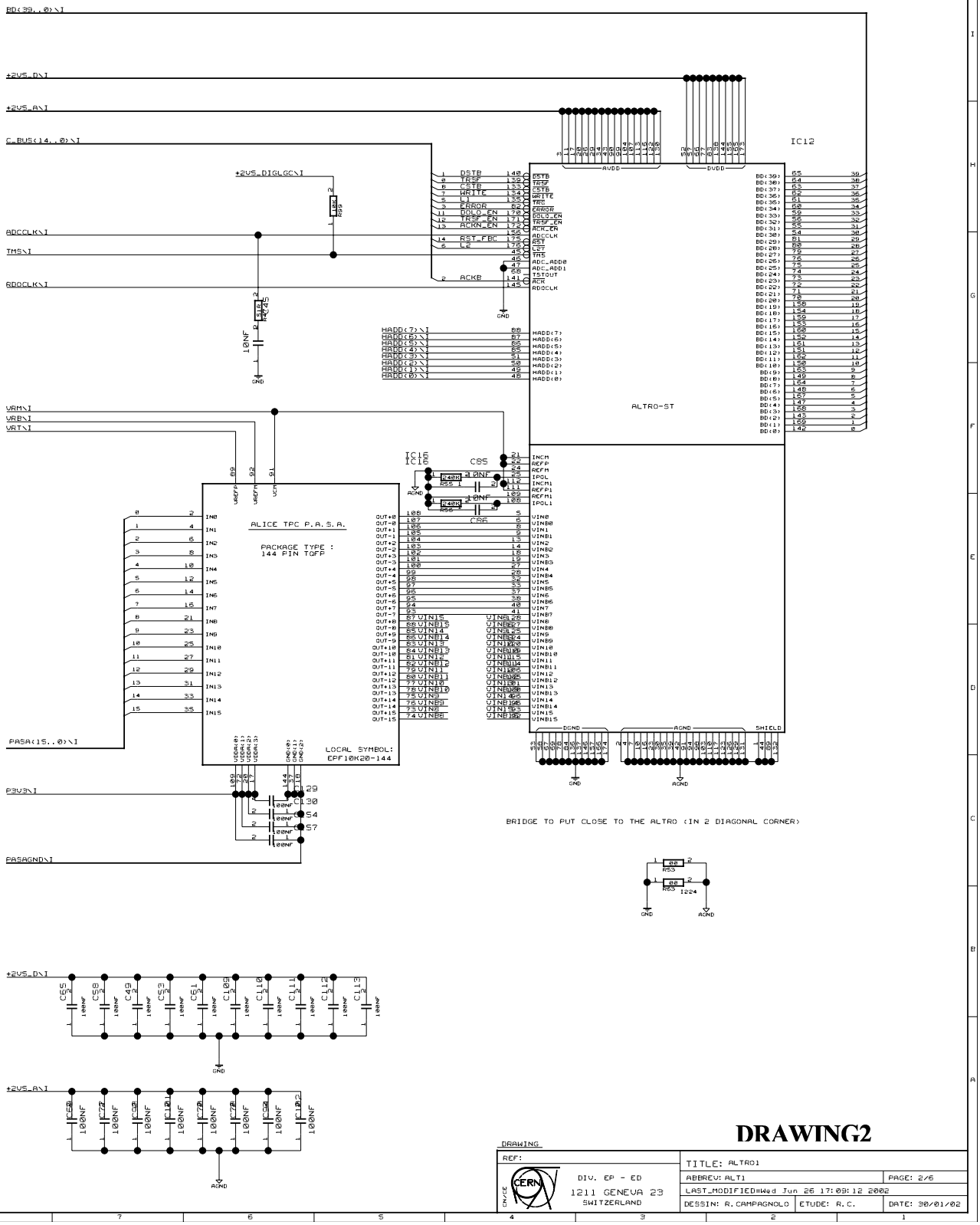
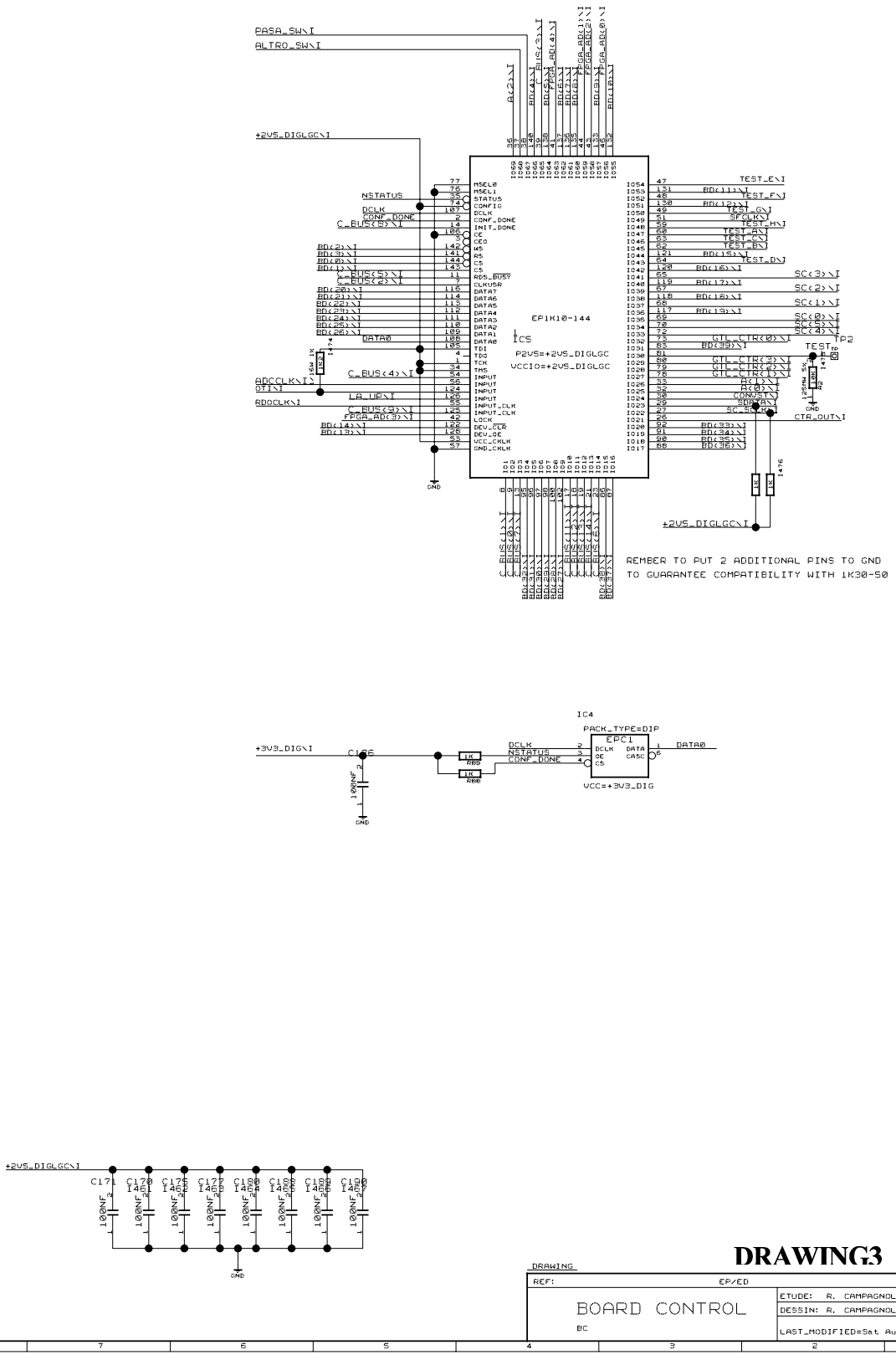

ALTRO-ST
ALICE TPC P.A.S.A.
PACKAGE TYPE :
144 PIN TQFP
LOCAL SYMBOL:
EPF10K20-144
BRIDGE TO PUT CLOSE TO THE ALTRO (IN 2 DIAGONAL CORNER)
DRAWING2
TITLE: ALTRO1
DIV. EP - ED
1211 GENEVA 23
SWITZERLAND
DESSIN: R.CAMPAGNOLO
ETUDE: R.C.
DATE: 30/01/02

Fig. 15



DRAWING3

DRAWING		
REF: EP/ED		
BOARD CONTROL	ETUDE: R. CAMPAGNOLO	PAGE: 4/5
	DESSIN: R. CAMPAGNOLO	DATE: 31/01/2002
BC	LAST_MODIFIED=Sat Aug 24 11:34:37 2002	

Fig. 16

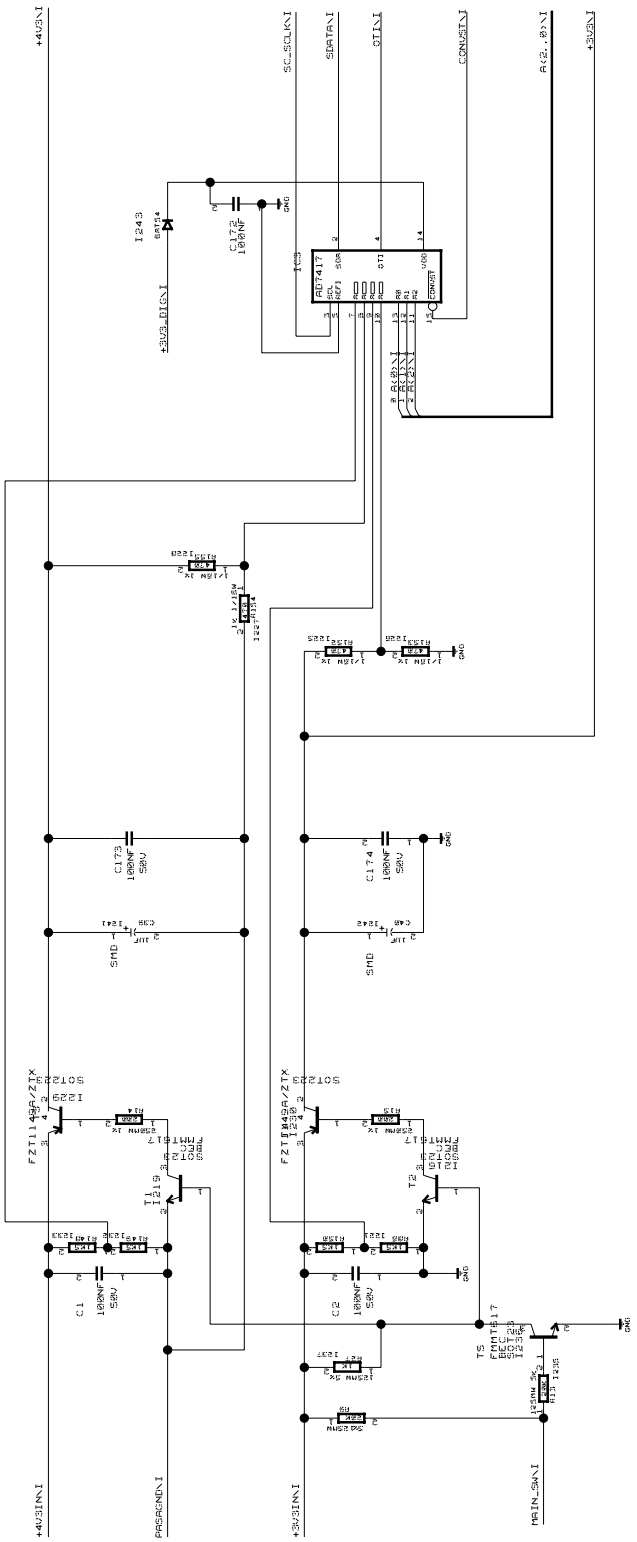

DRAWING 4
DRAWING:
TITLE: POWER_CTRL
REF:
DIV. EP/ED
1211 GENEVA 23
SWITZERLAND
ABBREV: PCTRL
LAST MODIFIED: Fri Aug 23 17:35:34 2002
DESSIN: R. CAMPAGNOLO
ETUDE: R. C.
DATE: 24/01/2003
PAGE: 2/8
+4V3N1
+3V3_DIGN1
SCL_SCLKN1
SDATAN1
GTIN1
CONVSTN1
AIN2..0N1
+3V3N1
AD7417
C172
100NF
C173
100NF
50V
C174
100NF
50V
C1
100NF
50V
C2
100NF
50V
SMD
FZT1149A/ZTX
FZT1149A/ZTX
ZMT617
ZMT617
T1
T2
T5
FMMT617
+4V3INN1
AGNDN1
+3V3INN1
MAIN_SWN1
GND

Fig. 17

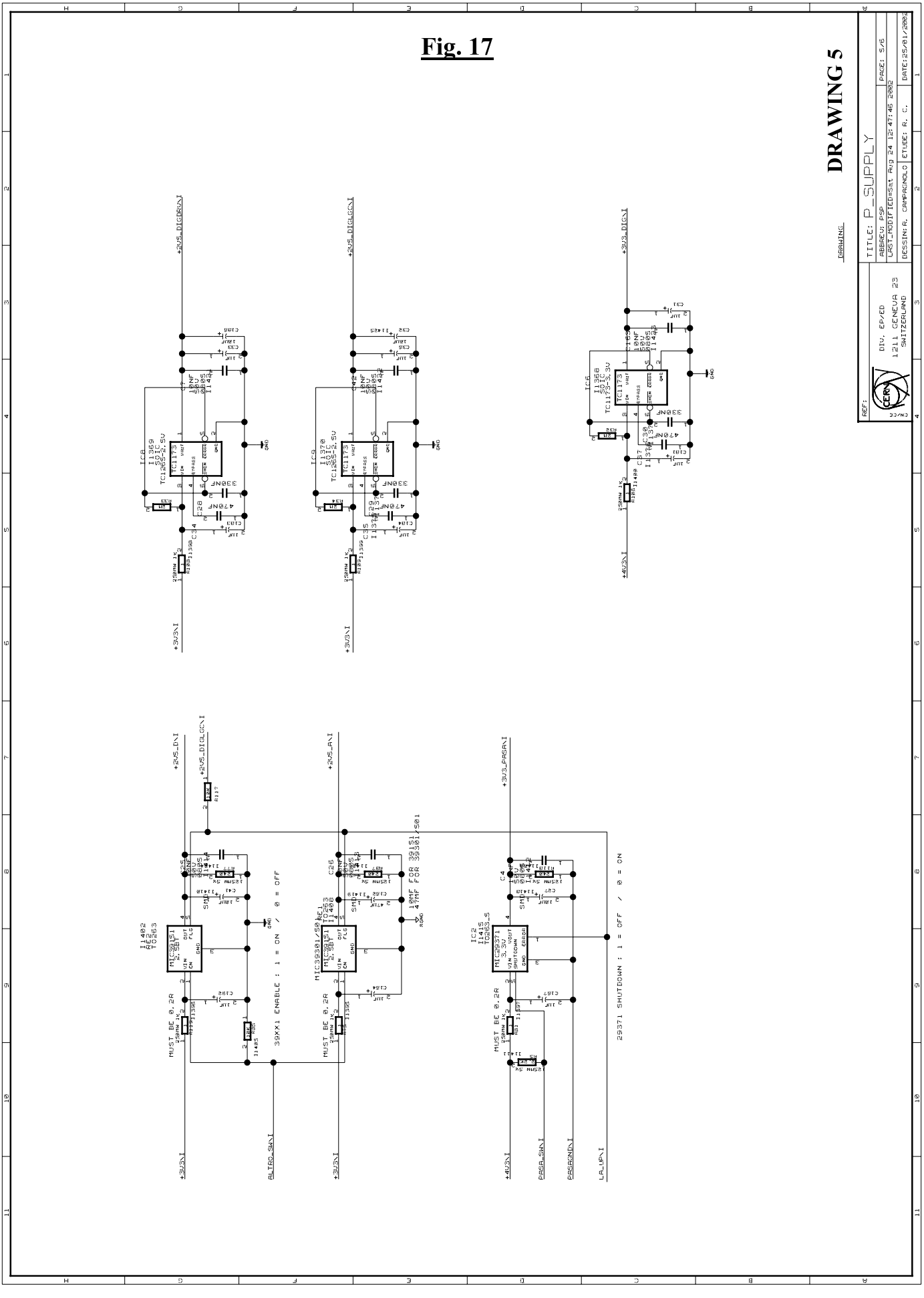
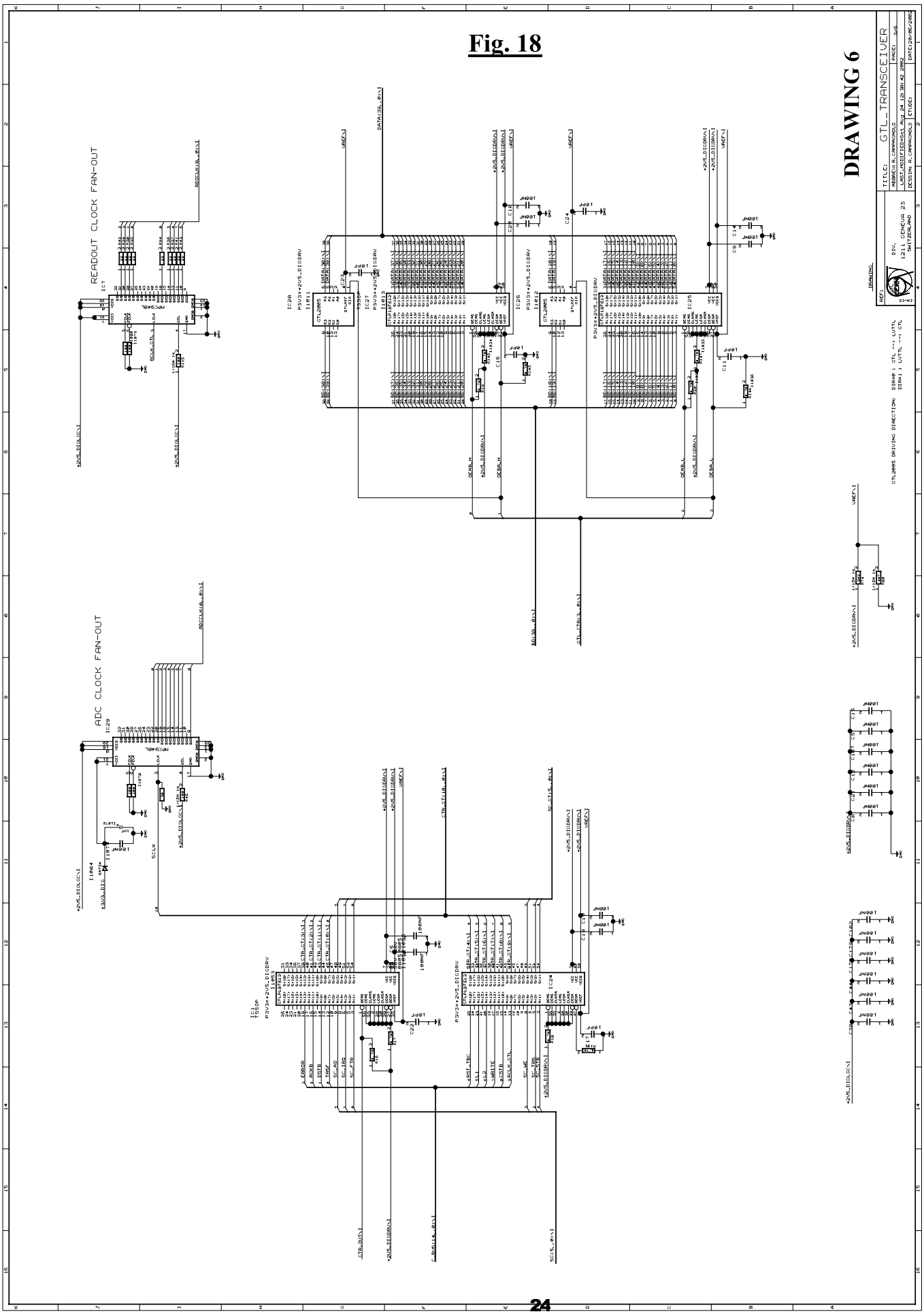

DRAWING 5
DRAWING
TITLE: P_SUPPLY
ABBREV: PSP
LAST_MODIFIED=Sat Aug 24 12:47:46 2002
DESSIN:R. CAMPAGNOLO
ETUDE: R. C.
DATE:25/01/2002
PAGE: 5/5
REF:
DIV. EP/ED
1211 GENEVA 23
SWITZERLAND
+2V5_DIGIN
+2V5_DIGLGCN
+3V3_DIGN
+3V3N
+4V2N
+2V5_DN
+2V5_AN
+3V3_PASN
ALTRG_SWN
PASR_SWN
PASRGNDN
LA_UPN
39XX1 ENABLE : 1 = ON / 0 = OFF
29371 SHUTDOWN : 1 = OFF / 0 = ON
MUST BE 0.2R
GND

Fig. 18


DRAWING 6
READOUT CLOCK FAN-OUT
ADC CLOCK FAN-OUT
TITLE: GTL_TRANSCEIVER
AUTHOR: R.CAMPAGNOLO
LAST_MODIFIED: Fri 24 12:38:42 2000
DESIGN: R.CAMPAGNOLO
DATE: 20/05/2005
PAGE: 1x6
DIV. 211 GENEVA 23 SWITZERLAND
GTL_DRMS DRIVING DIRECTION: DIR=0 : GTL --> LVTTL
DIR=1 : LVTTL --> GTL

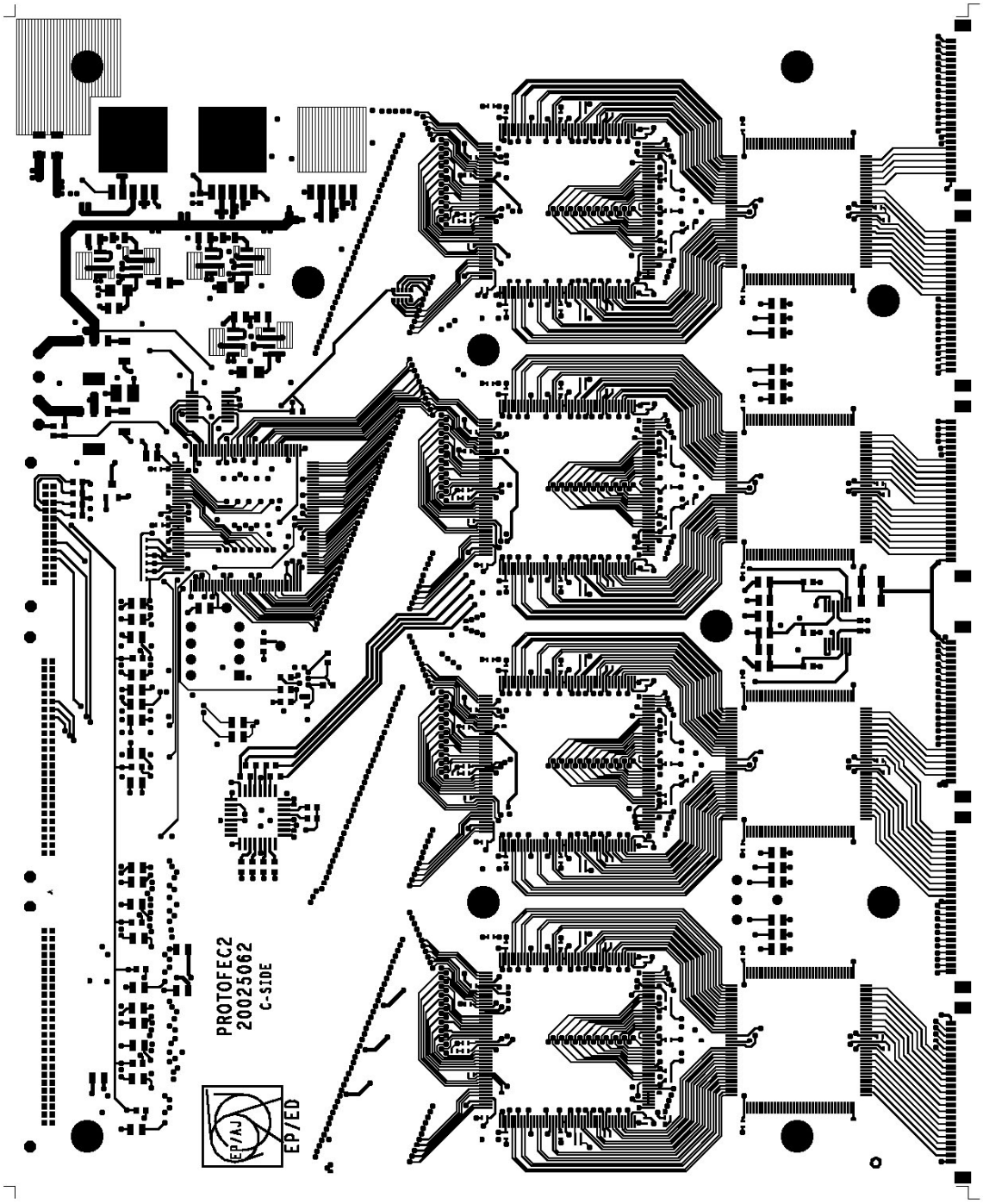


Fig.19. PCB layout: top layer.

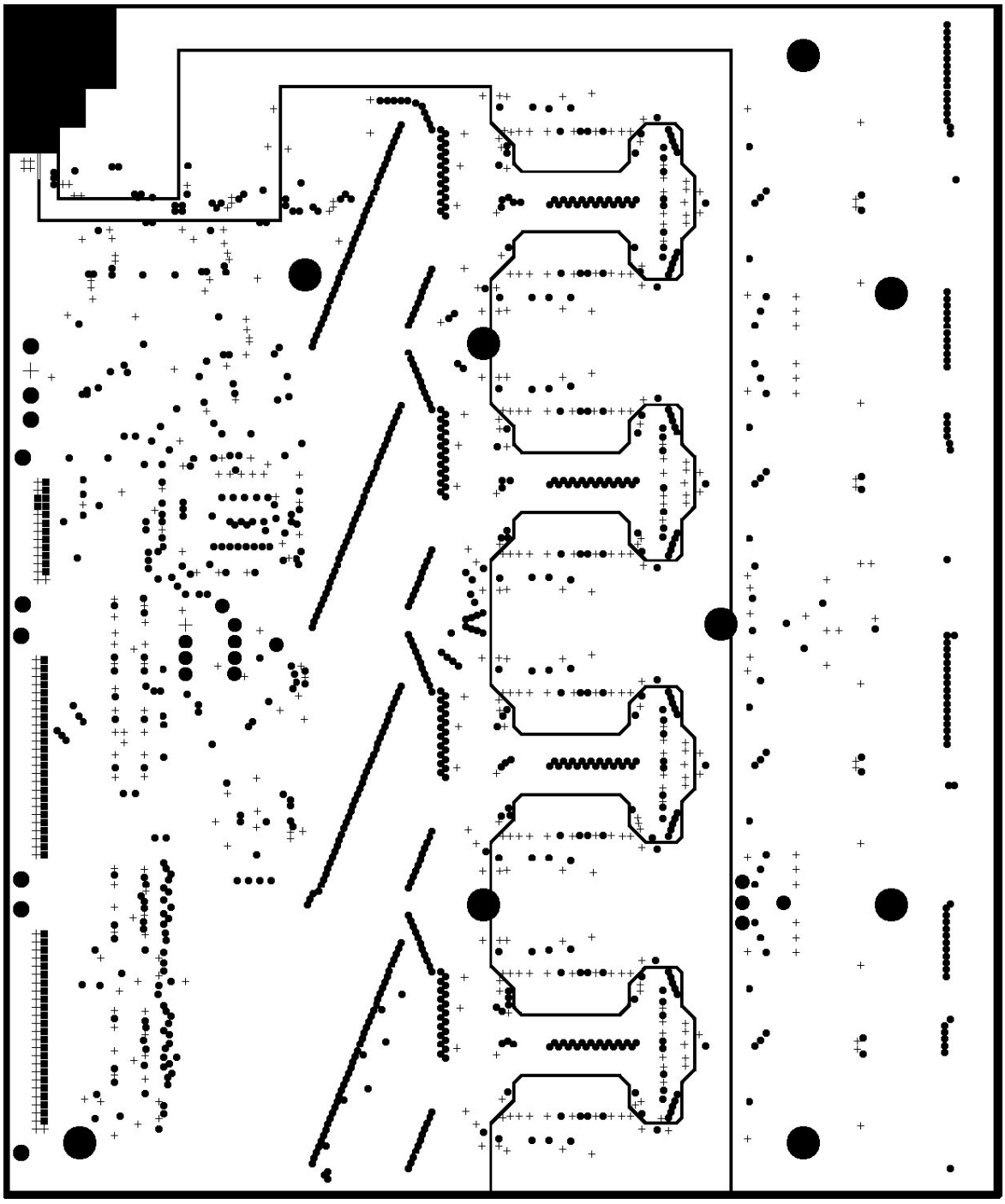


Fig. 20. PCB layout: ground layer.

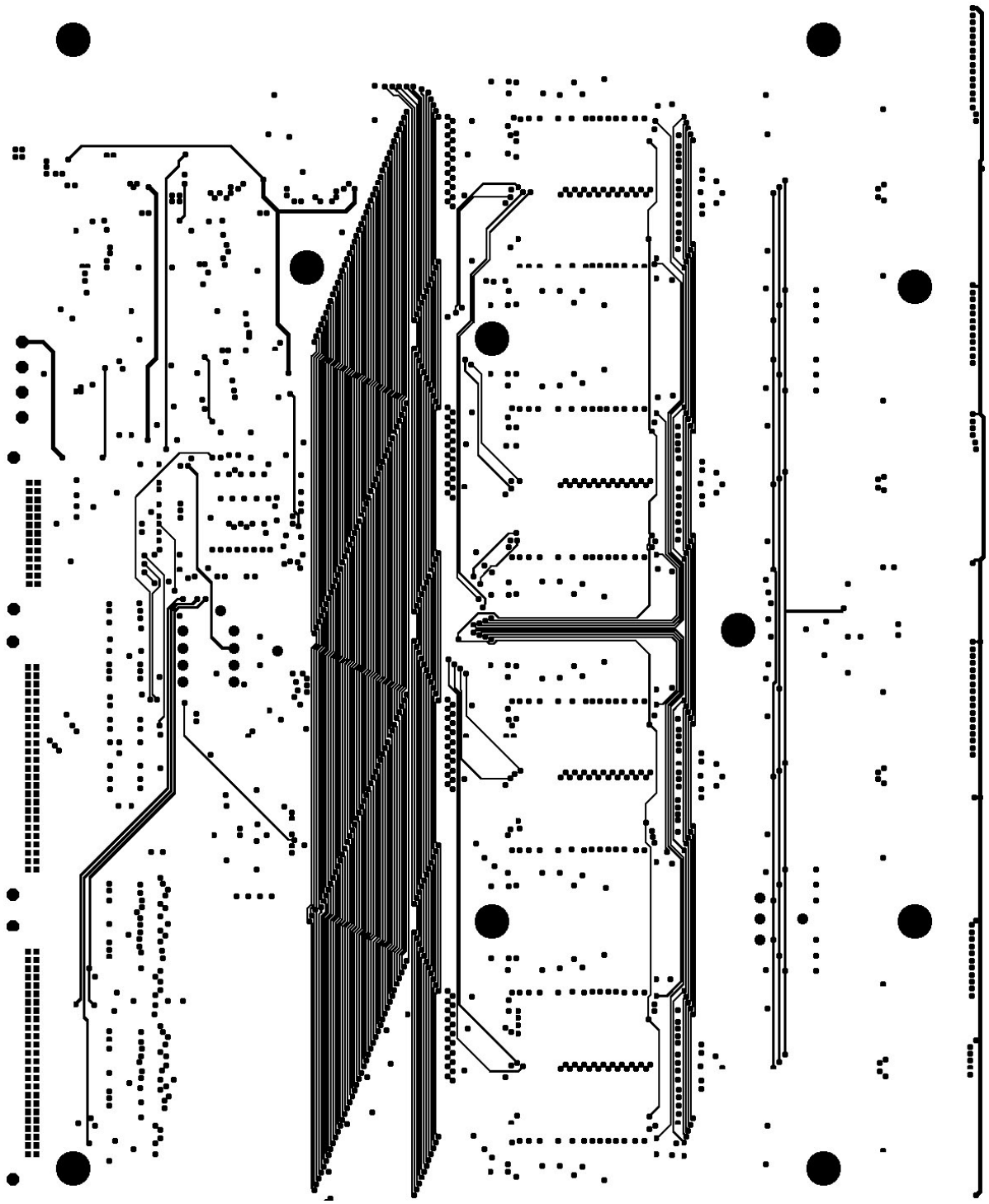


Fig. 21. PCB layout: layer 3.

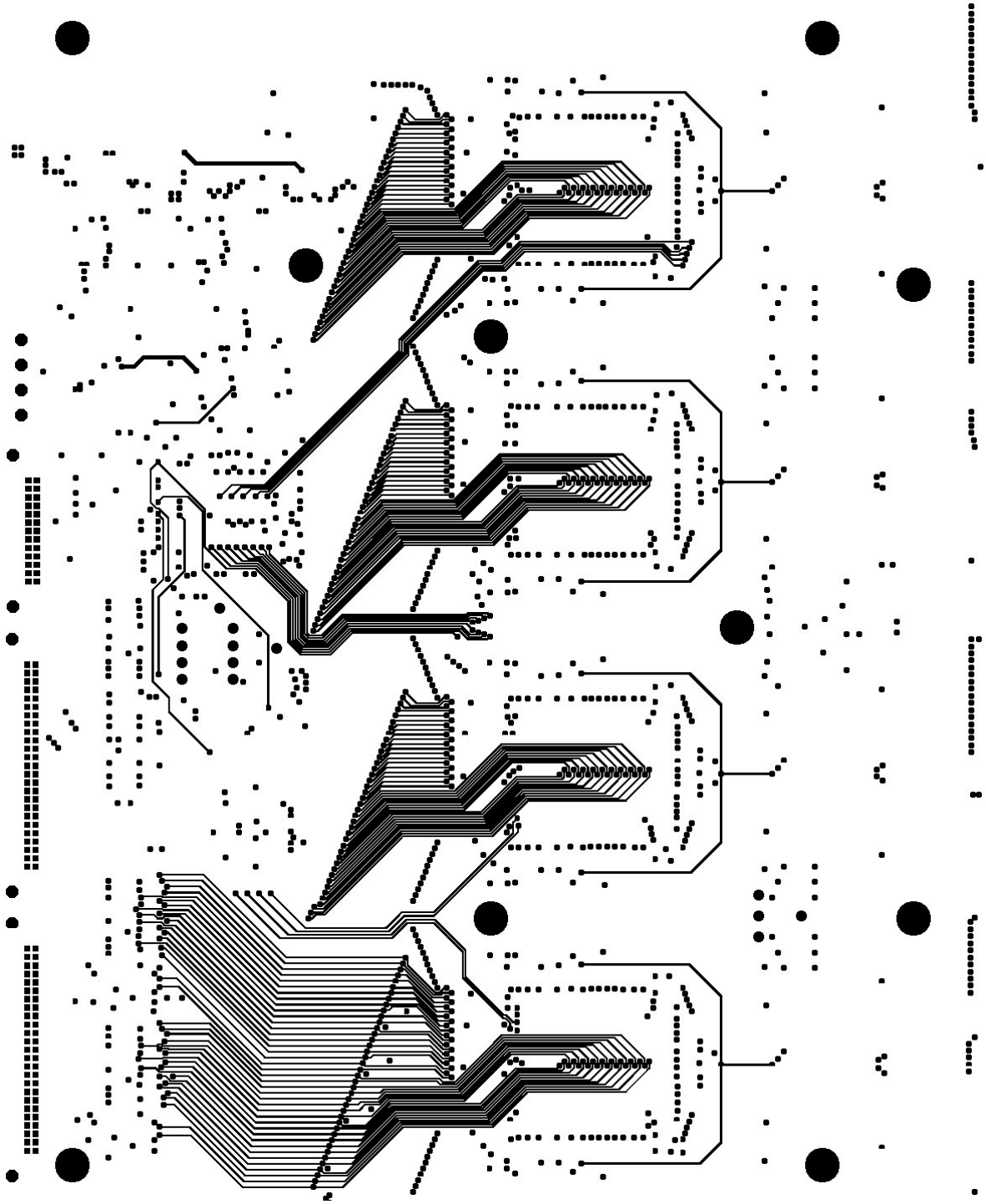


Fig. 22. PCB layout: layer 6.

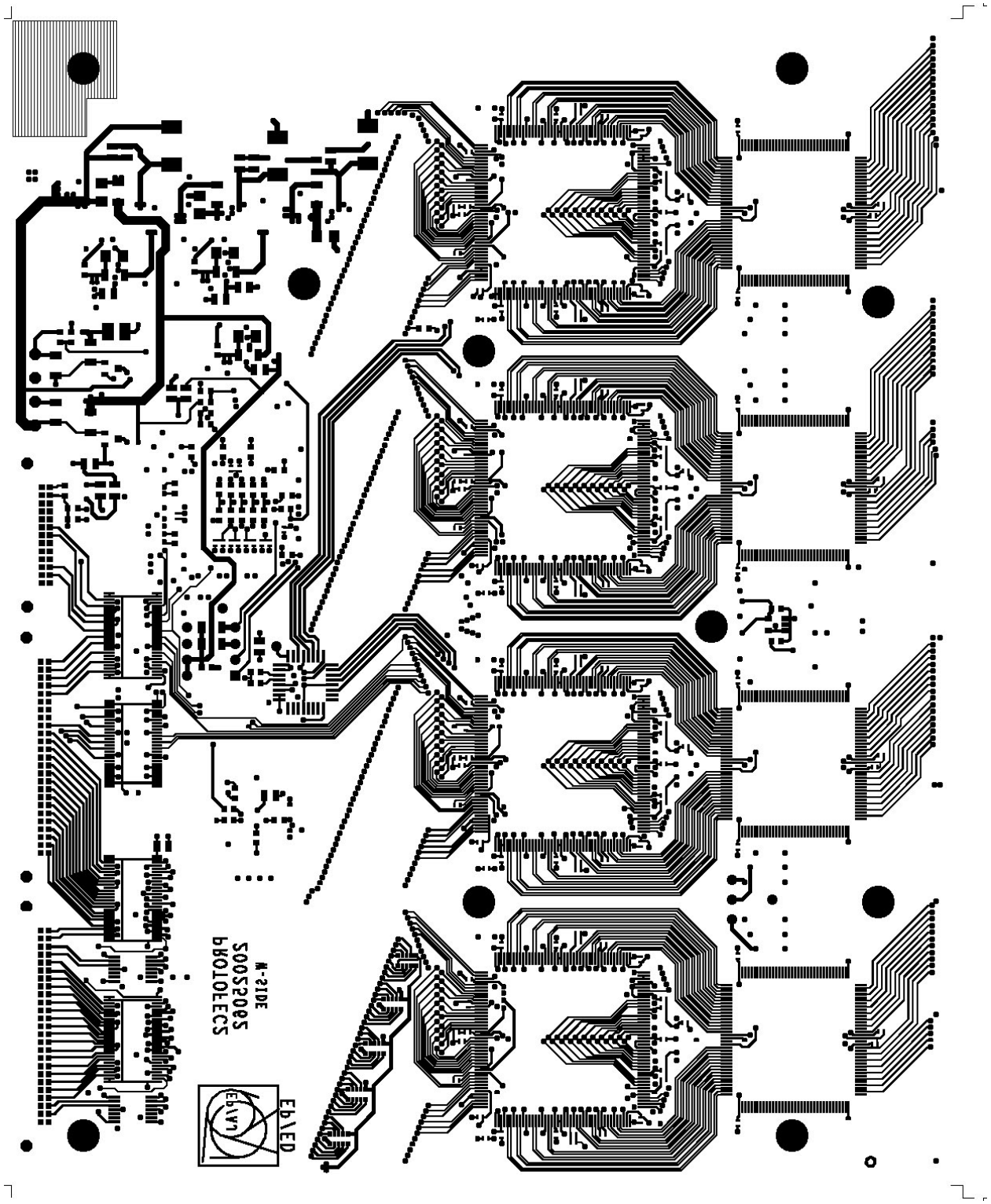


Fig. 23. PCB layout: bottom layer.

References

[1] ALTRO bus specifications
[2] ALTRO User Manual