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The Control Network (Slow Control) for the ALICE TPC Front-end Electronics

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DRAFT 0.1

Overview

The Control Network establishes a dedicated bus connection between the Readout Control Unit (RCU), [1], and the Board Controller (BC) in each Frontend Card (FEC), [2], in view of monitoring and controlling the FECs. This Control Network is based on the I^2C transmission protocol [3] with an extra line (INT) for handling interrupts from the FECs. It is also fully independent from the ALTRO bus and consists of three lines: two required from the I^2C protocol (SDA and SCL) and the INT line for issuing interrupts. In normal conditions the RCU uses the Control Network to read and write registers in the BC of a specific FEC. These registers contain information related to voltage and temperature probing, protocol and multi-event buffer errors and statistical data. Their complete description is given on the following chapters. The interrupts are sent via the INT line in the case any error conditions is detected. The Error Logbook contains a set of flags for each error detected by the BC. Upon the arrival of an interrupt, the RCU acknowledges it by setting the INT line LOW. The RCU should then read the Error Logbook to verify which error was generated. If the RCU wishes to investigate further the origin of the problem, it can read the related register. E.g. if the analogue current is detected to be out of the functioning range, the RCU can read its value on the dedicated register on the Temperature and Electrical Monitoring.

The first section of this document describes the main characteristics of the I^2C-bus. Section 2 focus on the Command Instructions that the RCU can send to the BC. Section 3 is dedicated to the Temperature, Current and Voltage Monitoring, section 4 focus on to the Error Logbook, section 5 treats the Statistical data gathered by the BC, section 6 describes the protocol and Buffer Monitoring.

1. The I^2C Bus

The I^2C bus [1], developed by Philips, is a transmission protocol for serial data transfer. This protocol uses only two lines: Serial Data Line (SDL) and Serial Clock Line (SCL). With these two lines a multi-master bus can be implemented, allowing simple master-slave relationships. Arbitration between several competitor masters is also supported. The I^2C bus is rather robust and is able to support up to 3.4Mbit/s in a bi-directional 8bit transfer. It is a world-wide protocol for which there is a wide range of devices available in the market. Moreover the number of devices that can be connected together depends only on the maximum bus capacitance of 400pF. Components can be added or removed from the system without any conflict.

2. Command set

The RCU can send two Reset commands via the I^2C bus to the BC for specific parts of the system. The CNTRST command resets all the counters on the BC and the BCRST resets the BC itself and all its registers. Finnaly the RERLBK resets the Error Logbook detailed in section 4. Table0 list these three commands.

Commands	
Command Name	**Function**
CNTRST	Resets all the Counters
BCRST	Board Controller Reset
RERLBK	Resets the Error Logbook

Table0. Commands

3. Temperature, Current and Voltage Monitoring

Several physical quantities, such as temperature, analogue/digital currents and voltages can be measured by a dedicated 5-channel 10bit ADC (AD7417) in the FEC. The status of the power switches and voltage regulators is also mapped in the BC. Table1 summarises the registers related with Temperature, Current and Voltage Monitoring.

Temperature and Electrical Monitoring			
Register Name	**Access**	**Function**	**# bits**
TEMP	R	Temperature	10
VOLTREG	R/W	State ON/OFF of 4 Voltage regulators	4
PWSW	R/W	State of the 2 Power Switches	2
ANVOLT	R	Analogue Voltage	10
DGVOLT	R	Digital voltage	10
ANCUR	R	Analogue Current	10
DGCUR	R	Digital Current	10
AVOLTHR	R/W	Analogue Voltage Acceptance Band	20
ACURTHR	R/W	Analogue Current Acceptance Band	20
DVOLTHR	R/W	Digital Voltage Acceptance Band	20
DCURTHR	R/W	Digital Current Acceptance Band	20
TPTHR	R/W	Temperature upper limit	10

Table1. Temperature, Current and Voltage Monitoring.

1) **TEMP (Temperature)**. The temperature of the FEC is sampled by one of the channels of the AD7417 and the value is stored in the TEMP register.

2) **VOLTREG (Voltage Regulators)** The status of 4 voltage regulators is given. The ON state is coded with “1” and the OFF state with “0”. Only the voltage regulator which controls the supply of the BC is not mapped is this register since if the case it is OFF the BC would not even respond. This register has both read and write access since the RCU can decide to switch ON or OFF a given power regulator.

3) **PWSW (Power Switches)** The status of the two power switches is coded in this 2bit register. The RCU can switch ON or OFF each one of the power switches by writing on the PWSW register.

4) **ANVOLT (Analogue Voltage)** The supply voltage for the Analogue circuitry of the FEC is sampeld by one of the channels of the AD7417 and the value is stored in the ANVOLT register.

5) **DGVOLT (Digital Voltage)** The supply voltage for the Digital circuitry of the FEC is sampeld by one of the channels of the AD7417 and the value is stored in the DGVOLT register.

6) **ANCUR (Analogue Current)** The current sank by the Analogue circuitry of the FEC is sampled by one of the channels of the AD7417 and the value is stored in the ANCUR register.

7) **DGCUR (Digital Current)** The current sank by the Digital circuitry of the FEC is sampled by one of the channels of the AD7417 and the value is stored in the DGCUR register.

8) **AVOLTHR (Analogue Voltage Threshold)** The analogue supply voltages should remain within an acceptance band given by RCU. The lower 10bit code the lower limit and the upper 10bit code the upper limit. This register has both write and read access.

9) **ACURTHR (Analogue Current Threshold)** The currents sank by the analogue supply voltages should remain within an acceptance band given by RCU. The lower 10bit code the lower limit and the upper 10bit code the upper limit. This register has both write and read access.

10) **DVOLTHR (Digital Voltage Threshold)** The digital supply voltages should remain within an acceptance band given by RCU. The lower 10bit code the lower limit and the upper 10bit code the upper limit. This register has both write and read access.

11) **DCURTHR (Digital Current Threshold)** The currents sank by the digital supply voltages should remain within an acceptance band given by RCU. The lower 10bit code the lower limit and the upper 10bit code the upper limit. This register has both write and read access.

12) **TPTHR (Temperature Upper Limit)** This register sets the upper limit for the temperature in the FEC.

4. Error Logbook

The Error Logbook contains the flag for all possible errors detected by the BC. The Error Logbook should be the first register to be read after an interrupt is received by the RCU. Some of these errors are redundant with the ALTRO status register [4]. Table2 shows which errors the BC can be detect.

Error Logbook			
Register Name	**Access**	**Function**	**# bits**
RDERR	R	Read Protocol Error	1
WRERR	R	Write Protocol Error	1
ROERR	R	Readout Protocol Error	1
PERR	R	Parity Error	1
BEMPY	R	Buffer Empty	1
BSYERR	R	Buffer synchronization Error	1
BFULL	R	Buffer Full	1
TROVP	R	Trigger Overlap	1
AVERR	R	Analogue Voltage out of range	1
DVERR	R	Digital Voltage out of range	1
DCERR	R	Digital Current out of range	1
ACERR	R	Analogue Current out of range	1
RCKERR	R	Readout Clock error	1
SCKERR	R	Sampling Clock error	1
ISTERR	R	Instruction error	1

Table2. Error Logbook.

1) **RDERR (Read Protocol Error)** Uppon the arrival of a READ instructions to the ALTROs, the BC checks the protocol and asserts the RDERR flag if the protocol is violated.

2) **WDERR (Write Protocol Error)** Uppon the arrival of a WRITE instructions to the ALTROs, the BC checks the protocol and asserts the WDERR flag if the protocol is violated.

3) **ROERR (Readout Protocol Error)** Uppon the arrival of a READOUT command to one of the ALTROs, the BC checks the protocol and asserts the ROERR flag if the protocol is violated.

4) **PERR (Parity Error)** The BC checks the parity of the 40bit bi-directional ALTRO bus and asserts the PERR flag in the case it detects a parity violation.

5) **BEMPY (Buffer Empty)** The BC maps the multi-event buffer of each one of the 8 ALTROs and asserts the BEMPY flag if the RCU sends a READOUT command when the multi-event buffer is empty.

6) **BSYERR (Buffer Synchronization Error)** The BC can detect if there is a mis-alignement on the Buffers of the 128 channels of one FEC. Such case can happen if, e.g., the status of the Multi-Event Buffer of two chip is not the same.

7) **BFULL (Buffer Full)** The BC maps the multi-event buffer of each one of the 8 ALTROs and asserts the BFULL flag if the RCU sends a L1-L2 trigger sequence when the multi-event buffer is full.

8) **TROVP (Trigger Overlap)** The BC detects if two L1 triggers are issued within $100\mu m$, creating a trigger overlap condition. The ALTROs are also able to detect this error.

9) **AVERR (Analogue Voltage Error)** The Analogue supply Voltage being sampled by a dedicated ADC should remain within the band defined by the AVOLTHR registers, in the case it doesn't the AVERR flag is asserted.

10) **DVERR (Digital Voltage Error)** The Digital supply Voltage being sampled by a dedicated ADC should remain within the band defined by the DVOLTHR registers, in the case it doesn't the DVERR flag is asserted.

11) **DCERR (Digital Curent Error)** The current sank by the digital supply being sampled by a dedicated ADC should remain within the band defined by the DCURTHR registers, in the case it doesn't the DCERR flag is asserted.

12) **ACERR (Analogue Curent Error)** The current sank by the analogue supply being sampled by a dedicated ADC should remain within the band defined by the ACURTHR registers, in the case it doesn't the ACERR flag is asserted.

13) **RCKERR (Readout Clock Error)** The Readout clock periods are counted and any period of time without the readout clock will be detected and the RCKERR flag asserted.

14) **SCKERR (Sampling Clock Error)** The Sampling clock periods are counted and any period of time without the readout clock will be detected and the SCKERR flag asserted.

15) **ISTERR (Instruction Error)** Any Addressing of non-valid location in the ALTRO register set by the RCU is signaled the assertion of the ISTERR flag.

16) **TPERR (Temperature Error)** The temperature sampled by the dedicated ADC should remain inferior of a value defined by the TPTHR registers, in the case it doesn't the TPERR flag is asserted.

5. Statistical Data

Statistical data is stored for a better understanding of the overall system, but also enables the RCU to cross-check the number of triggers, resets, etc, it has sent with the ones actually received by each FECs. This data is summarised in table3.

Statistical Data			
Register Name	**Access**	**Function**	**# bits**
NBRL1	R	Number of L1 triggers	16
NBRL2	R	Number of L2 triggers	16
NBRRS	R	Number of Global Resets	16
NDSTB	R	Number of DSTB for the last event readout	9
NBRDO	R	Number of Readout commands	16
HWADD	R	Hardware Address	8

Table3. Statistical Data.

1) **NBRL1 (Number of L1 triggers)** The number of L1 triggers received by the FEC is stored in this 16bit register.

2) **NBRL2 (Number of L2 triggers)** The number of L2 triggers received by the FEC is stored in this 16bit register.

3) **NBRRS (Number of Global resets)** The number of global resets received by the FEC is stored in this 16bit register.

4) **NDSTB (Number of DSTB)** The number of data strobes received by the FEC in the last readout operation is stored in this 9bit register. It corresponds to the number of 40bit words sent by one of the ALTRO chips to the RCU.

5) **NBRDO (Number of Readout Commands)** The number of readout commands sent by the RCU to any ALTRO chip of the FEC is stored in the NBRDO 16bit register.

6) **NCSTB (Number of Command Strobes)** The Multi-Event Buffer (MEB) of each one of the 16 ALTROs is mirroed in this 4bitx8 register. The state of the MEB for each ALTRO chip is, in principle, the same. This mirror register allows redundancy and certifies that the data in each channel is properly synchronized.

7) **HWADD (Hardware Address)** The Hardware address of the FEC is stored in this register which can be read by the RCU.

6. Protocol and Buffer Monitoring

The RCU should monitor the ALTRO chip Multi-Event Buffer (MEB) in order to certify the time synchronization of all the channels and all the chips of each FEC and of the full sector. The BC, each time it receives a L2 and/or a WPINC or RPINC ALTRO commands updates its mirror version of the MEB. The BC can also keep all the control signal of the last instruction issued for a maximum of 10 periods of the RCLK. In this way, the RCU can understand which control signal is not properly generated. This functionality can be compared with a state analyser for the control signals. The Protocol and Buffer Monitoring registers are listed in table4.

Control and Buffer Monitoring				
Register Name	**Access**	**Function**	**Type**	**# bits**
RBUFF	R	Remaining Buffers	per channel	4x8x16
WRPTER	R	Write Pointer	per chip	3x8
MEVBF	R	Mirror of the Multi-Event buffer	per chip	4x8
RDPTER	R	Read Pointer	per chip	3x8
DSTBSC	R	CSTB scope	global	10
WRSC	R	WRITE scope	global	10
ACKSC	R	ACK scope	global	10
TRSFSC	R	TRSF scope	global	10

Table4. Control and Buffer Monitoring.

1) **RBUFF (Remaining Buffers)** The BC takes into account all the read and write pointer increments and readout commands sent to have a constant update of the remaining buffer in a per channel basis. This register is not necessarily the same as the remaining buffer given by the ALTROs status register.

2) **WRPTER (Write Pointer)** This register stores the location of the Write pointer in each one of the 8 ALTRO chips of the FEC.

3) **MEVBF (Mirror of the MEB)** This register is a mirror of the MEB for each one of the 8 ALTRO chips of the FEC.

4) **WRPTER (Write Pointer)** This register stores the location of the Read pointer in each one of the 8 ALTRO chips of the FEC.

5) **DSTBSC (DSTB scope)** This register stores the value of the control signal DSTB for 10 clock cycles of the RCLK in the last instruction received by the ALTROs from the RCU.

6) **WRSC (WRITE scope)** This register stores the value of the control signal WRITE for 10 clock cycles of the RCLK in the last instruction received by the ALTROs from the RCU.

7) **ACKSC (ACK scope)** This register stores the value of the control signal ACK for 10 clock cycles of the RCLK in the last instruction received by the ALTROs from the RCU.

8) **TRSFSC (TRSF scope)** This register stores the value of the control signal TRSF for 10 clock cycles of the RCLK in the last instruction received by the ALTROs from the RCU.

References

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