ALICE TPC Front End Card

(PCB id: 40021090)

Bus and signals assignment

Control Bus: C_BUS <14..0>

0	TRSF	TRanSFer
1	DSTB	Data STroBe
2	ACKN	ACKNowledge
3	ERROR	FEC ERROR flag
4	RST_TBC	(Reset To Board Controller only, from the RCU)
5	L1	Level 1 trigger
6	L2	Level 2 trigger
7	WRITE	WRITE instruction
8	CSTB	Command STrobe
9	RCLK	ReadOut CloCK (upstream the Fan Out)
10	free	(formerly GTL-sampling CloCK)
11	DOLO_EN	ALTRO's ext. driver output enable
12	TRSF_EN	ALTRO's ext. driver output enable
13	ACK_EN	ALTRO's ext. driver output enable
14	RST_FBC	(Reset From B.C., distributed to the ALTRO chip)

GTL Drivers control bus : GTL_CTR<5..0>

0	OEAB_H	Output Enable for BD <39..20>
1	OEBA_H	Input Enable for BD <39..20>
2	OEAB_L	Output Enable for BD <19..0>
3	OEBA_L	Input Enable for BD <19..0>
4	CTR_OUT	Control Signals Output Enable
5	CTR_IN	Control Signals Input Enable

Local Slow Control Bus : SC <2..0>

0	SCCLK	: (Clock/synch)	(RCU → FEC)
1	SCDIN	: (Serial Data Input)	(RCU → FEC)
2	SCDOUT	: (Serial Data Output)	(FEC → RCU)

Additional Busses :

PASA_# <15..0> : TPC signals to PASA section #

SCLK_D<1..0> : Sampling Clock in Differential technology
(0 = P ; 1 = N)

RDOCLK <8..0> : ReaD Out CLocK from the fan-out section

ADCCLK <8..0> : ADC (sampling) ClocK from the fan-out section

BD <39..0> : FEC internal data bus (in LV-TTL/CMOS levels)

DATA<39..0> : ReadOut Network-side corresponding of
BD <39..0> (in GTL level)

SC_GT <2..0> : " corresponding of SC <2..0>

CTR_GT <10..0> : " corresponding of C_BUS <10..0>

CARD_AD <4..0> : CARD (geographical) ADdress configuration

BCOUT_AD <4..0> : BC (masked) – card ADdress OUTput

ALTRO_AD <4..0> : corresponding of the BCOUT_AD <4..0> -
ALTRO ADdress configuration

Additional Signals :

CARD_SW : Card main-switch (LV)-TTL levels / positive logic

BC_CONF : BC (SRAM-FPGA) re-CONFiguration / positive logic

BC_INT: Interrupt signal generated by the Board Controller

INTERRUPT : Card General Interrupt signal sent through the bus

TP_SPARE #: Board Controller FPGA TestPoint / Spare I/O pins

TEST_A/B/C/D/E/F/G/H :TESTmode for ALTROs (ch. 0,1,2,3 def.)

ADC_ADD0/1:ADC channel addr in TEST mode

MPS_ENABLE : Master Power Supplies Enable

MPS_ERROR : Master Power Supplies Error

ALTRO_SW : enable the ALTRO power regulator (1=ON,0=OFF)

PASA_SW : enable the PASA power regulator (0=ON,1=OFF)

ALPS_ERROR : ALTROs Power Supplies Error

PAPS_ERROR : PASAs Power Supplies Error

SCLK_DN : Neg. of the Sampling Clock distributed in Differential

SCLK_PN : Pos. of the Sampling Clock distributed in Differential

MSCL : Monitor ADC ClocK

MSDA : Monitor ADC Serial Data

MCST : Monitor ADC Conversion STart

OTI : Monitor ADC Over Temperature Indicator

ADCCLK_EN : Sampling Clock Fan-Out Enable

RDOCLK_EN : ReadOut Clock Fan-Out Enable

Power Supplies:

+4V0IN : external 4.0 Volt power supply (for the 3.3V regulators)

+3V3IN : external 3.3 Volt power supply (for the 2.5V regulators)

+4V0 : Internal 4.0 V

+3V3 : Internal 3.3 V

+3V3_DIG : 3.3V for digital supply

+3V3_PASA: 3.3V PASA power supply

+2V5_DIGDRV : 2.5V for GTL DRIVERs

+2V5_DIGLGC : 2.5V for the BC FPGA + Fan Out Clock Drivers

+2V5_D : 2.5V logic power supply for ALTRO

+2V5_A : 2.5V analog power supply for ALTRO

VRA <7..0> : VRA (InCM + RefP) voltage for the ALTROs

VRT : VRT reference voltage for all the PASA

VRM : VRM (common mode) voltage for all the PASA

VRB : VRB reference voltage for all the PASA

PASAGND : PASA Input Signals Ground

GND : Digital Ground

AGND : Analog Ground

EARTH : Common Ground Reference

GTL_VREF : REFerence Voltage for GTL transceivers