ALICE TPC Board Controller (version 2.3)

Register Table description

CERN – PH / ED

Registers Table (9/12/2004)

Reg. Addr.	*Mnemonic*	*Reg. Name*	*Width*	*Acc. Mode*	*Allow Bcast*	*Meaning*
00						
01	T_TH	Temperature Thr.	10	R/W	Y	Maximum Temperature Threshold
02	AV_TH	AV threshold	10	R/W	Y	Minimum Analog Voltage Threshold
03	AC_TH	AC threshold	10	R/W	Y	Maximum Analog Current Threshold
04	DV_TH	DV threshold	10	R/W	Y	Minimum Digital Voltage Threshold
05	DC_TH	DC threshold	10	R/W	Y	Maximum Digital Current Threshold
06	TEMP	Temperature	10	R	N/A	Temperature Value
07	AV	Analog Voltage	10	R	N/A	Analog Voltage Value
08	AC	Analog Current	10	R	N/A	Analog Current Value
09	DV	Digital Voltage	10	R	N/A	Digital Voltage Value
0A	DC	Digital Current	10	R	N/A	Digital Current Value
0B	L1CNT	L1 Counter	16	R	N/A	Number of L1 Trigger Received
0C	L2CNT	L2 Counter	16	R	N/A	Number of L2 Trigger Received
0D	SCLKCNT	Sampling clk counter	16	R	N/A	Sampling Clock counter
0E	DSTBCNT	Data Strobe counter	8	R	N/A	Number of Data Strobe in the last ReadOut
0F	TSMWORD	Test Mode Word	9	R/W	Y	Number of words to store/read in test mode
10	USRATIO	Under sampling ratio	16	R/W	Y	Under sampling factor
11	CSR0	Configuration Status 0	16	R/W	Y	Interrupt - Mask Register
12	CSR1	Configuration Status 1	16	R/W	Y	Error Status Register
13	CSR2	Configuration Status 2	16	R/W	Y	Card Configuration Status Register
14	CSR3	Configuration Status 3	16	R/W	Y	Card Configuration Status Register
15	FREE					

16	CNTLAT	Counters Latch	-	W	Y	Latch L1, L2, SCLK counters
17	CNTCLR	Counters Clear	-	W	Y	Clear L1, L2, SCLK counters
18	CSR1CLR	Conf. St. Reg 1 Clear	-	W	Y	Clear Error Status Register
19	ALRST	ALTRO Reset	-	W	Y	Reset all the ALTROs
1A	BCRST	BC Reset	-	W	Y	Set default values in registers of BC
1B	STCNV	Start Conversion mADC	-	W	Y	Start Conversion / Read Out Monitor ADC
1C	SCEVL	Scan event length	-	W *	Y	
1D	EVLRDO	Read event length	-	W *	N/A	
1E	STTSM	Start Test Mode	-	W *	Y	
1F	ACQRDO	Read acquisition memory	-	W *	N/A	

* Accessible with the ALTRO protocol interface only

T_TH

Temperature threshold

Instruction Code	5´h01
Width	10
Access Type	Read / Write
Allow Broadcast	Yes
Conversion Factor	0.25 ºC / ADC count
Default value	10'hA0 (40ºC)

Description:

The **temperature** readout by the BC from the monitor ADC is continuously compared with the T_TH. As soon as the temperature is higher than the threshold, the error flag CSR1 [0] is set to 1 and the Interrupt line asserted.

AV_TH

Analog Voltage threshold

Instruction Code	5´h02
Width	10
Access Type	Read / Write
Allow Broadcast	Yes
Conversion Factor	4.43 mV / ADC count
Default value	10'h330 (3.61 V)

Description:

The **Analog Voltage** readout by the BC from the monitor ADC is continuously compared with the AV_TH. As soon as this value is lower than the threshold, the error flag CSR1 [1] is set to 1 and the Interrupt line asserted.

AC_TH

Analog Current threshold

Instruction Code	5´h03
Width	10
Access Type	Read / Write
Allow Broadcast	Yes
Conversion Factor	17 mA / ADC count
Default value	10'h2C (0.75 A)

Description:

The **Analog Current** readout by the BC from the monitor ADC is continuously compared with the AC_TH. As soon as this value is higher than the threshold, the error flag CSR1 [2] is set to 1 and the Interrupt line asserted.

DV_TH

Digital Voltage threshold

Instruction Code	5´h04
Width	10
Access Type	Read / Write
Allow Broadcast	Yes
Conversion Factor	4.43 mV / ADC count
Default value	10'h280 (2.83 V)

Description:

The **Digital Voltage** readout by the BC from the monitor ADC is continuously compared with the DV_TH. As soon as the value is higher than the threshold, the error flag CSR1 [3] is set to 1 and the Interrupt line asserted.

DC_TH

Digital Current threshold

Instruction Code	5´h05
Width	10
Access Type	Read / Write
Allow Broadcast	Yes
Conversion Factor	30 mA / ADC count
Default value	10'h40 (1.92 A)

Description:

The **Digital Voltage** readout by the BC from the monitor ADC is continuously compared with the DC_TH. As soon as the digital voltage is higher than its threshold, the error flag CSR1 [4] is set to 1 and the Interrupt line asserted.

TEMP

Temperature

Instruction Code	5´h06
Width	10
Access Type	Read
Allow Broadcast	No
Conversion Factor	0.25 ºC / ADC count
Default value	10'hA0 (40ºC)

AV

Analog Voltage

Instruction Code	5´h07
Width	10
Access Type	Read
Allow Broadcast	No
Conversion Factor	4.43 mV / ADC count
Default value	10’h330 (3.61 V)

AC

Analog Current

Instruction Code	5´h08
Width	10
Access Type	Read
Allow Broadcast	No
Conversion Factor	17 mA / ADC count
Default value	10’h2C (0.75 A)

DV

Digital Voltage

Instruction Code	5´h09
Width	10
Access Type	Read
Allow Broadcast	No
Conversion Factor	4.43 mV / ADC count
Default value	10’h280 (2.83 V)

DC

Digital Current

Instruction Code	5´h0A
Width	10
Access Type	Read
Allow Broadcast	No
Conversion Factor	30 mA / ADC count
Default value	10’h40 (1.92 A)

L1CNT

Number of L1 triggers received

Instruction Code	5´h0B
Width	16
Access Type	Read
Allow Broadcast	No
Default value	16'h0

Description:

The command CNTLAT (5'h16) stores the content of the Level-1 trigger counter in the register L1CNT. It can be reset with the CNTCLR (5'h17) command.

L2CNT

Number of L2 triggers received

Instruction Code	5´h0C
Width	16
Access Type	Read
Allow Broadcast	No
Default value	16'h0

Description:

The command CNTLAT (5'h16) stores the content of the Level-2 trigger counter in the register L2CNT. It can be reset with the CNTCLR (5'h17) command.

SCLKCNT

Number of Sampling Clock cycles

Instruction Code	5´h0D
Width	16
Access Type	Read
Allow Broadcast	No
Default value	16'h0

Description:

The command CNTLAT (5'h16) stores the content of theSCLK counter in the register SCLKCNT. It can be reset with the CNTCLR (5'h17) command.

DSTBCNT

DSTB counter

Instruction Code	5´h0E
Width	8
Access Type	Read
Allow Broadcast	No
Default value	8'hF

Description:

This register stores the number of DSTB asserted in the last ALTRO channel readout

TSMWORD

Test Mode word

Instruction Code	5´h0F
Width	9
Access Type	Read / Write
Allow Broadcast	Yes
Default value	9'h1

8	0
Number of words to store/read in test mode	

USRATIO

Under sampling factor

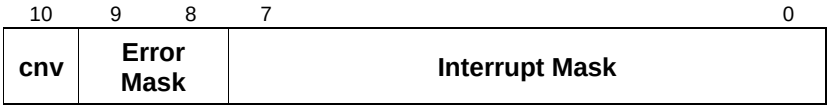
Instruction Code	5´h10
Width	16
Access Type	Read / Write
Allow Broadcast	Yes
Default value	16’h1

CSR0

Configuration – Status Register 0

Instruction Code	5´h11
Width	11
Access Type	Read / Write
Allow Broadcast	Yes
Default value	11'h3FF

Instruction Coding



Description

Parameter	Description	Range (hex)
cnv	Conversion Mode: 0 The BC reads the content of the monitor ADC with the STCNV command (1B) 1 monitor ADC converts continuously	0 – 1
Error Mask	These two bits mask the assertion of the **Error line.** This line is asserted with the flags registered in CSR1 [9 : 8] 0 the error is masked 1 the error asserts the line	0 – 3
Interrupt Mask	These bits mask the bits of CSR1 [7:0] for the assertion of the **Interrupt line**	0 – FF

Note:

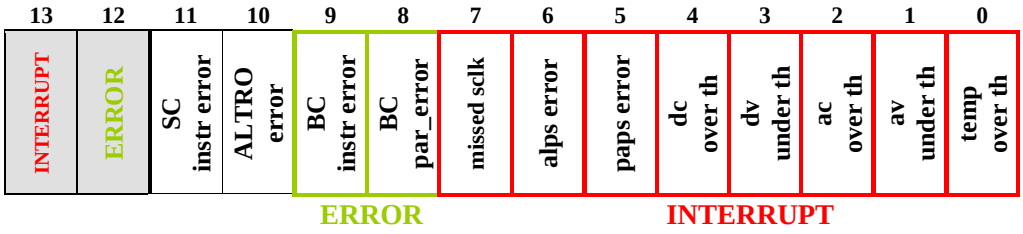
For the Interrupt and Error signals assertion, the corresponding mask should be enabled. Each error flag in CSR1 must have its mask in CSR0 enabled. If it is disabled, the Error/Interrupt line will no be asserted with the event of the corresponding error.

CSR1

Configuration – Status Register 1

Instruction Code	5´h12
Width	14
Access Type	Read / Write
Allow Broadcast	Yes
Default value	14'h0

Instruction Coding



Description

Parameter	Description	Line asserted
temp over th	Temperature is higher than the threshold T_TH	Interrupt Line
av under th	Analog voltage is lower than the threshold AV_TH	Interrupt Line
ac over th	Analog current is higher than the threshold AC_TH	Interrupt Line
dv under th	Digital voltage is lower than the threshold DV_TH	Interrupt Line
dc over th	Digital current is higher than the threshold DC_TH	Interrupt Line
paps error	PASA power supply error: the power regulator that supply the PASA asserts its error line	Interrupt Line
alps error	ALTRO power supply error: the power regulator that supply the ALTRO asserts its error line	Interrupt Line
missed sclk	Missing sampling clock: this flag is asserted in the case that any SCLK cycle is detected during the number of readout clock cycles specified by CSR3 [7 : 0] (rclk / sclk ratio)	Interrupt Line
BC par_error	This flag is the parity bit of the 20 most significant bits of the ALTRO bus.	Error Line

BC instr error	This bit is asserted if there was a wrong access mode to the BC Register Table from the ALTRO bus (ex: try to write a only read register)	Error Line
ALTRO error	The value of the ALTRO bus error signal is registered	-
SC instr error	This bit is asserted if there was a wrong access mode to the BC Register Table from the Slow Control bus	-
ERROR	Value of the ALTRO bus **error** line	-
INTERRUPT	Value of the Slow Control **interrup**t line	-

Note:

The command CSR1CLR (5'h16) reset all the content of the CSR1 register.

CSR2

Configuration – Status Register 2

Instruction Code	5´h13
Width	16
Access Type	Read / Write
Allow Broadcast	Yes
Default value	16'hF

Instruction Coding

15 … 11	10	9	8	7	6	5	4	3	2	1	0
		ALTRO test mode						clock_en		paps_en	
HADD	Card isolated	Continuous TSM	ALTRO address			ADC address		adcclk_en	rdoclk_en	pasa_sw	altro_sw

Description

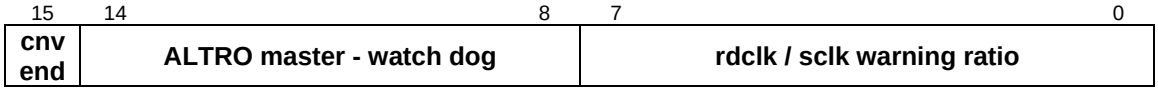
Parameter	Description	Access mode
HADD	FEC hardware address	read
Card isolated		read / write
Continuous TSM		read / write
ALTRO address	ALTRO address for the Test Mode	read / write
ADC address	ADC address for the Test Mode	read / write
adcclk_en	It enables the distribution of the sampling clock	read / write
rdoclk_en	It enables the distribution of the readout clock	read / write
pasa_sw	It enables the power regulator that provides the voltage to the PASA	read / write
altro_sw	It enables the power regulator that provides the voltage to the ALTRO	read / write

CSR3

Configuration – Status Register 3

Instruction Code	5´h14
Width	16
Access Type	Read / Write
Allow Broadcast	Yes
Default value	16'h2220

Instruction Coding



Description

Parameter	Description	Access mode
cnv end	This bit is set to 1 when the BC has completed the transaction with the mADC. It is reset at the beginning of every transaction.	read
ALTRO master – watch dog		read/write
rdclk / sclk warning ration	Referred to the detection of the missing sampling clock	read/write