FEE: STATUS AND PLANNING FOR 2002

CERN, April 29-30, 2002

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OUTLINE

- Progress
- Milestones
- Work to be completed in 2002

Detailed planning: http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/

PROGRESS (DEC '01 – APR '02)

- PASA final version
 - Characterization of 3 samples
 - PASA meet all design requirements
- ALTRO final version
 - Characterization of 110 samples
 - ALTRO meet all design requirements
 - Production yield > 85%
- New FEC card (final version of all components):
 - Standalone test completed: good signal integrity of FEC internal bus up to 100 MHz (required frequency ≤ 40MHz)
- Upgrade of pRCU-I (PCI-RCU)
 - Hardware complete
 - Firmware/software <u>almost</u> complete

TPC FEE STATUS – MILESTONES

PASA (40 000 chips) LHCC **STATUS** January '02 **Prototyping:** done **Engineering run: April '02 – August '02** 2 mm delay **Full production:** September '02 – January '03 Testing: February '03 – September '03 **ALTRO (40 000 chips) Prototyping:** January '02 done **Engineering run: April '02 – August '02** on schedule **Production:** September '02 – January '03 February '03 – September '03 **Testing: FEC (4500 boards)** Prototyping (test of 50 FEC +IROC): August '02 on schedule October '02 - January '03 **Production:** ?? Testing: May '03 - January '04 **READOUT BUS (216 units) Prototyping:** September '01 done **Production:** January '03 - June '03 **READOUT CONTROL UNIT (216 boards)** April '03 **Prototyping:** • RCU-I (PLDa-based RCU) March '02 2 mm delay • RCU-II (delivery) May '02 2 mm delay **Production:** May '03 – July '03 July '03 - Nov '03 Testing:

PASA

♦ Tests:

Test of packaged chips in FEC (CERN): May

Radiation test – tolerance to SEL in FEC (CERN): September

Engineering Run

Layout optimization (Heidelberg):

Manufacturing of full-sheet wafer (AMS):
July - September

Delivery of ER samples: October

Test of ER samples (Heidelberg ?):
November

Automatic Test Equipment (ATE)

Design and construction of ATE (Darmstadt TU): October

Validation of PASA ATE (Darmstadt - Heidelberg): October - November

Test software (???):

ALTRO

♦ Tests:

Test of additional 187 chips (CERN): May '02

Radiation test – tolerance to SEU and SEL (CERN):

Test setup (under construction): May '02

• Test: July

Engineering run

Manufacturing of the full-sheet wafer (STM): started

Delivery of ER samples:
September

Test of ER samples: October

Test equipment

Design and construction of ATE (LUND): July

Validation of ATE (LUND):
July - August

Test software (CERN-LUND): well advanced

FRONT END CARD

Tests:

Test of standalone FEC (CERN): doneTest of FEC + pRCU-I (CERN + BERGEN): May

Radiation test – tolerance to SEU and SEL (CERN): July - August

Test of 50FEC, 2 pRCU-II, LVPS, COOLING, IROC: from August onwards

FEC final version

Modification of card layout (CERN): MayManufacturing (Lund - CERN): June

■ Test (CERN): August - September

Test equipment

Design and construction of ATE (Frankfurt): June

Validation of ATE (Frankfurt-CERN): July

Test software (Frankfurt): ??

Market survey and Price Enquiry / Call for tenders (Lund)

READOUT CONTROL UNIT

Test of PCI-RCU (pRCU-I) (Bergen - CERN): May

Design of pRCU-II (Bergen – Oslo - Heidelberg):

May

Manufacturing of pRCU-II (Bergen):
June

Test of pRCU-II

Standalone pRCU- II (Bergen – Oslo - Heidleberg)
 August

pRCU-II + FEC (Bergen – CERN)
September

pRCU-II + RORC (Bergen)
October

Market survey and Price Enquiry / Call for tenders (Lund)

TASKS TO BE COMPLETED IN 2002 AND NOT YET ASSIGNED

- Characterization of PASA ER samples
- Software for PASA ATE
- Database for FEE components sorting and history