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- ALTRO Test Setup and Equipment
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- Noise and Crosstalk
- Power Consumption
- ALTRO Testing Strategy
- Functional and Physical Validation
- Yield Results and Considerations
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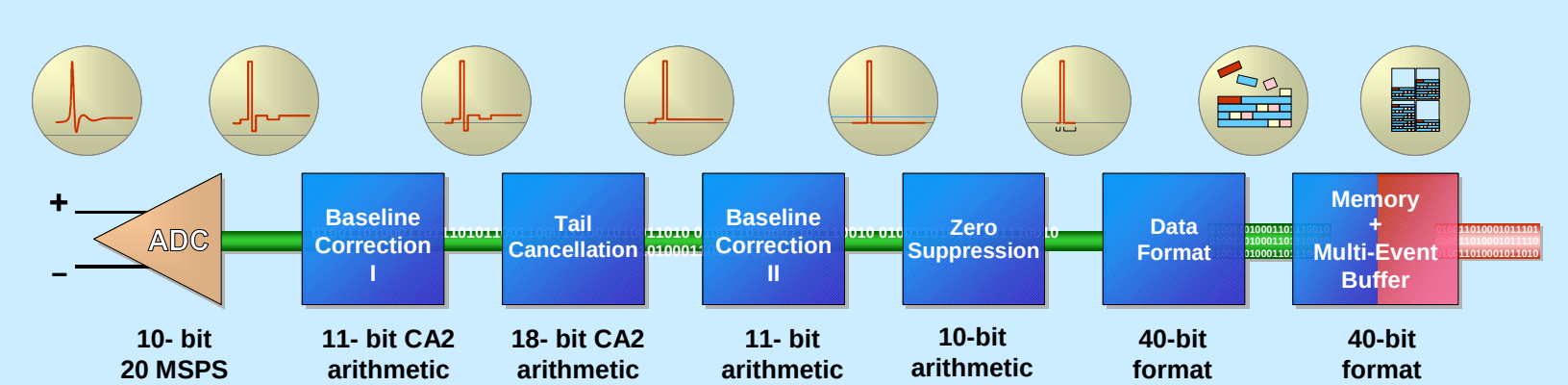
ALICE TPC READOUT CHIP (ALTRO-16)

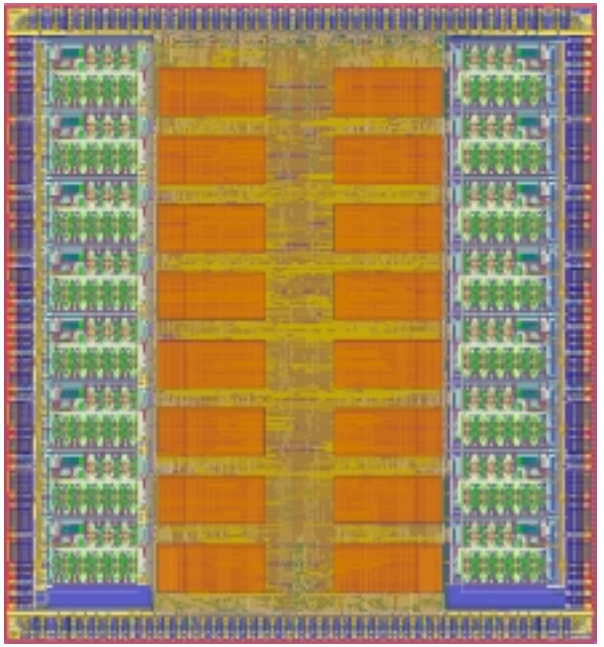


MAX SAMPLING CLOCK 40 MHz

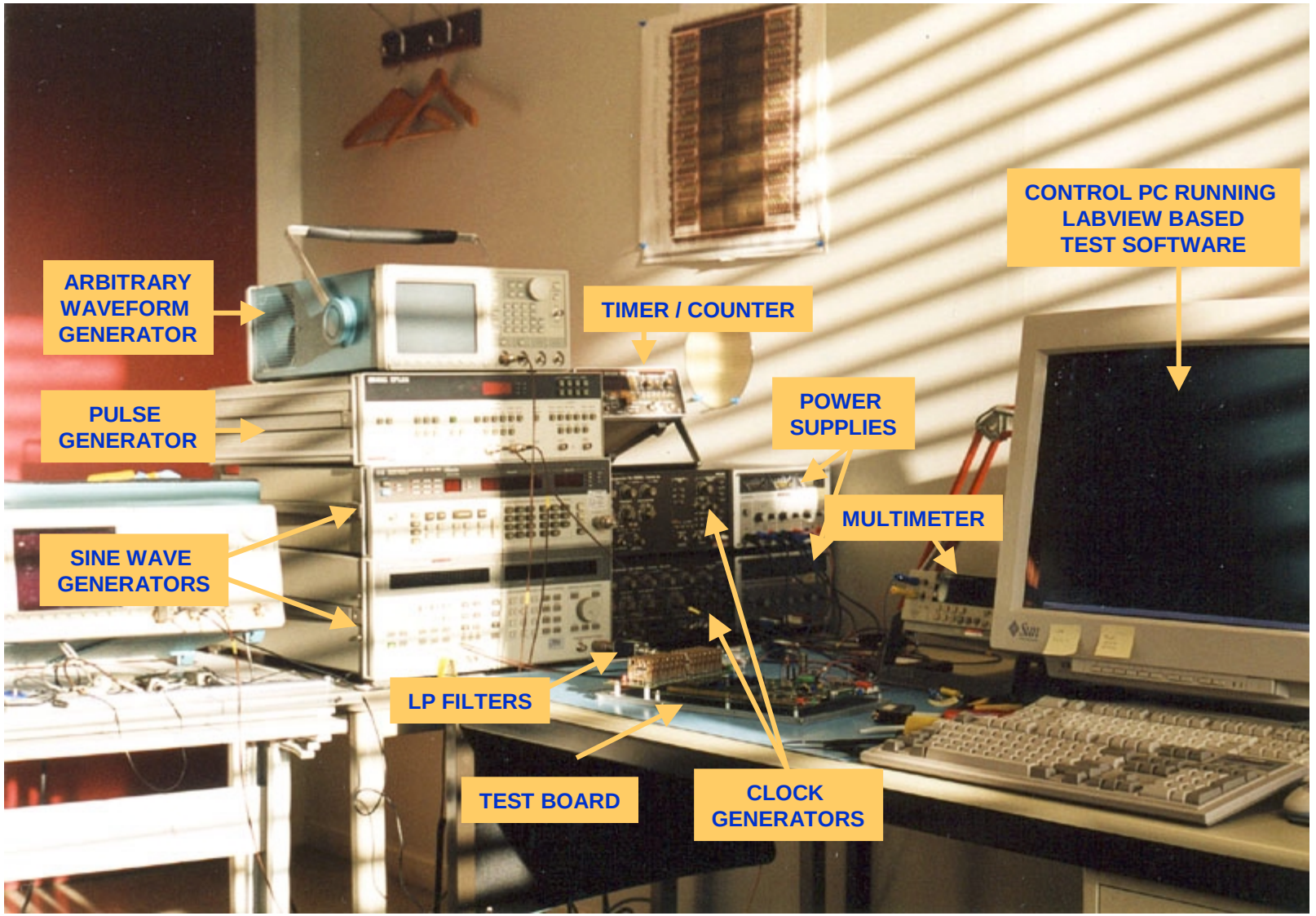
MAX READOUT CLOCK 60 MHz

16-ch signal digitizer and processor

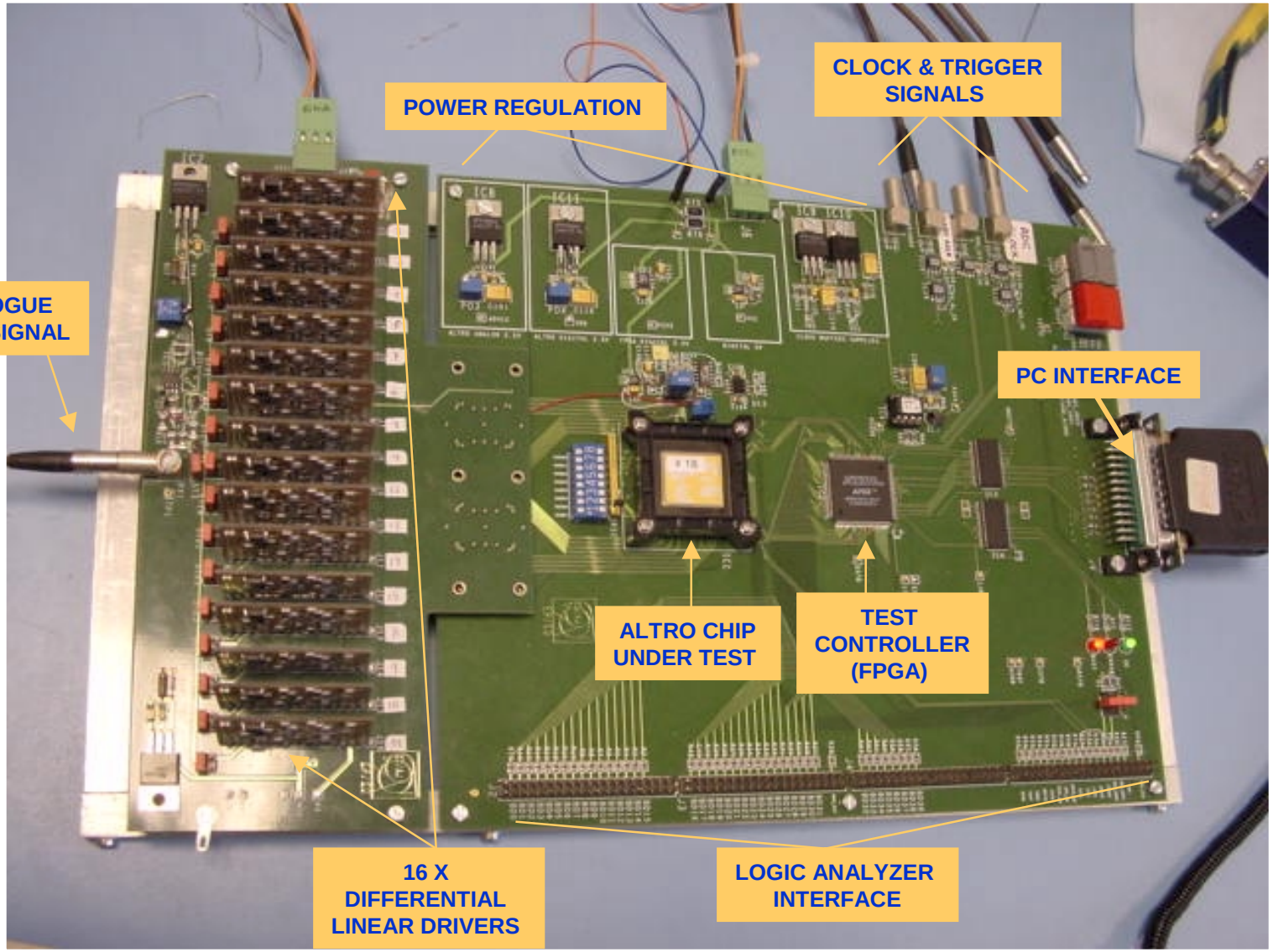
- HCMOS7 0.25 μm (ST)
- area: 64 mm^2
- power: < 20 mW / ch
- prototype delivery: Feb '02
- 300 samples fully tested



ALTRO Test Setup



ALTRO Test Board



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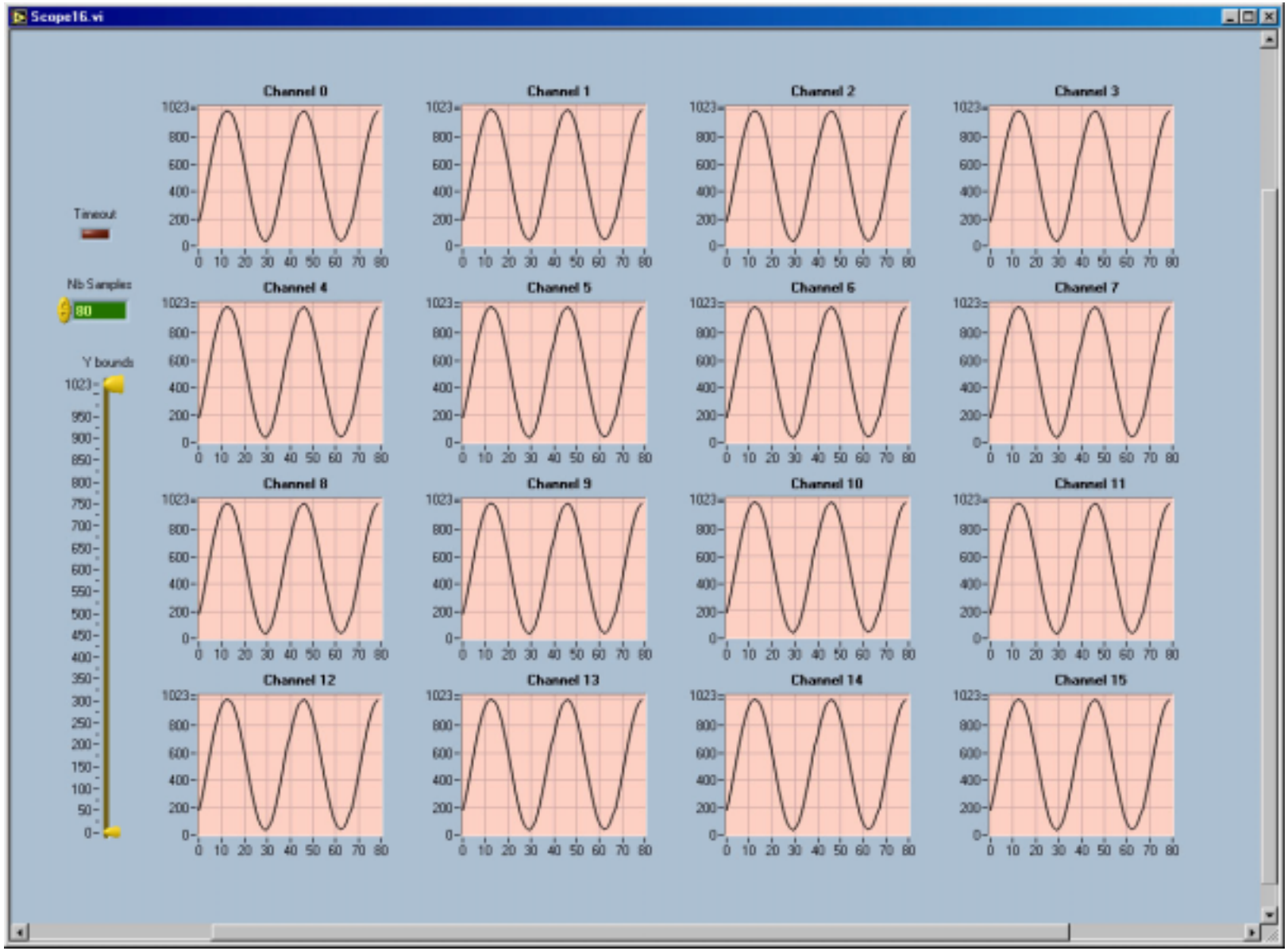
16 channels in one shot



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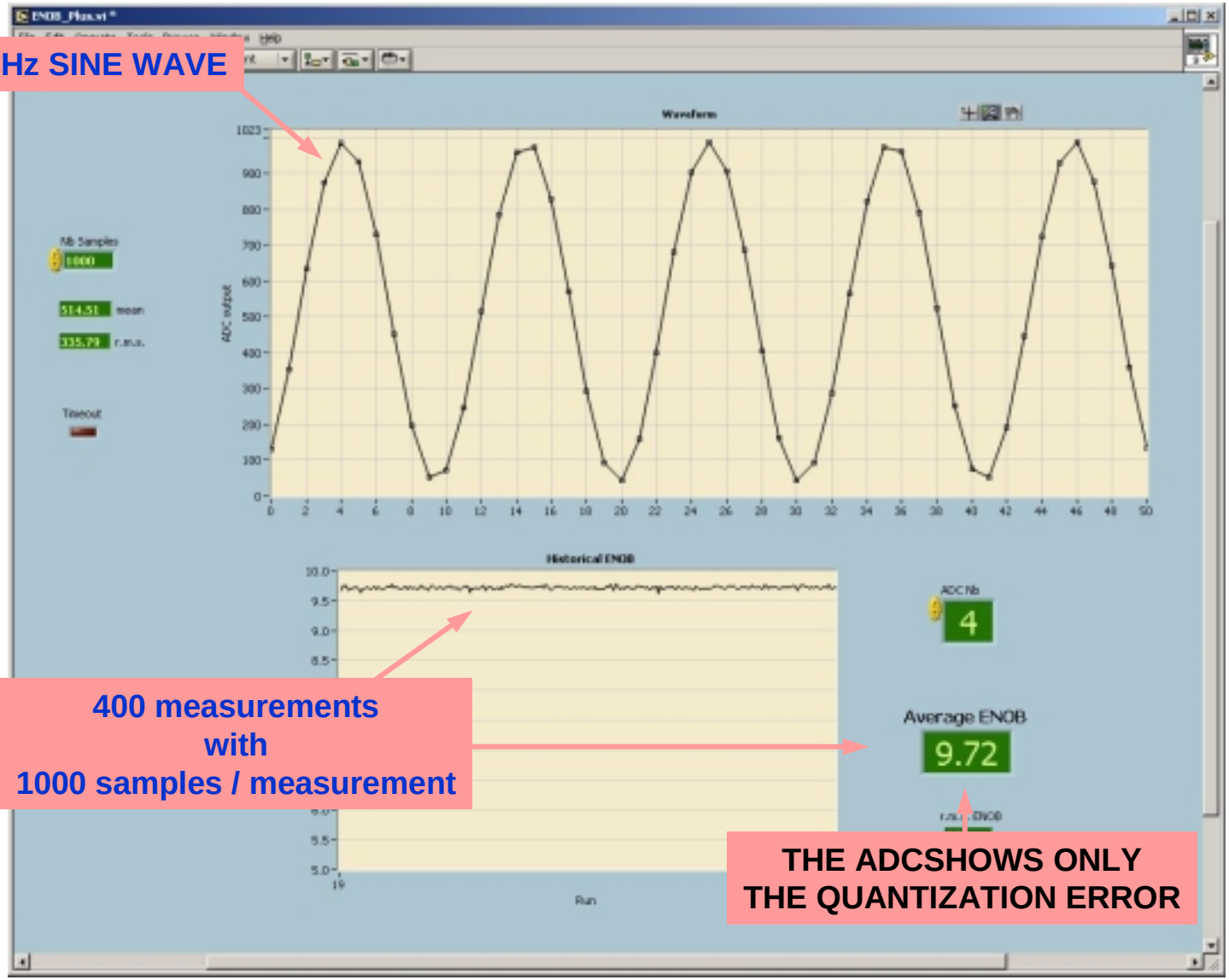
Effective Number of Bits (ENOB)



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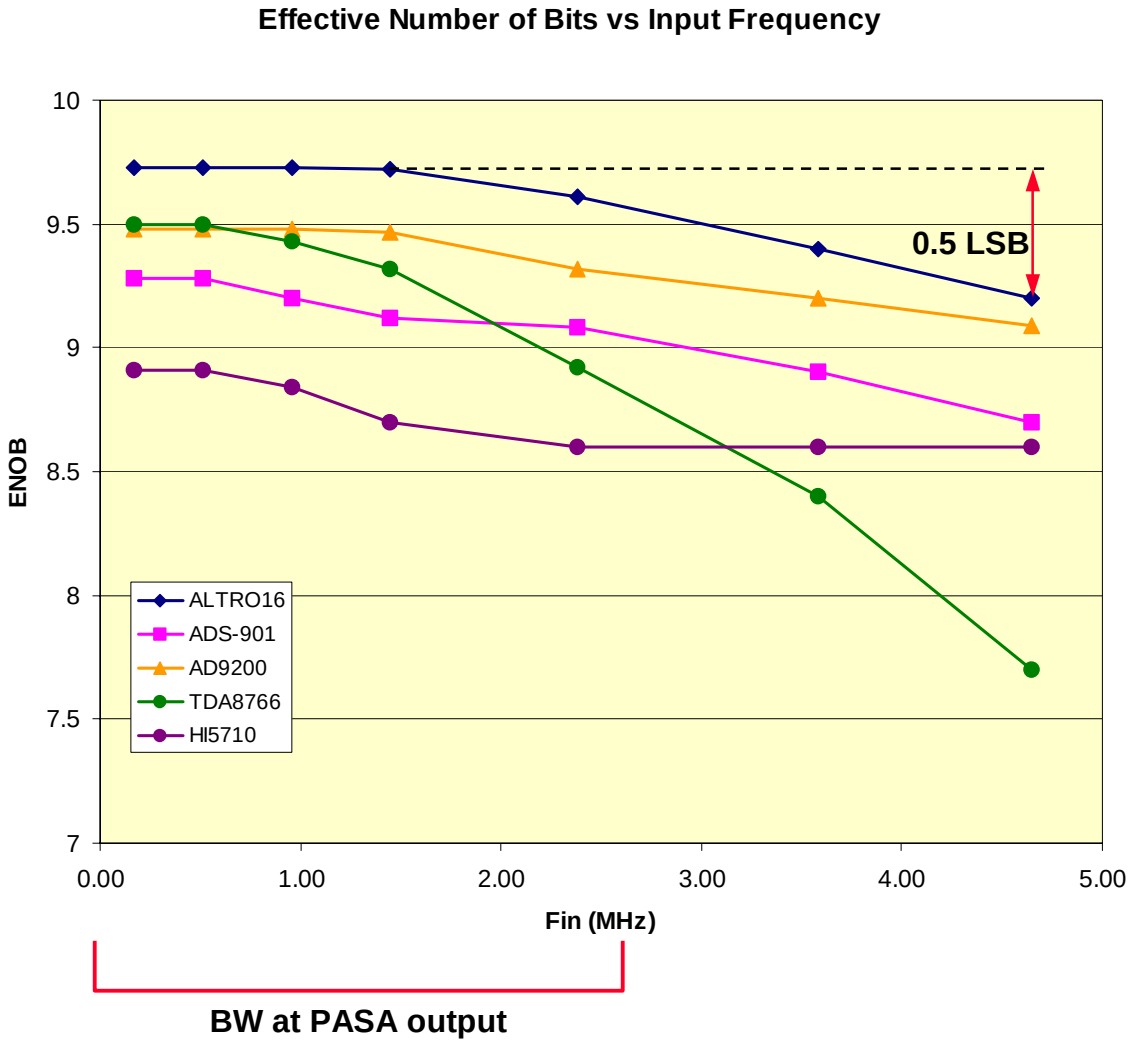
ENOB vs Frequency



Quartz Jitter:

25ps r.m.s.

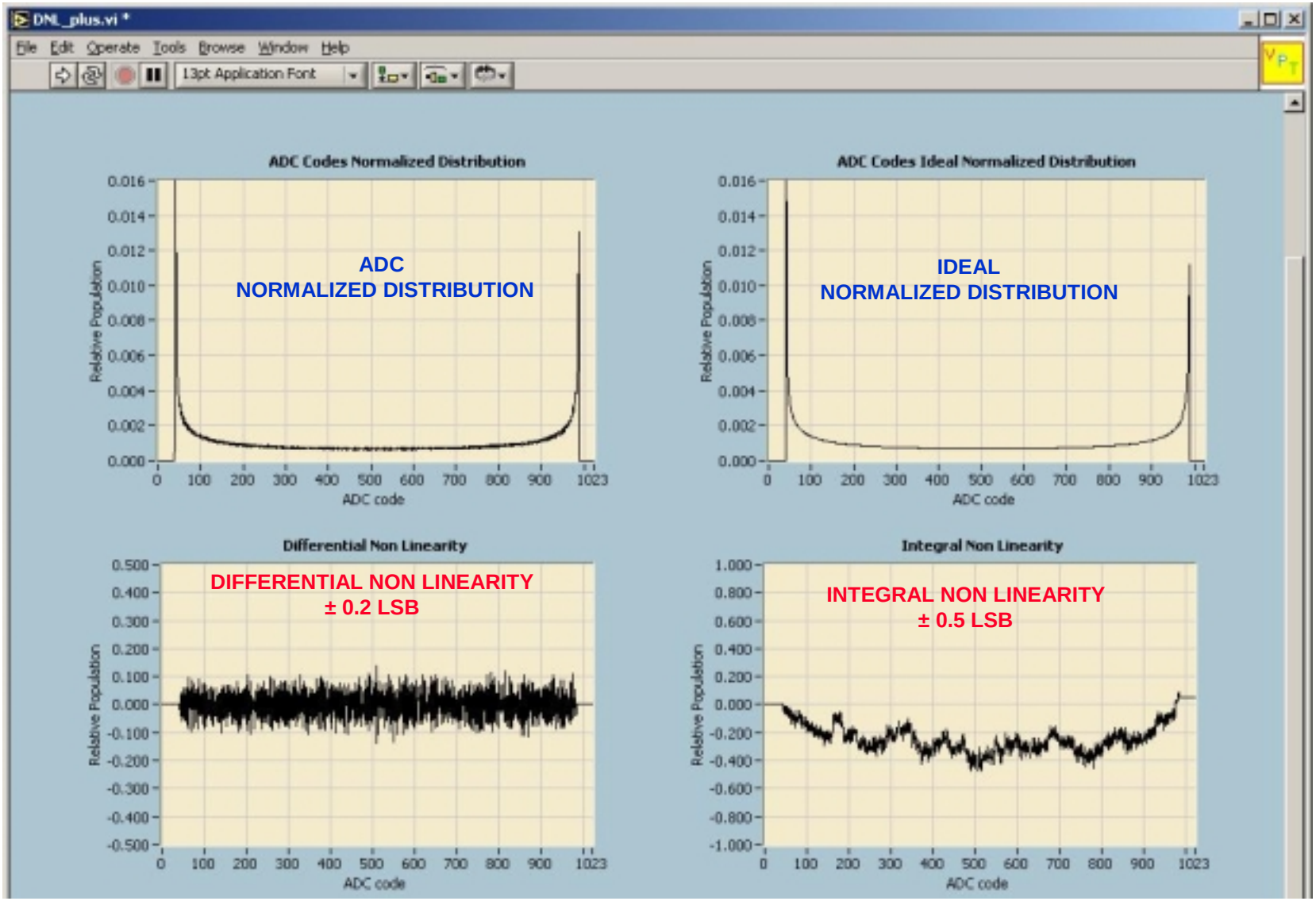
100ps absolute

Amplitude Uncertainty:

$$\frac{\text{jitter}}{4 \cdot f_{in}} \cdot 2^{10}$$

0.5 bits at 4.8 MHz

Differential and Integral Non-Linearity



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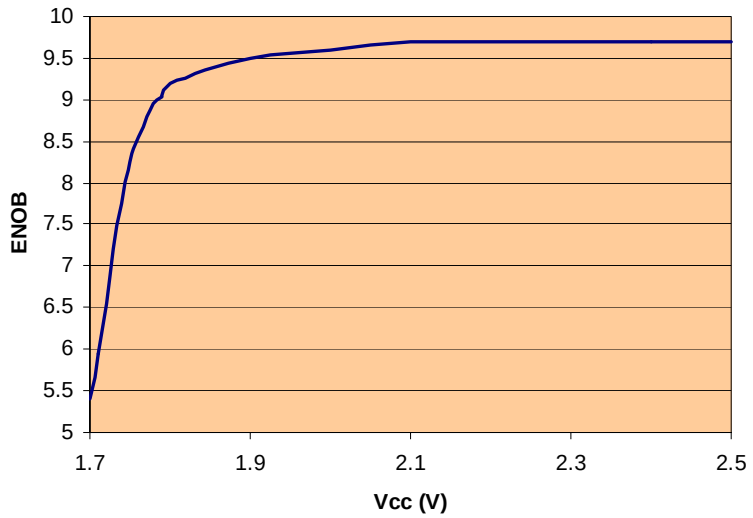
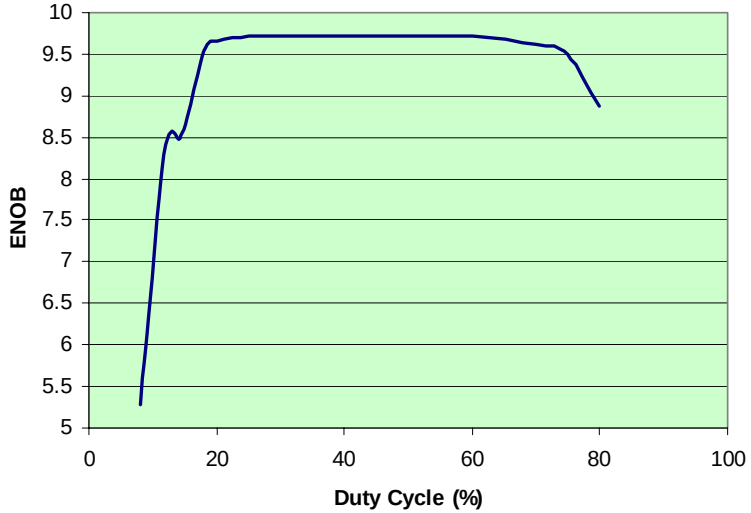
Chip Performance

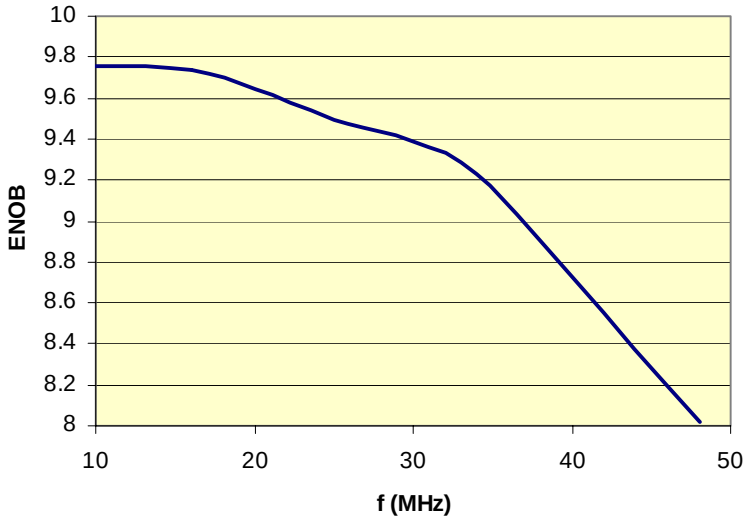
ENOB vs Analog Vcc



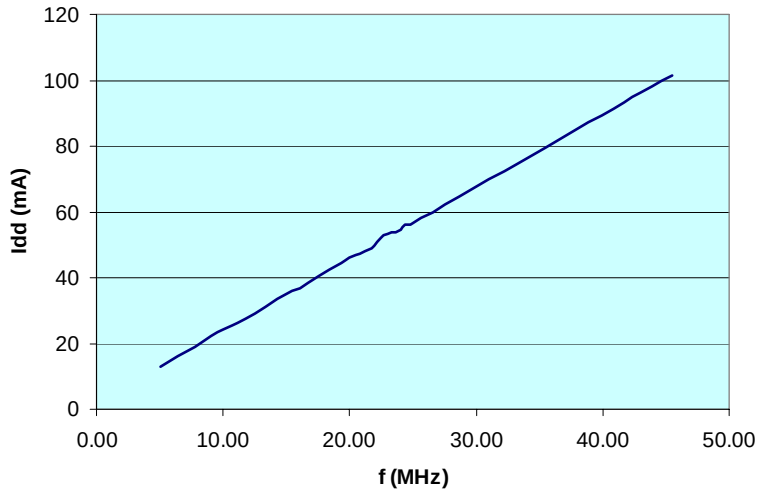
ENOB vs Duty Cycle



ENOB vs Sampling Frequency

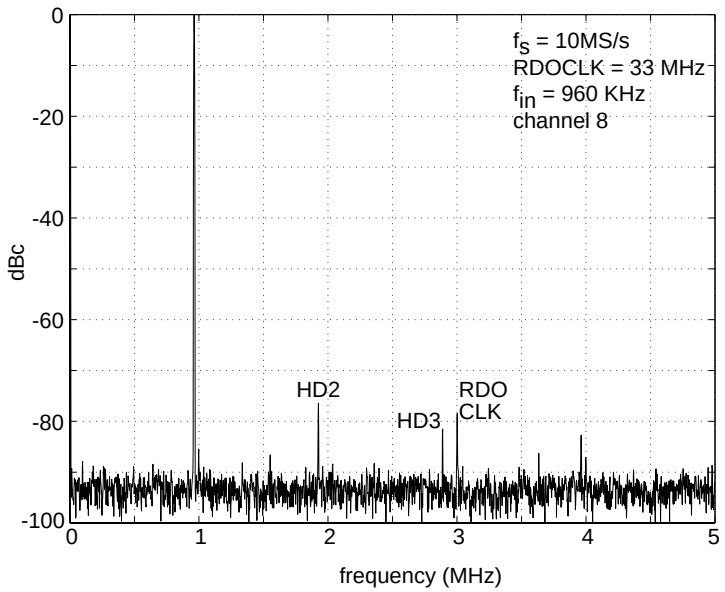


Digital Power Consumption vs Sampling Frequency

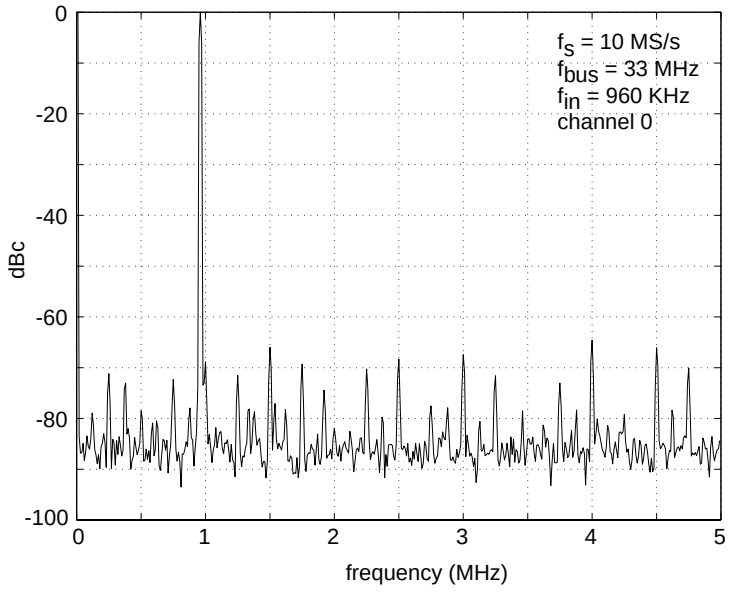


Crosstalk and Digital Noise

DIGITAL NOISE



Readout Clock below -78 dBc (WC)



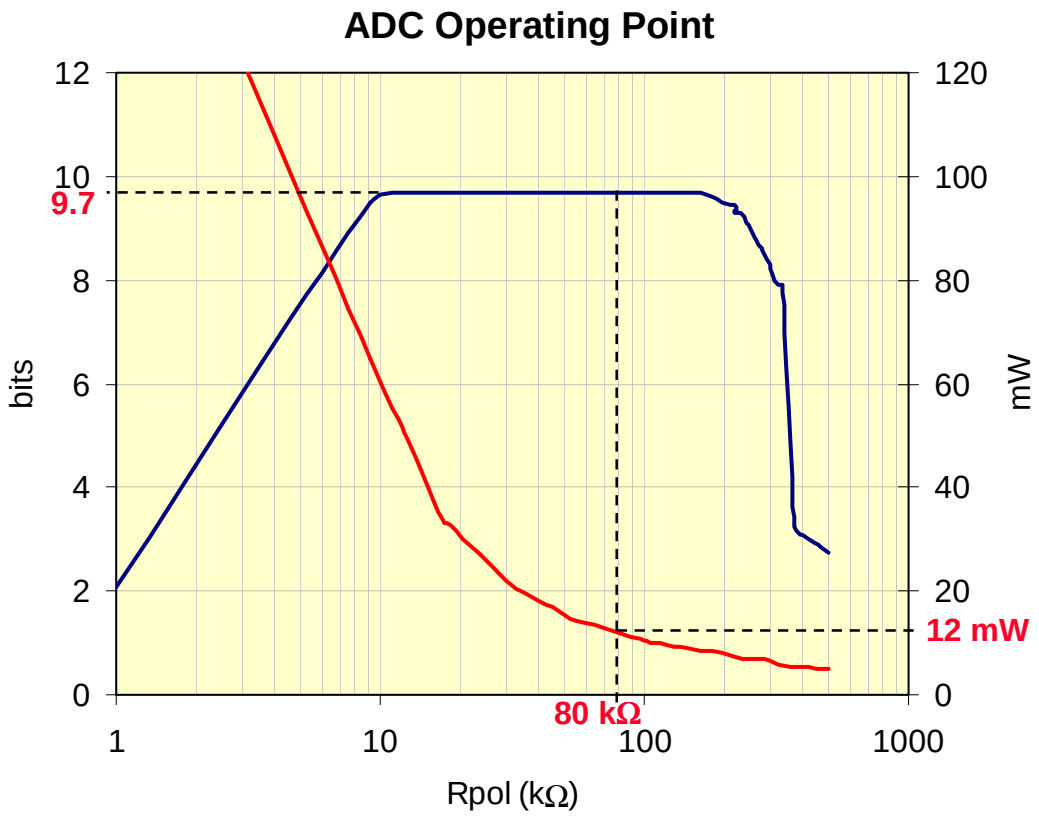
Bus interference below -65 dBc (WC)

CHANNEL-TO-CHANNEL CROSSTALK

F_{in} = 1 MHz 0.05 LSB rms (-80 dBc)
F_{in} = 5 MHz 0.2 LSB rms (-68 dBc)

Dynamic Range of a 10-bit ADC: 60 dB

Power Consumption



Effective Number of Bits

Power Consumption per Channel

ONE CHIP		
	Digital leakage current	1.2 mA
	ADC Clock Tree (10 MHz)	23 mA
	Readout Clock Tree (40 MHz)	1.4 mA
	Processing Logic during Trigger (1%)	28 mA
	16 ADCs at 10 MS/s	77 mA

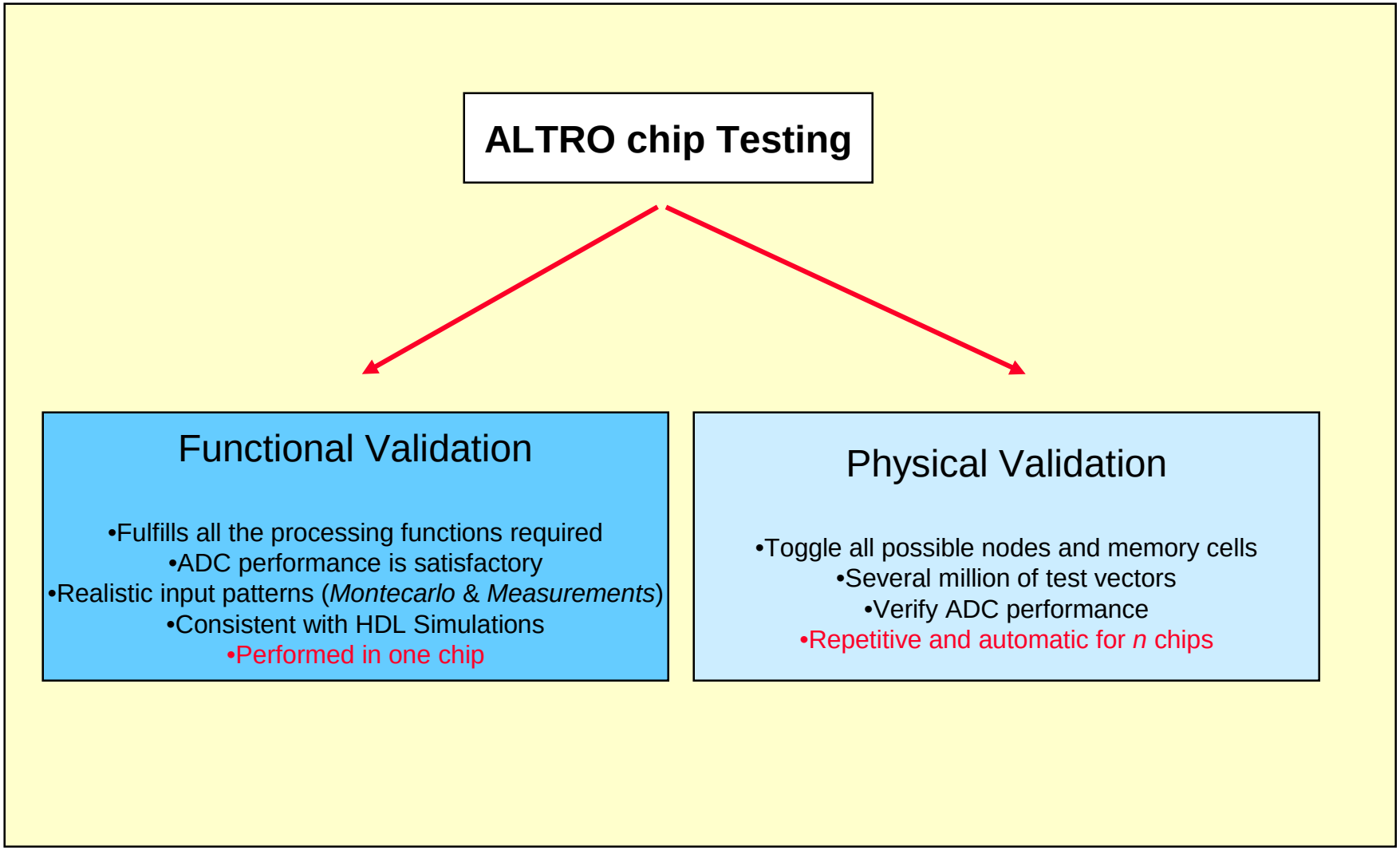
Average Power Per Chip

257 mW

Average Power Per Channel

16 mW

Testing Strategy



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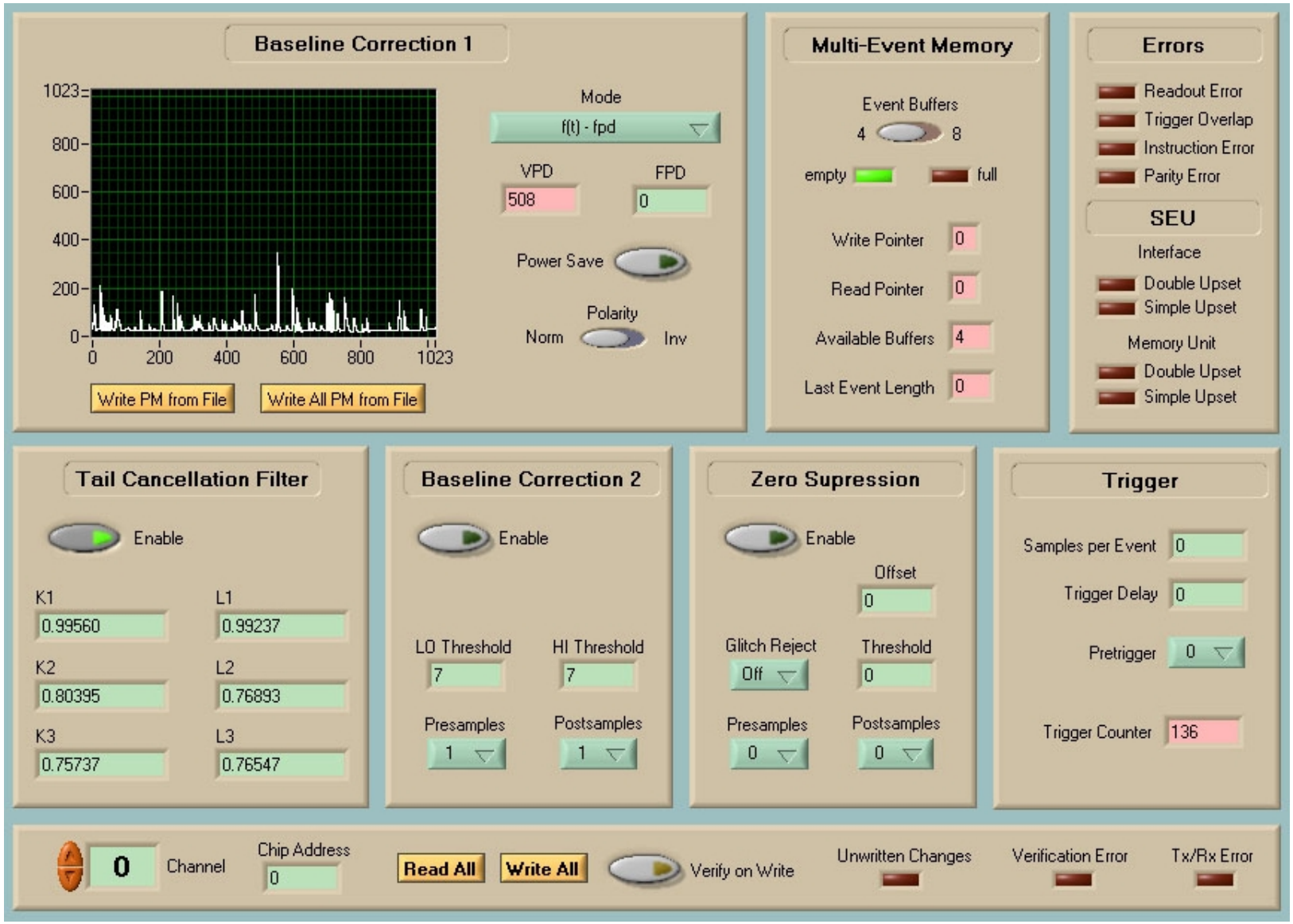
Functional Validation: Register Control Panel



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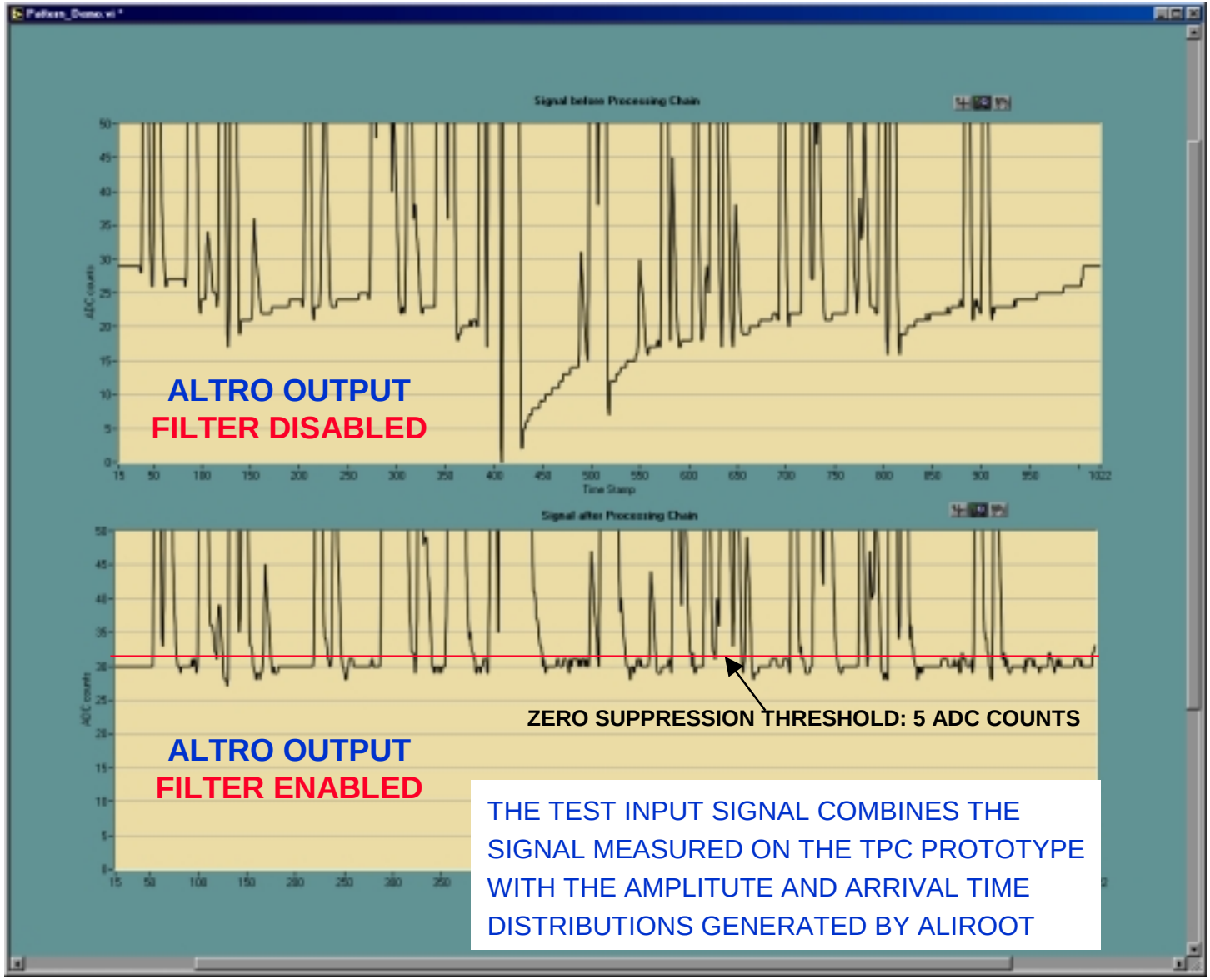
Functional Validation: Realistic Input Pattern



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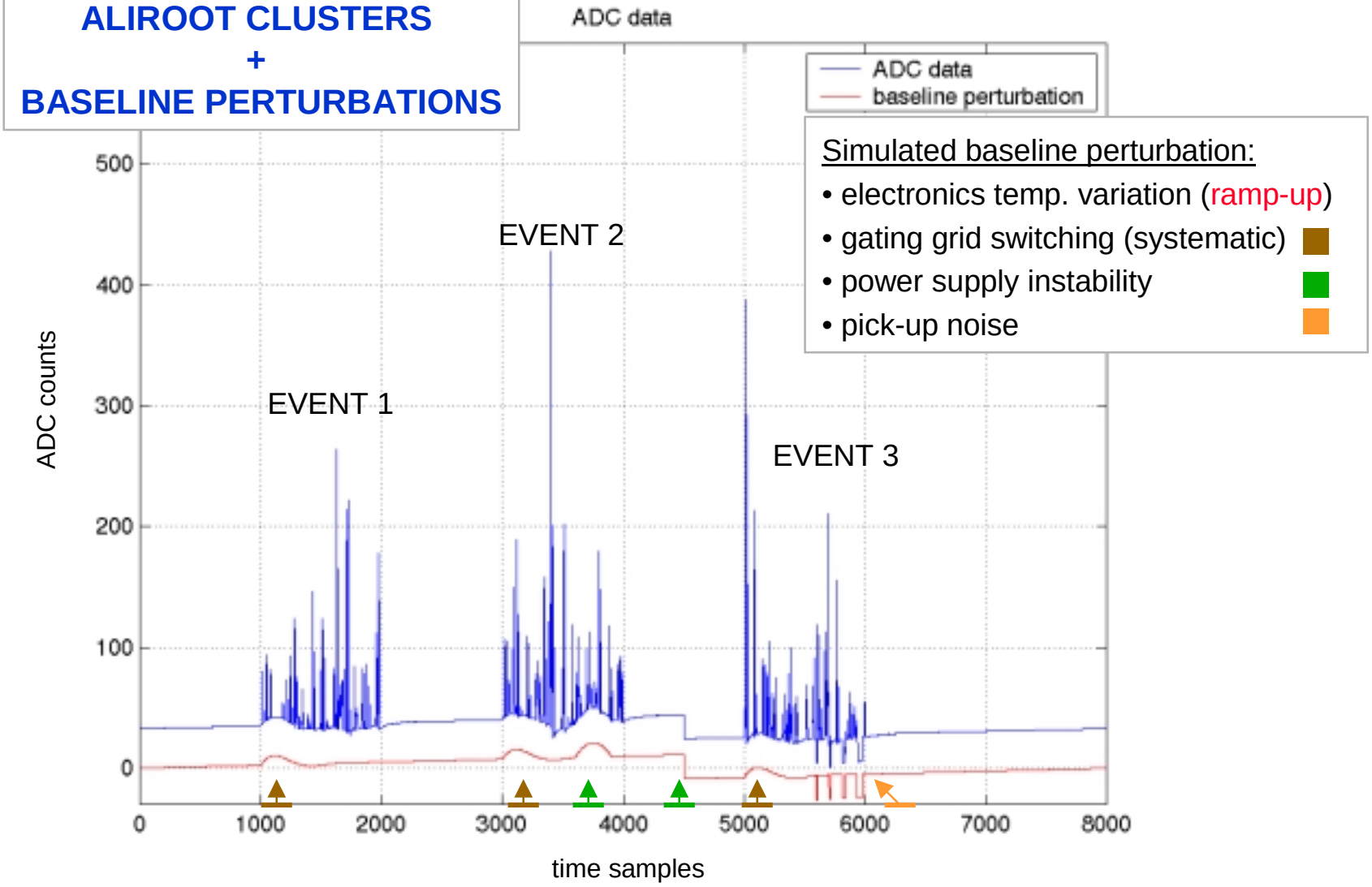
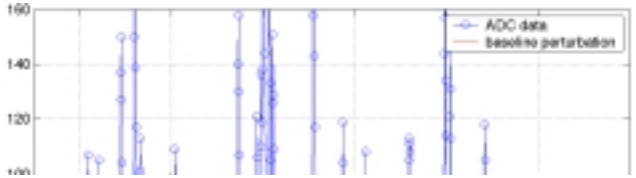
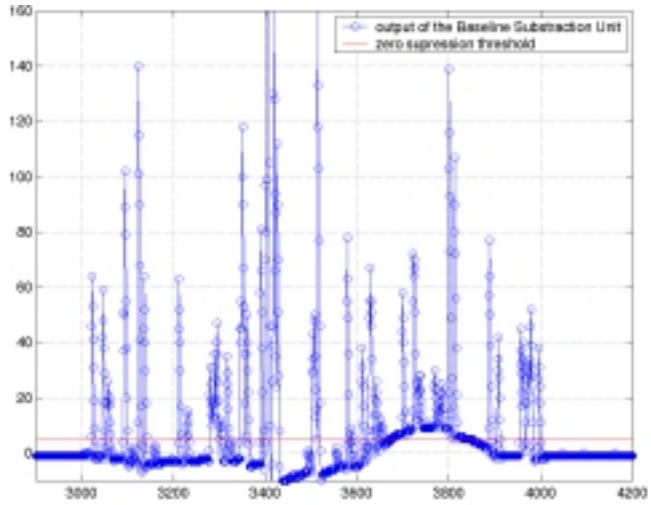
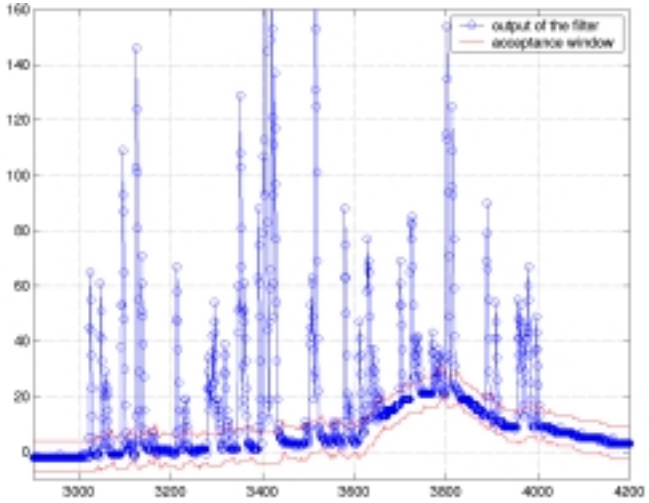
Functional Validation: Realistic Input Pattern

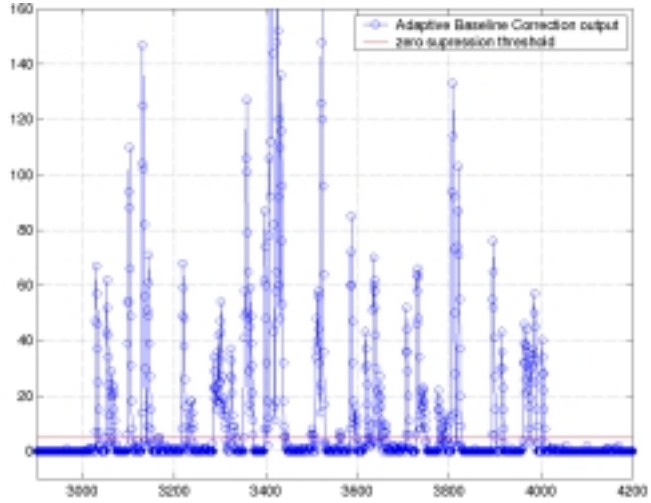
ALIROOT CLUSTERS
+
BASELINE PERTURBATIONS




ADC data
baseline perturbation


output of the Baseline Substraction Unit
zero supression threshold


output of the filter
acceptance window


Adaptive Baseline Correction output
zero supression threshold