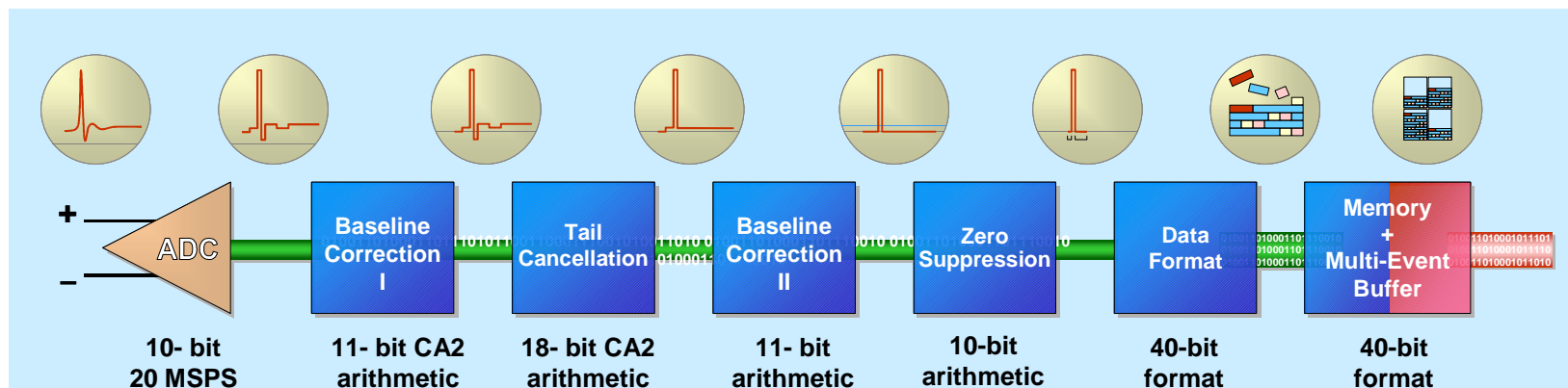


# Contents

---

- **ALTRO Implementation**
- **ALTRO Test Setup and Equipment**
- **ADC Characterisation**
- **Noise and Crosstalk**
- **Power Consumption**
- **ALTRO Testing Strategy**
- **Functional and Physical Validation**
- **Yield Results and Considerations**
- **Conclusions**

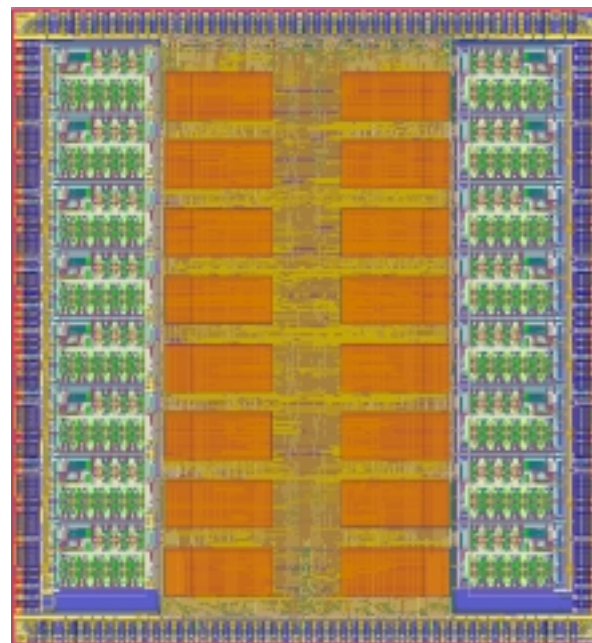
# ALICE TPC READOUT CHIP (ALTRO-16)



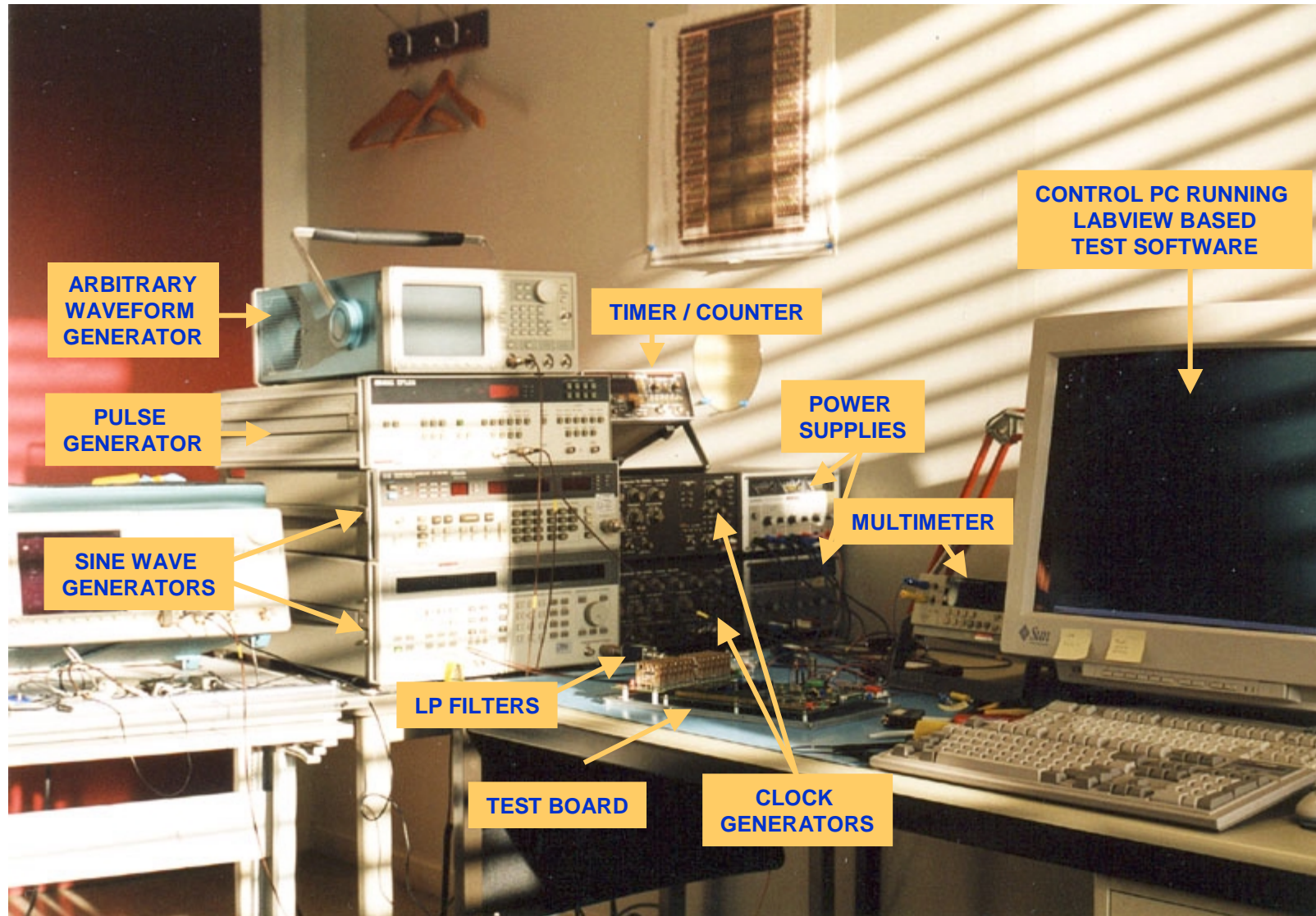
- MAX SAMPLING CLOCK 40 MHz
- MAX READOUT CLOCK 60 MHz

## 16-ch signal digitizer and processor

- ◆ HCMOS7 0.25  $\mu\text{m}$  (ST)
- ◆ area: 64  $\text{mm}^2$
- ◆ power: < 20 mW / ch
- ◆ prototype delivery: Feb '02
- ◆ 300 samples fully tested

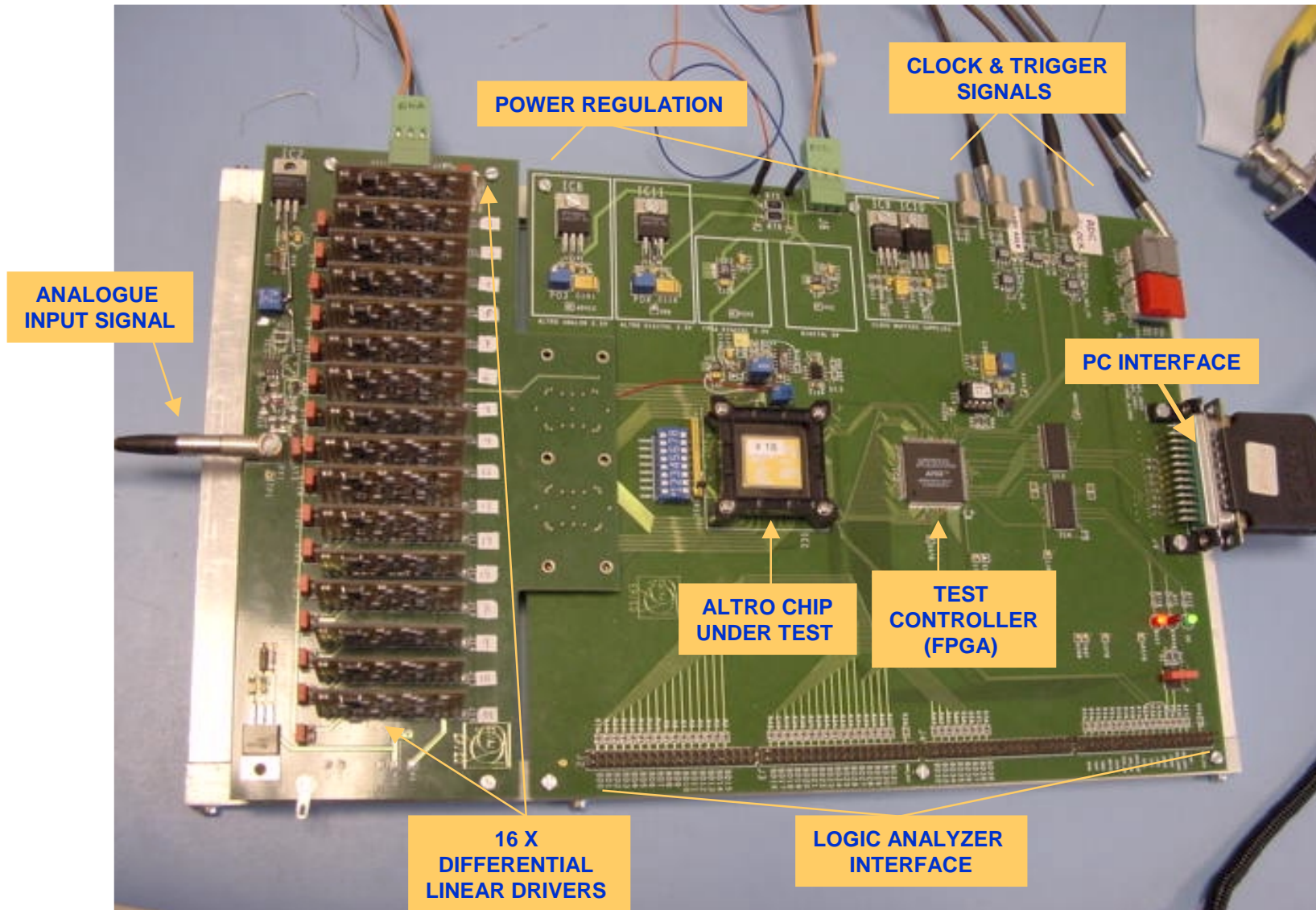


# ALTRO Test Setup

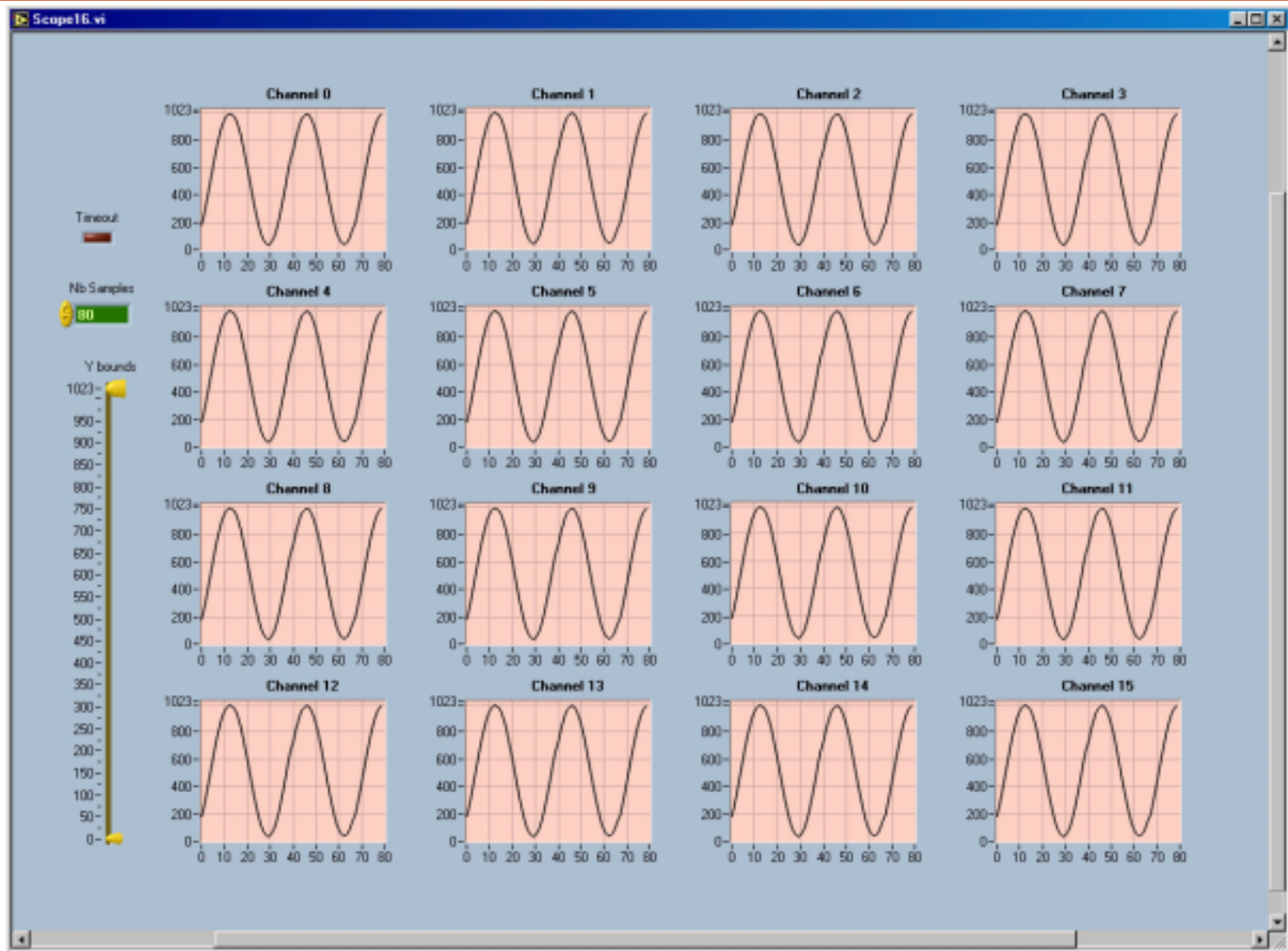




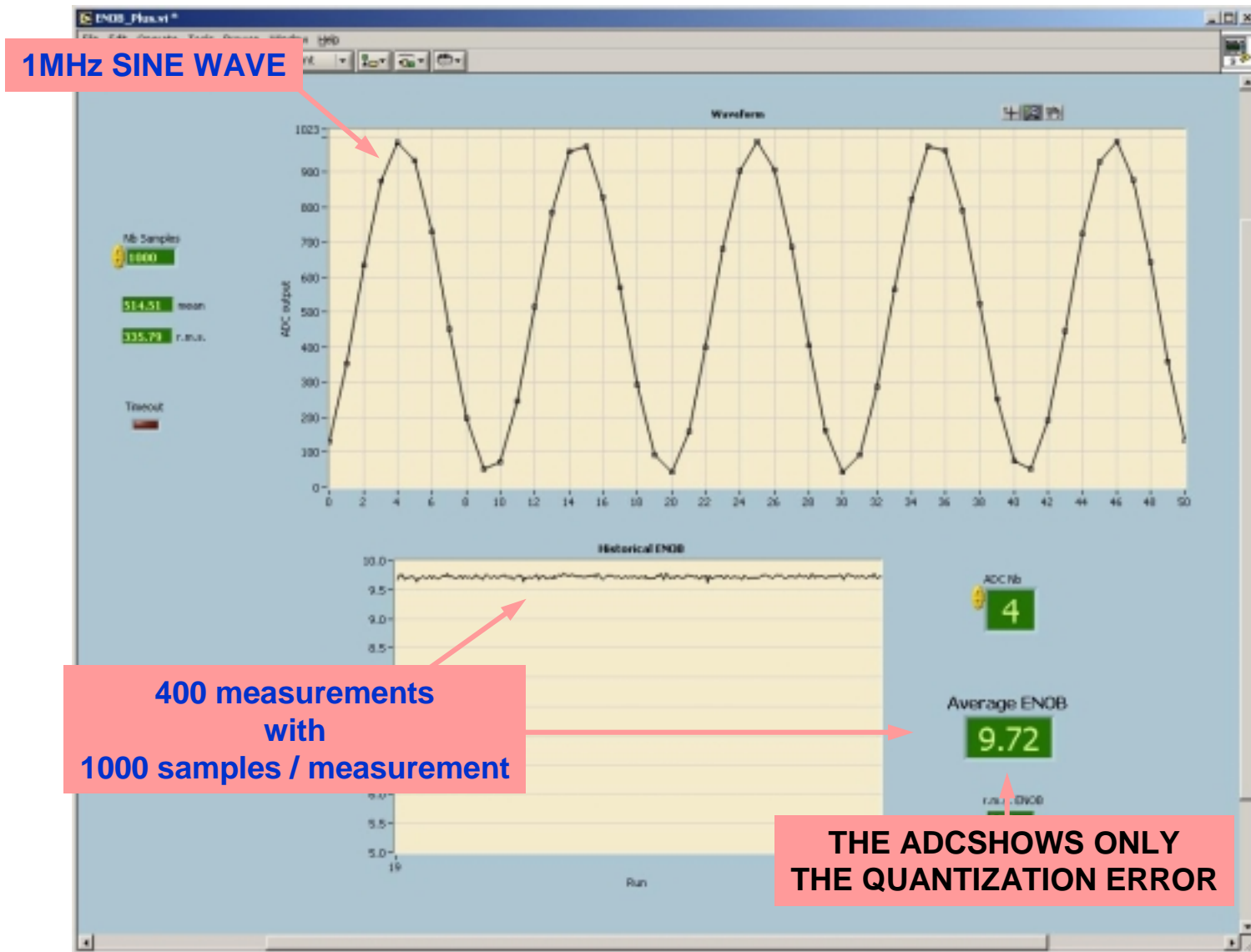
# ALTRO Test Board



# 16 channels in one shot

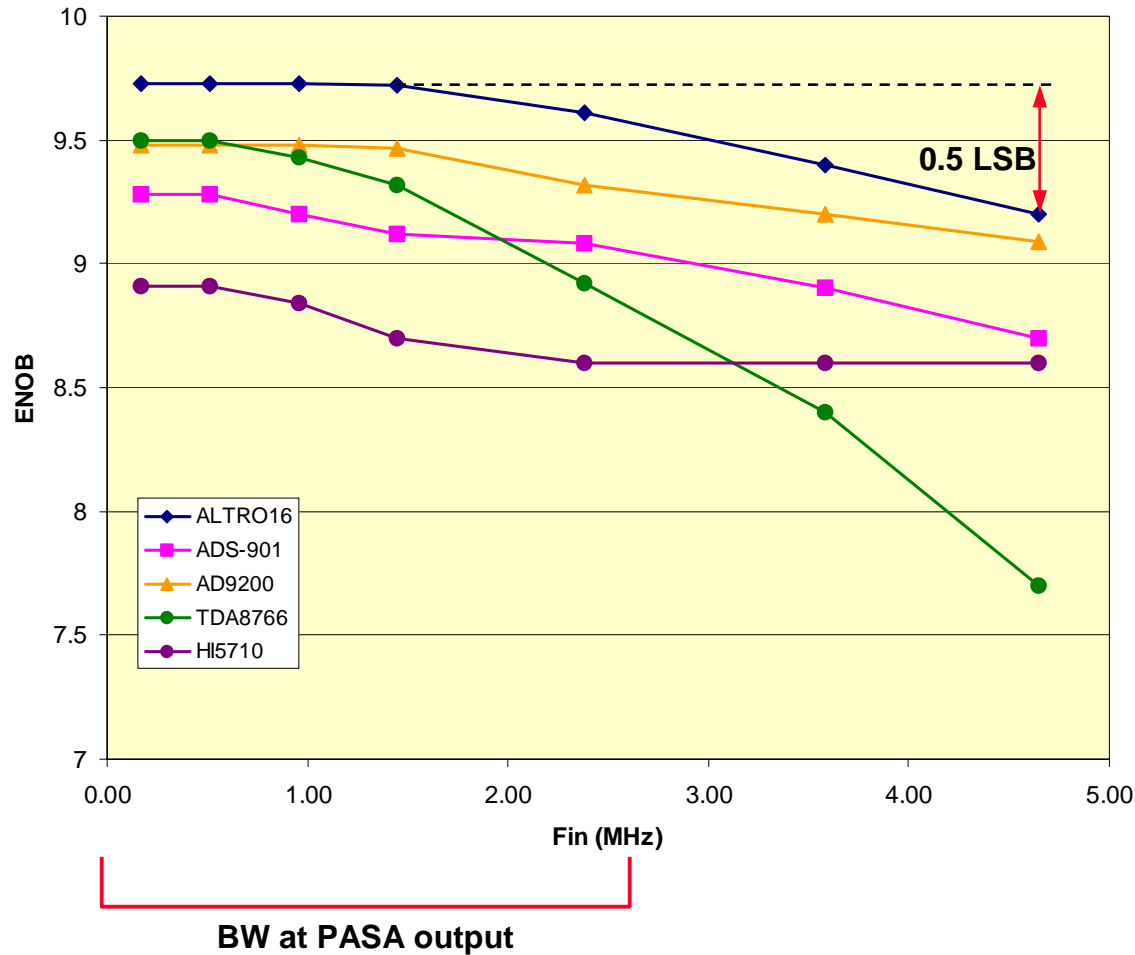


# Effective Number of Bits (ENOB)



# ENOB vs Frequency

Effective Number of Bits vs Input Frequency



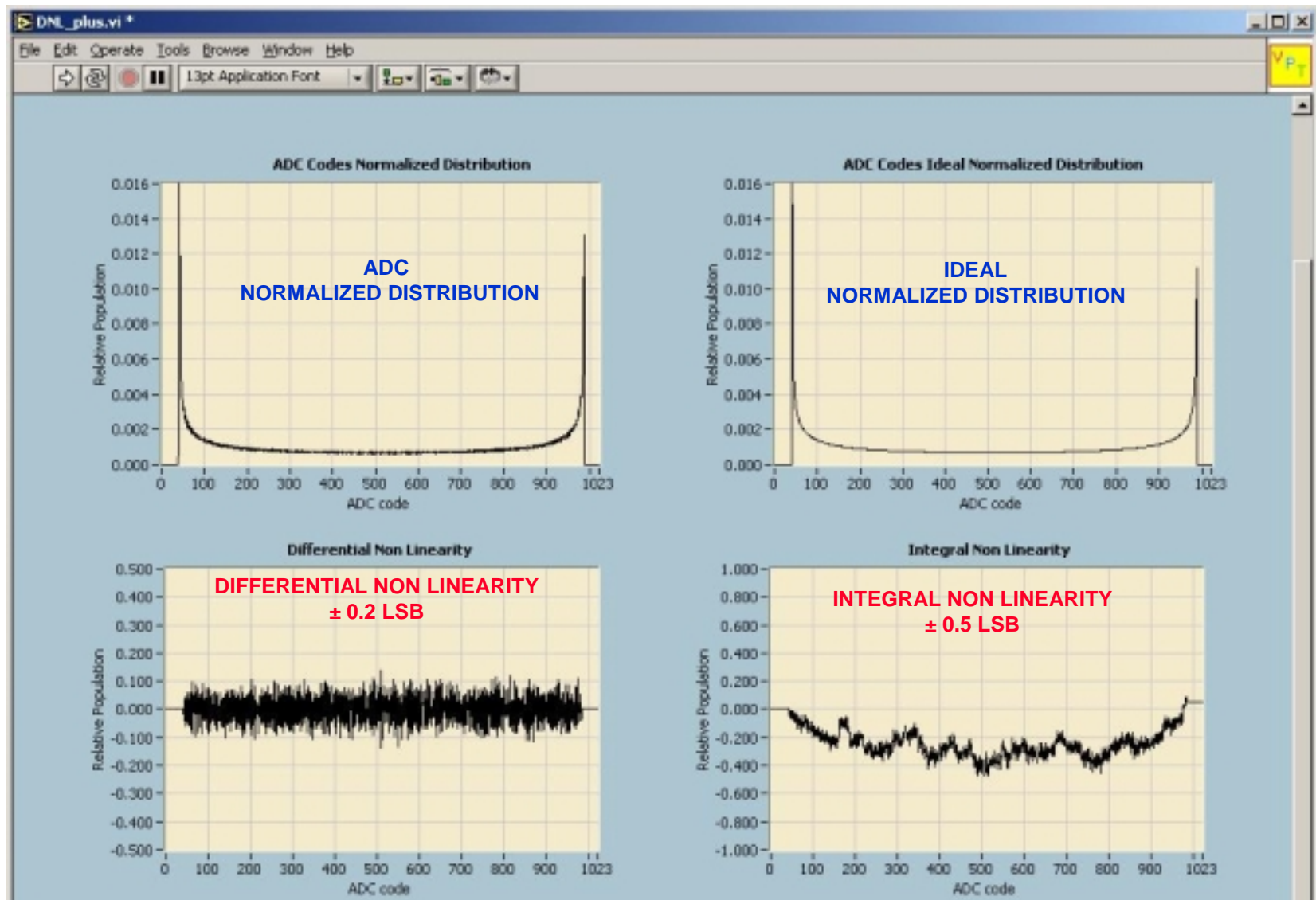
Quartz Jitter:  
 25ps r.m.s.  
 100ps absolute

Amplitude Uncertainty:

$$\frac{\text{jitter}}{4 \cdot f_{in}} \cdot 2^{10}$$

0.5 bits at 4.8 MHz

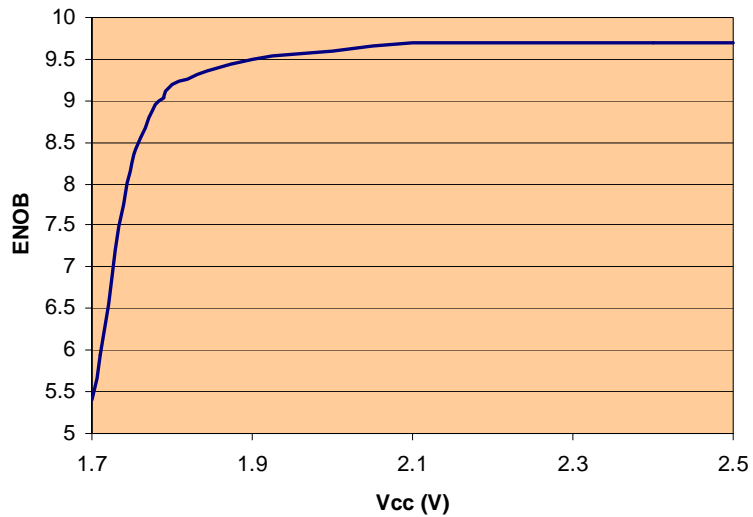
# Differential and Integral Non-Linearity



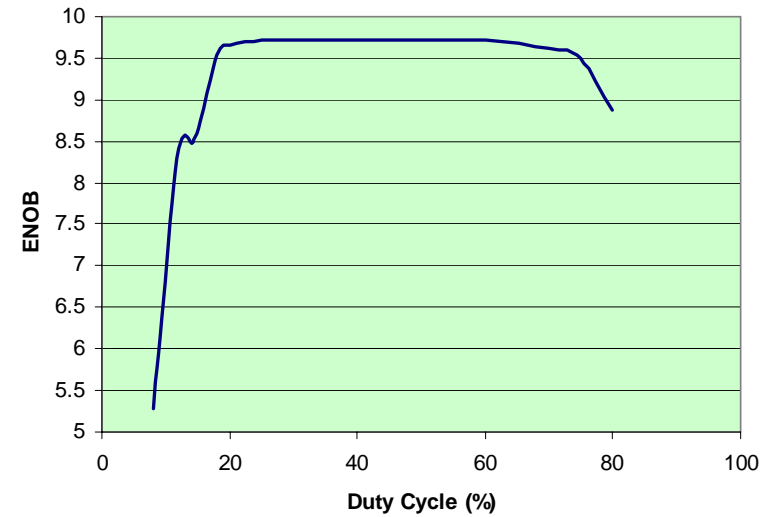


# Chip Performance

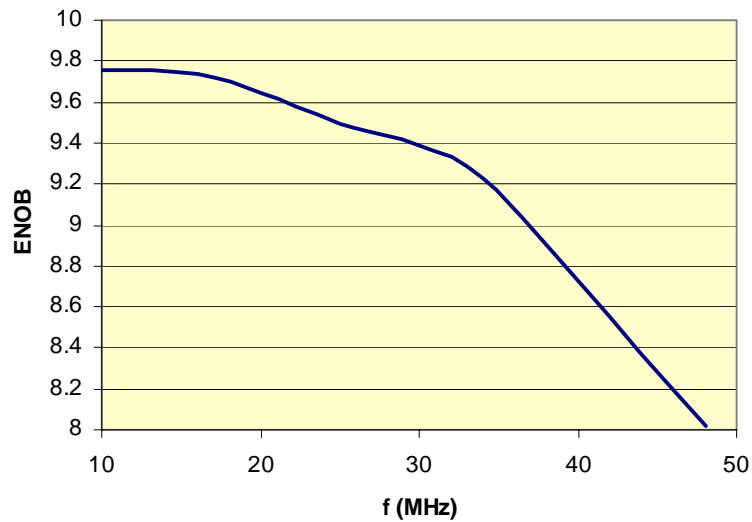
ENOB vs Analog Vcc



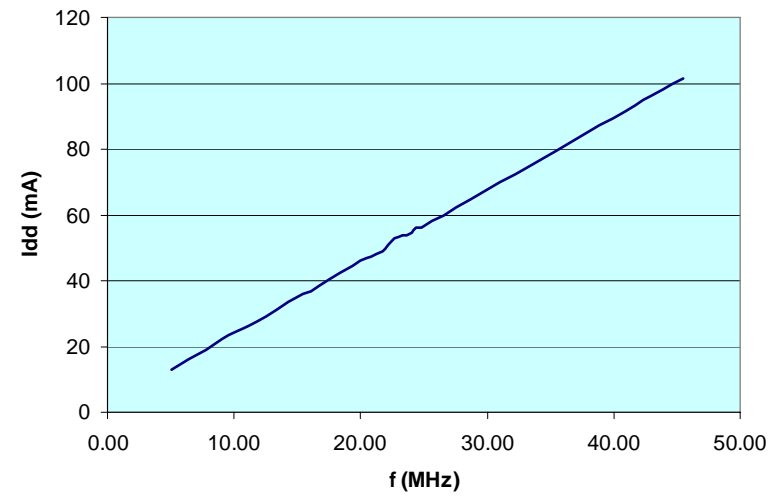
ENOB vs Duty Cycle



ENOB vs Sampling Frequency

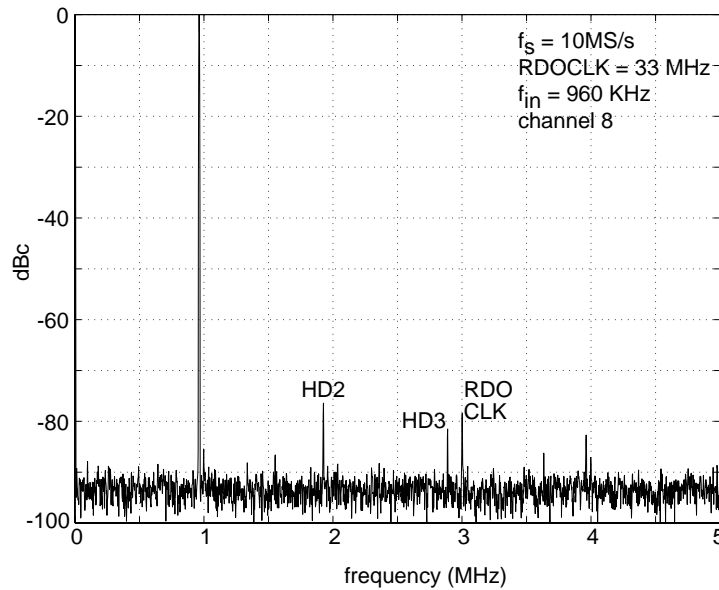


Digital Power Consumption vs Sampling Frequency

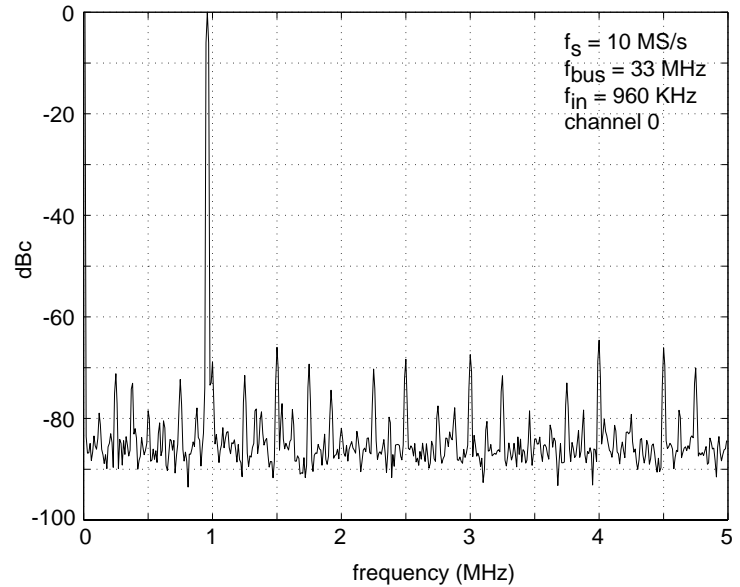


# Crosstalk and Digital Noise

DIGITAL NOISE



Readout Clock below -78 dBc (WC)



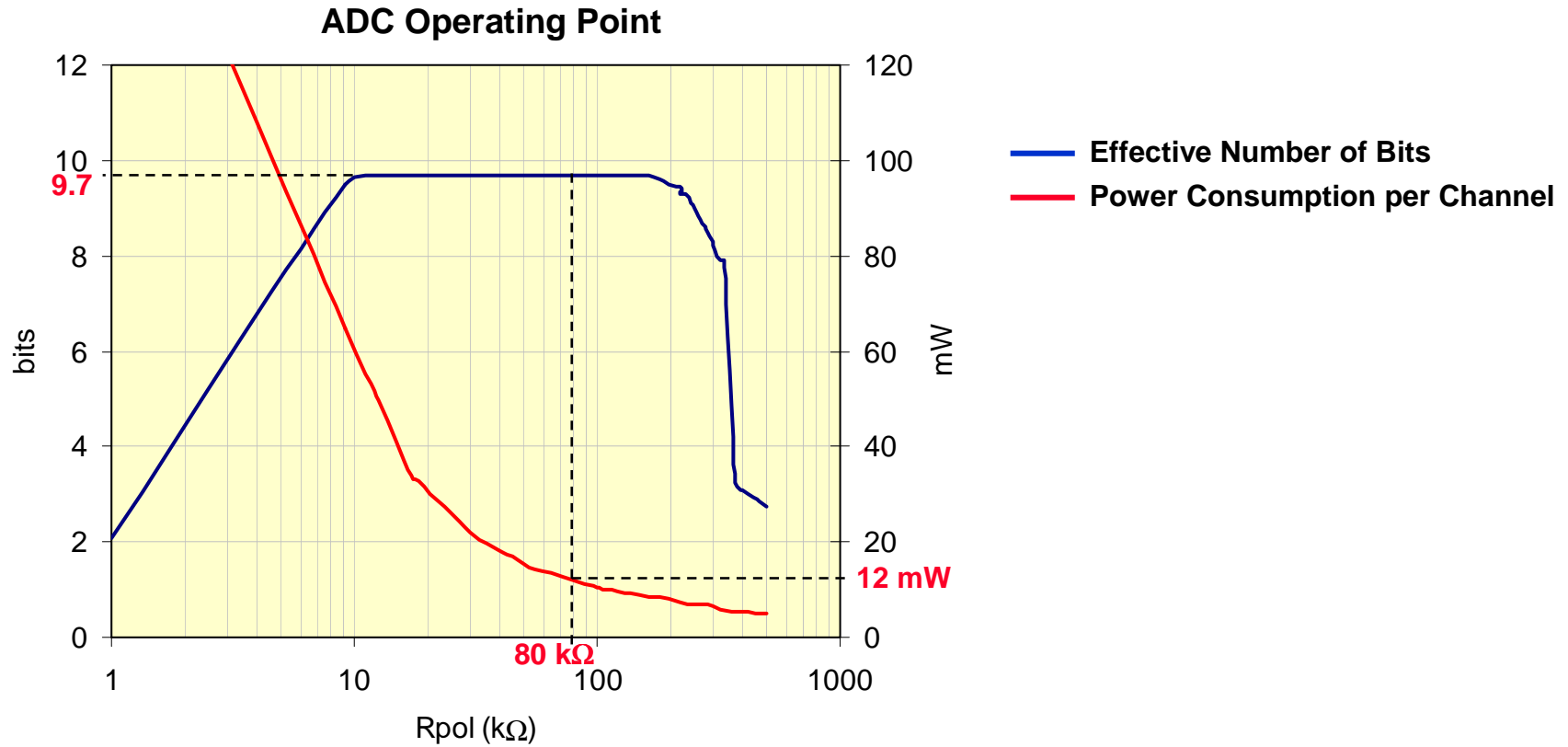
Bus interference below -65 dBc (WC)

## CHANNEL-TO-CHANNEL CROSSTALK

$F_{in} = 1\text{ MHz}$     0.05 LSB rms    (-80 dBc)  
 $F_{in} = 5\text{ MHz}$     0.2    LSB rms    (-68 dBc)

Dynamic Range of a 10-bit ADC: 60 dB

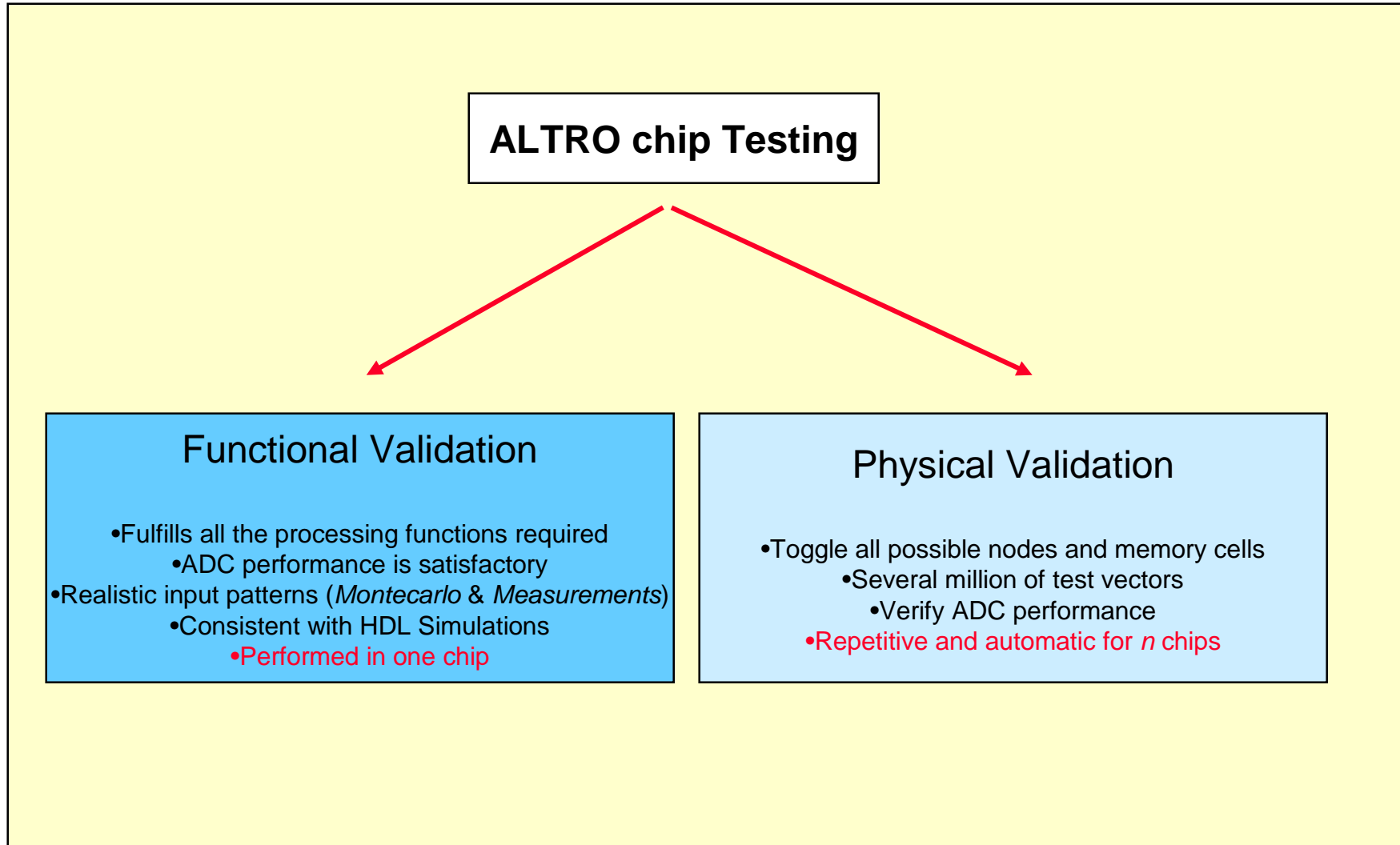
# Power Consumption



<b>ONE CHIP</b>	Digital leakage current	1.2 mA
	ADC Clock Tree (10 MHz)	23 mA
	Readout Clock Tree (40 MHz)	1.4 mA
	Processing Logic during Trigger (1%)	28 mA
	16 ADCs at 10 MS/s	77 mA

Average Power Per Chip	<b>257 mW</b>
Average Power Per Channel	<b>16 mW</b>

# Testing Strategy



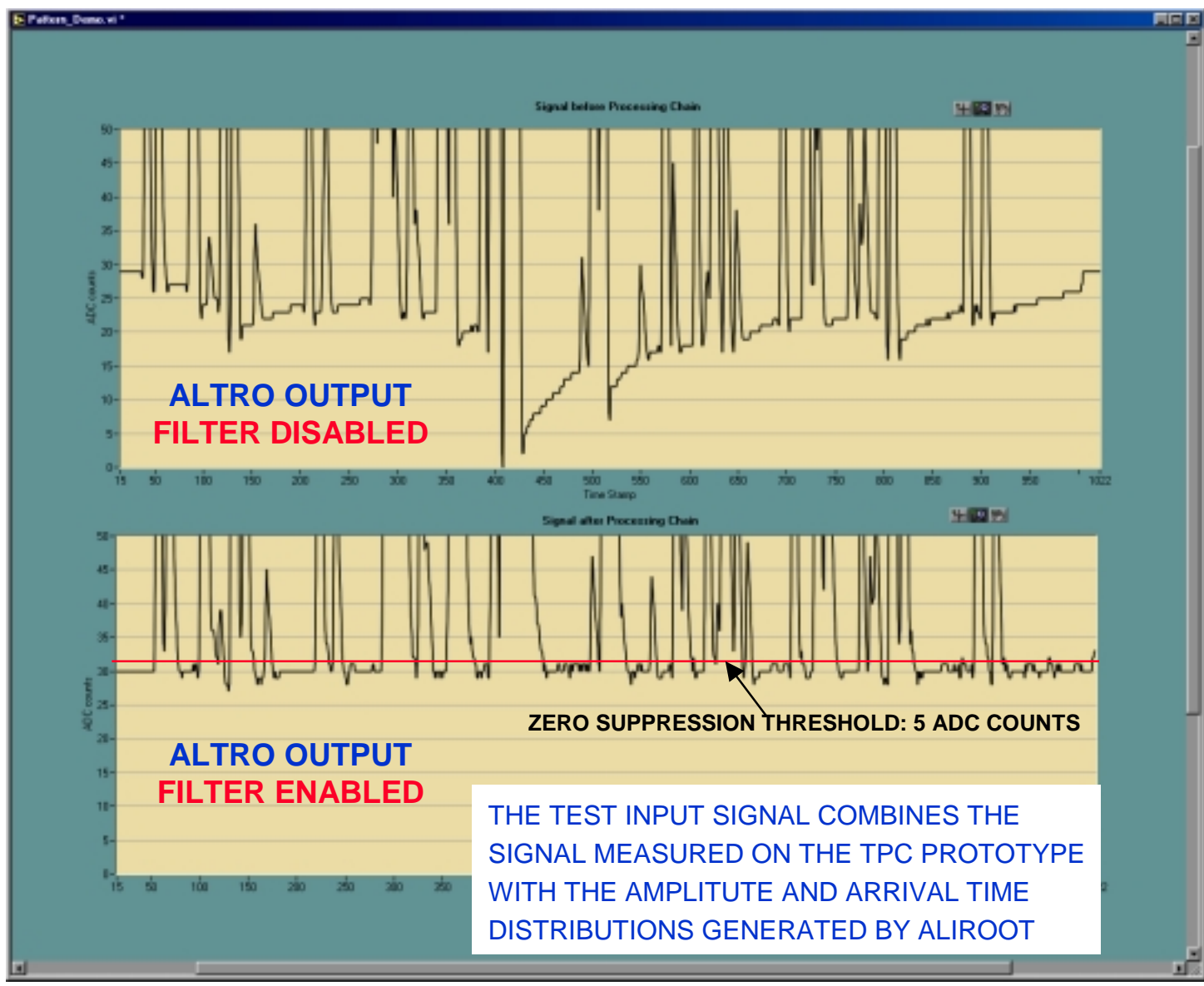


# Functional Validation: Register Control Panel

The screenshot displays the Register Control Panel for the ALTRO CHIP, organized into several functional sections:

- Baseline Correction 1:** Features a waveform plot with a y-axis from 0 to 1023 and an x-axis from 0 to 1023. Controls include Mode (f(t) - fpd), VPD (508), FPD (0), Power Save (enabled), and Polarity (Norm).
- Multi-Event Memory:** Shows Event Buffers (4/8), empty/full status, Write Pointer (0), Read Pointer (0), Available Buffers (4), and Last Event Length (0).
- Errors:** Includes Readout Error, Trigger Overlap, Instruction Error, Parity Error, and SEU (Double/Simple Upset) for both Interface and Memory Unit.
- Tail Cancellation Filter:** Has an Enable toggle and six gain settings (K1-L3) ranging from 0.75737 to 0.99560.
- Baseline Correction 2:** Includes an Enable toggle, LO/Hi Thresholds (7), and Presamples/Postsamples (1).
- Zero Suppression:** Features an Enable toggle, Offset (0), Glitch Reject (Off), Threshold (0), and Presamples/Postsamples (0).
- Trigger:** Controls Samples per Event (0), Trigger Delay (0), Pretrigger (0), and shows a Trigger Counter of 136.
- Bottom Panel:** Contains Channel (0), Chip Address (0), Read All/Write All buttons, Verify on Write toggle, and status indicators for Unwritten Changes, Verification Error, and Tx/Rx Error.

# Functional Validation: Realistic Input Pattern



# Functional Validation: Realistic Input Pattern

