Irradiation results

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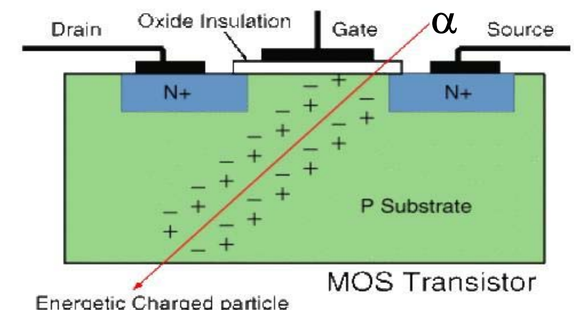
- SEU
- Test setup
- Cross section measurement
- Error estimate per run

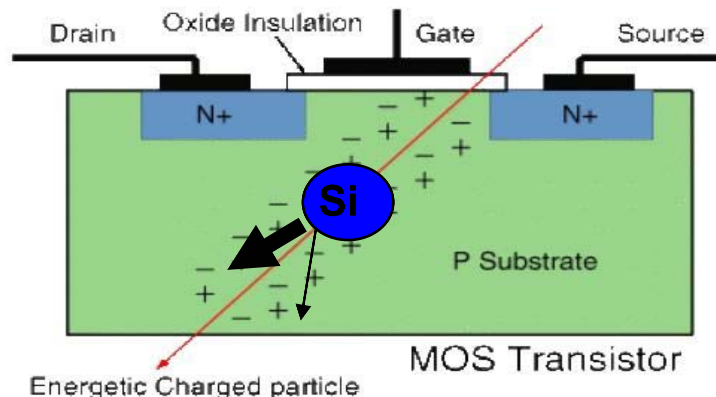
Single Event Upset (SEU)

- Charge deposition by ionizing particle can lead to a change in state of a transistor
- Critical charge $Q_{crit} = 0.0023\ pC/\mu m^2 \bullet L^2$
  L = feature size (APEX 20k400: $L=0.18\ \mu m$)
- Energy deposition $E_{dep} = LET \bullet \rho \bullet s$
  ρ = density (Si: $\rho = 2.33\ g/cm^3$);
  s = path length ($s^2 = 2L^2 + c^2$, c = device depth)
- Charge deposition $Q_{dep} = E_{dep} \bullet q / w_{ehp}$
  w_{ehp} = electron-hole pair creation energy (Si: $w_{ehp} = 3.6\ eV$)
- $Q_{dep} > Q_{crit}$: SEU -> minimum LET: $LET_{threshold}$
- $LET_{threshold}$ (APEX) $\approx 100\ keV/mg/cm^2$
- LET(30 MeV proton in Si) = $15\ keV/mg/cm^2$



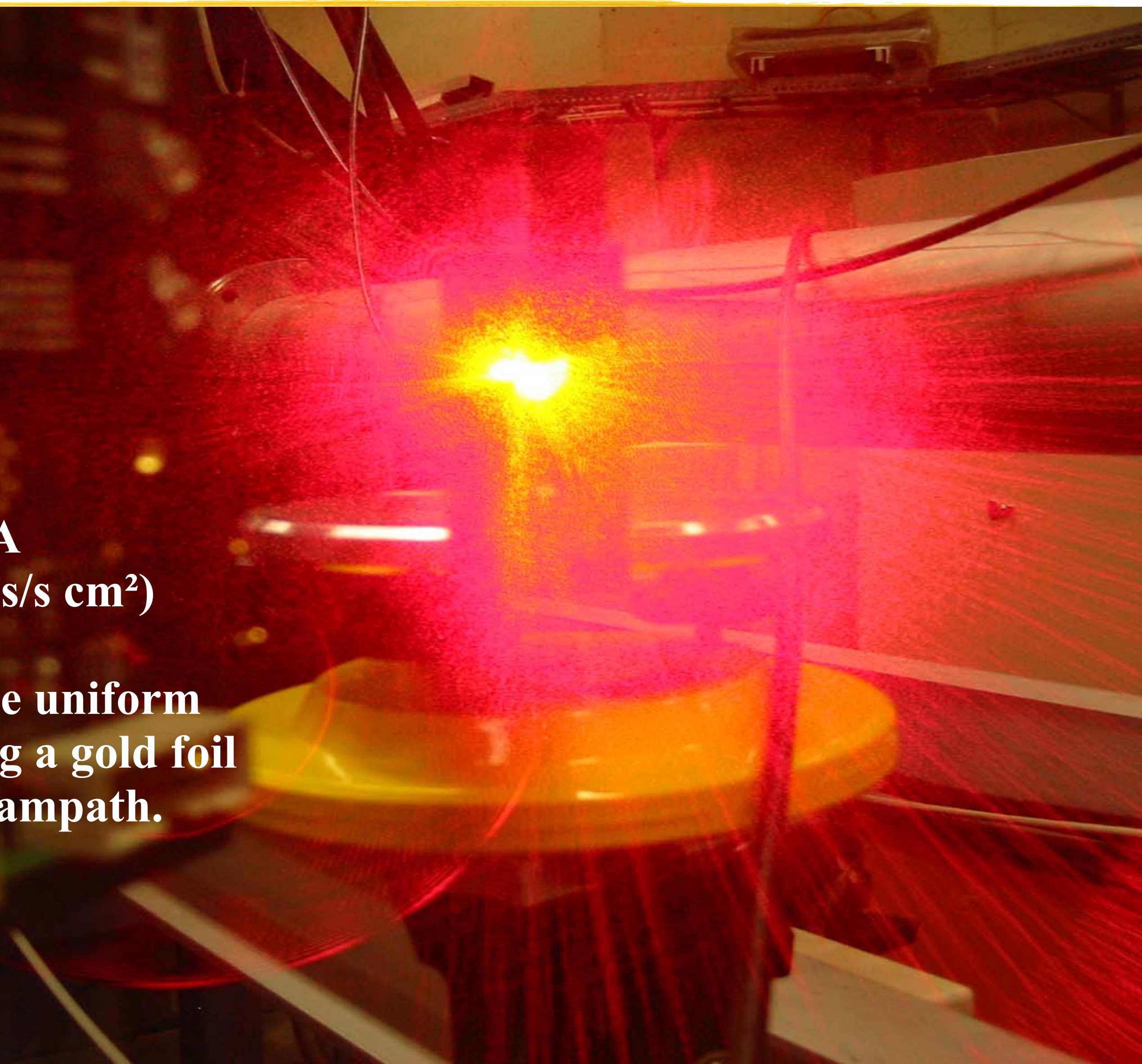
Single Event Upset (SEU)

- High-energetic hadrons induce nuclear reactions in the silicon (E > 20 MeV - protons, neutrons, pions, kaons)
- Intermediate energy neutrons (2 MeV < E < 20 MeV) contribute little (10%) to SEUs
- (Almost) no effect due to thermal neutrons
- Heavy recoil ions from reactions ionize the material
- Protons do not deposit enough charge deposited by direct ionization to cause a SEU
- Charge deposition leads to a change in state of a transistor (SEU)
- Soft error – can be corrected (rewriting or reprogramming)



- Si(p,2p)Al
- Si(p,pα)Mg
- Si(n,p)Al
- Si(n,α)Mg
- Spallation

Test setup



Oslo Cyclotron

- 29 MeV external proton beam
- beamspot 1 x 1cm
- beam intensities > 10pA (flux : 0.6x10^8 protons/s cm²)
- beam distribution made uniform by defocusing and using a gold foil placed upstream in beampath.

Upset detection in ALTERA FPGAs

Two types of concern

- Upsets in configuration SRAM cells
- Single bitflips in register elements

The APEX20K400E offers no direct readout of configuration SRAM

-*Indirectly detection* of configuration upset through the VHDL design

Error observed reflects a change in logic due to a configuration upset, and not the configuration upset itself

Upset detection

Possibility of undetectable configuration upsets

-Not 100% usage of SRAM bits --> some upset do not influence logic

-Test results give an *estimate* of configuration upsets.

First glance – configuration upsets and single bitflips induced in logic look the same

-Distinguishable by looking at them over time

-Configuration upset: Permanent until reprogramming of device

-Single upsets: Limited in time, present until *next clock cycle*

Task: Design hardware that detects SEU's in both logic and internal RAM blocks of the device

VHDL design

-32 bit wide and 400 bit long **shiftregister** implemented in **logic elements** (approx. 90% of the LEs)

-32 bit wide and 4096 bit deep **FIFO** implemented in **internal RAM** blocks (approx 60% of the internal RAM bits)

Upset detection

A fixed pattern is shifted through and compared for setups when read out.

Communication through SCSN (Slow Control Serial Network)
-Introduces problem of SEUs in the SCSN

Software on Linux PC to read out and analyse data (C, Matlab)

Data in

0000000
1000000
0100000
0010000
0001000
0000100
0000010
0000001
0000000
0000000
.
.
.
0000000

FPGA

Serial Slow Control Network

SCSN

D Q Clk

Serial Slow Control Network

SCSN

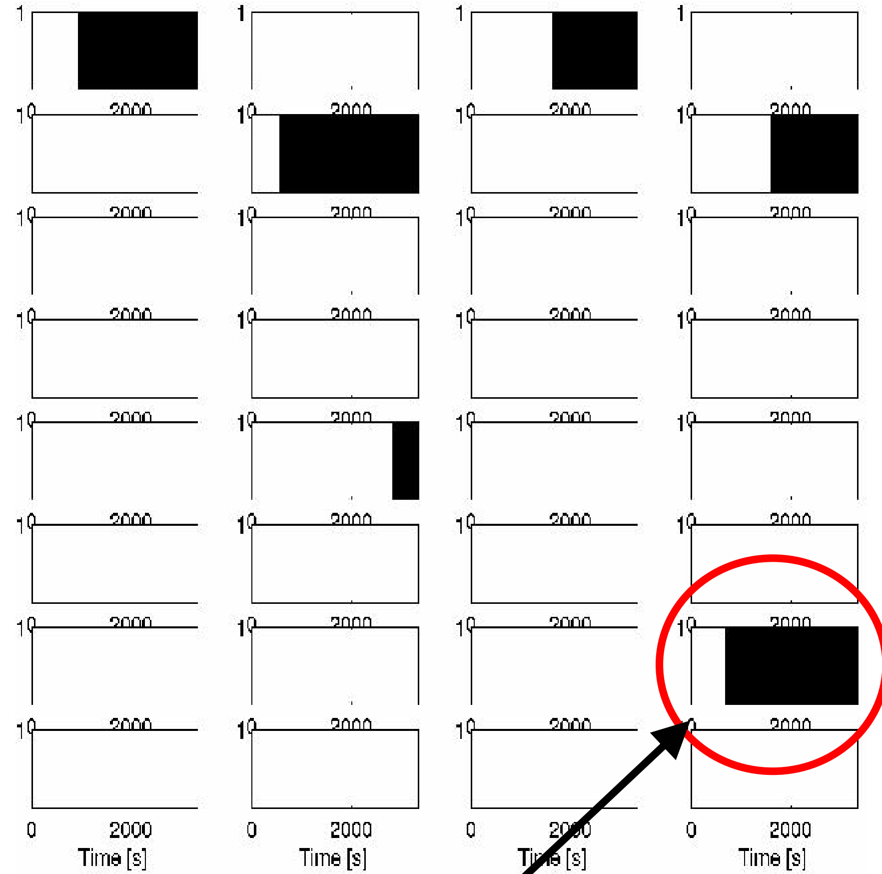
Data out

0000000
1000000
0100000
0010000
0001000
0000100
0000010
0010001
0000000
0000000
.
.
.
0000000

Example of analyzing data

FIFO in internal RAM

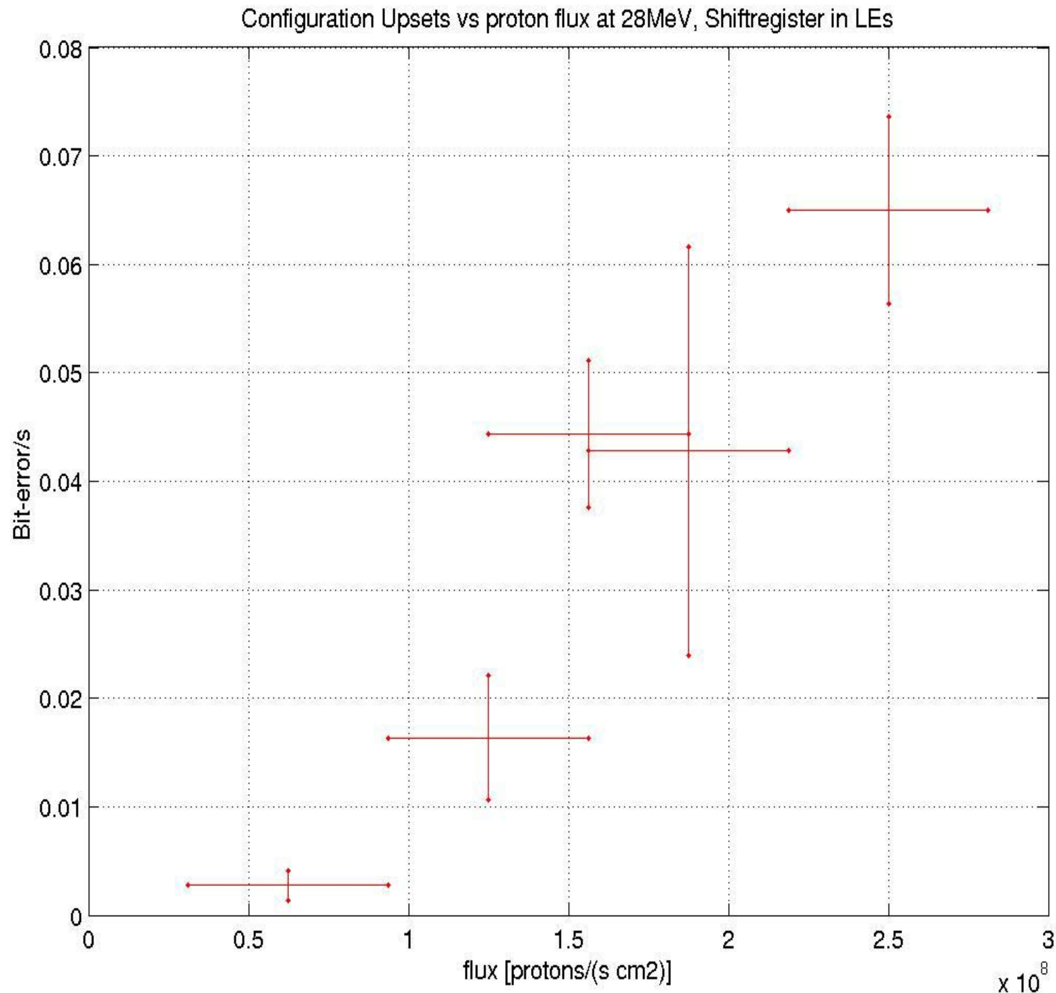
Shiftregister in logic elements



Single upset

Configuration upset

Preliminary results



Observations

Configuration upsets in logic and internal RAM

Single upsets in internal RAM only

- **Many interconnection in logic elements**
- **Low density of SRAM cells compared to internal RAM blocks**

- SEU - uncorrelated
- Expecting linear dependency

Cross section results

- General observation
  - No SEU at a proton beam energy of 10 MeV
  - Dependence on orientation of device in respect to beam direction
    - » increase of cross section by a factor of 2 at 45° orientation as compared to 0°

Cross section results

- FPGA APEX 20K400

	Cross section [cm^2]
Configuration RAM	
Logic	$1.9 \times 10^{-10} \pm 0.8 \times 10^{-10}$
Internal RAM	$1.5 \times 10^{-10} \pm 0.8 \times 10^{-10}$
Single upsets	
Logic	$<5.3 \times 10^{-12}$
Internal RAM	$4.1 \times 10^{-10} \pm 2.2 \times 10^{-10}$

- FPGA ACEX 1K30

	Cross section [cm^2]
Configuration RAM	4×10^{-11}

Cross section results

- External compoments

	Cross section [cm^2]
External SRAM	$\approx 2 \times 10^{-10}$
SDRAM	$\approx 3 \times 10^{-11}$

- FLASH errors after 7×10^{11} protons

- FPGA EPX1

	Cross section [cm^2]
ARM core program	1.5×10^{-10}

Error estimates per run

Particle E > 10 MeV	Fluence [cm^{-2}] per 10 ALICE years (Simulation 1, non-absorber & absorber side)	Fluence [cm^{-2}] per 10 ALICE years (Simulation 2, incl. absorber side)
Protons	6×10^8 3×10^8	8.6×10^8
Pions, kaons	3.5×10^9 1.5×10^9	1.4×10^9
Neutrons (5%)	1.9×10^9 5×10^9	$\approx 10^{10}$? tbc

Particle E > 10 MeV	Flux [$sec^{-1}cm^{-2}$] (Simulation 1)	Flux [$sec^{-1}cm^{-2}$] (Simulation 2)
Protons	24 13	34
Pions, kaons	140 60	56
Neutrons (5%)	76 206	450? tbc

Error estimates per run

- High-energetic hadron flux:
  250 – 550 hadrons/ $sec^{-1}cm^{-2}$

	Error rate per run (4 hours) per device	Error rate per run (4 hours) per system
FEC	3×10^{-4}	1.4
RCU	1.5×10^{-3}	0.3
DCS	3×10^{-3}	0.6

Conclusion

- SRAM based FPGAs
  - SEU rate acceptable?
- Alternative: FLASH based FPGA (Actel)
  - Supposed to be radiation tolerant
  - Provide similiar resources
  - Irradiation tests are underway