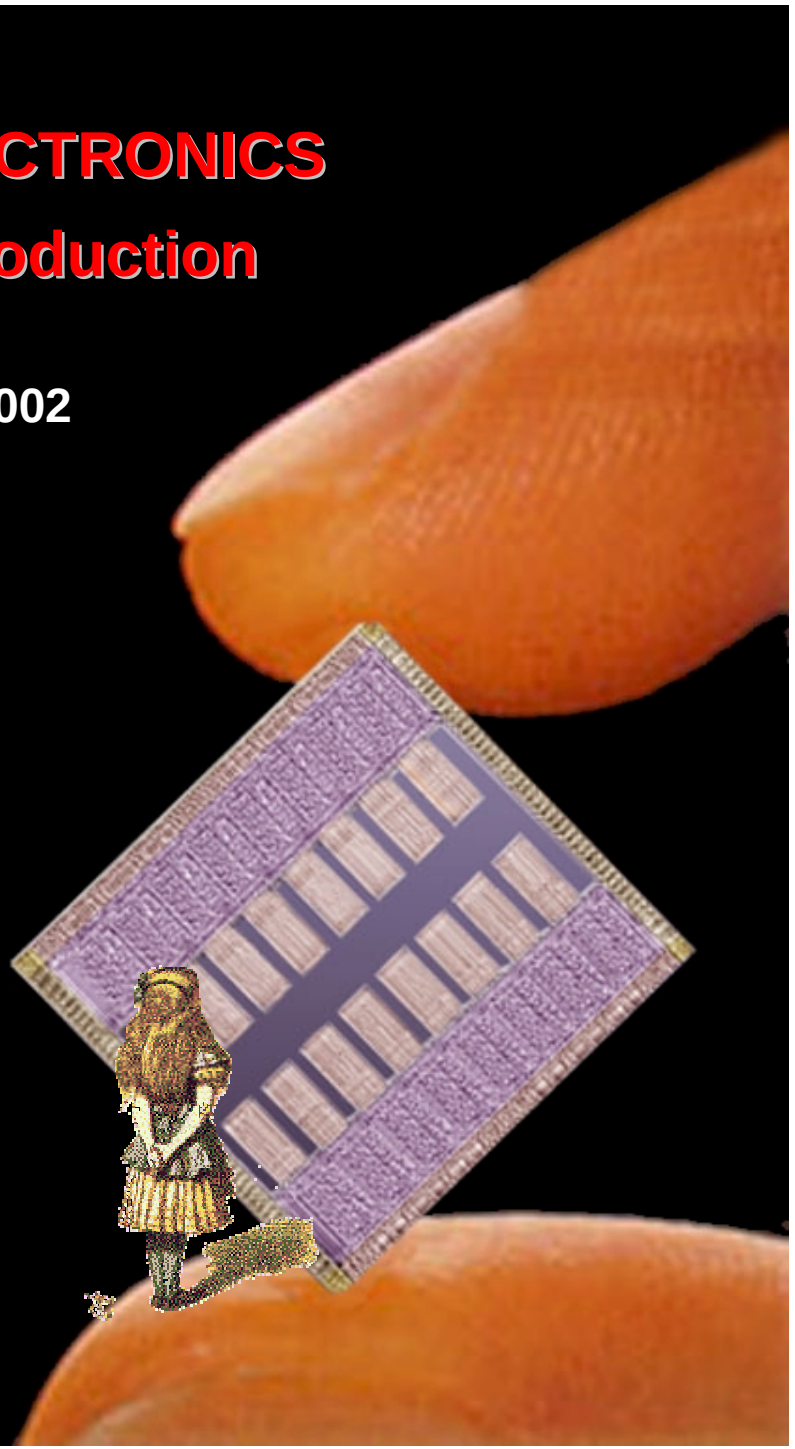
TPC FRONT END ELECTRONICS

Approaching the production

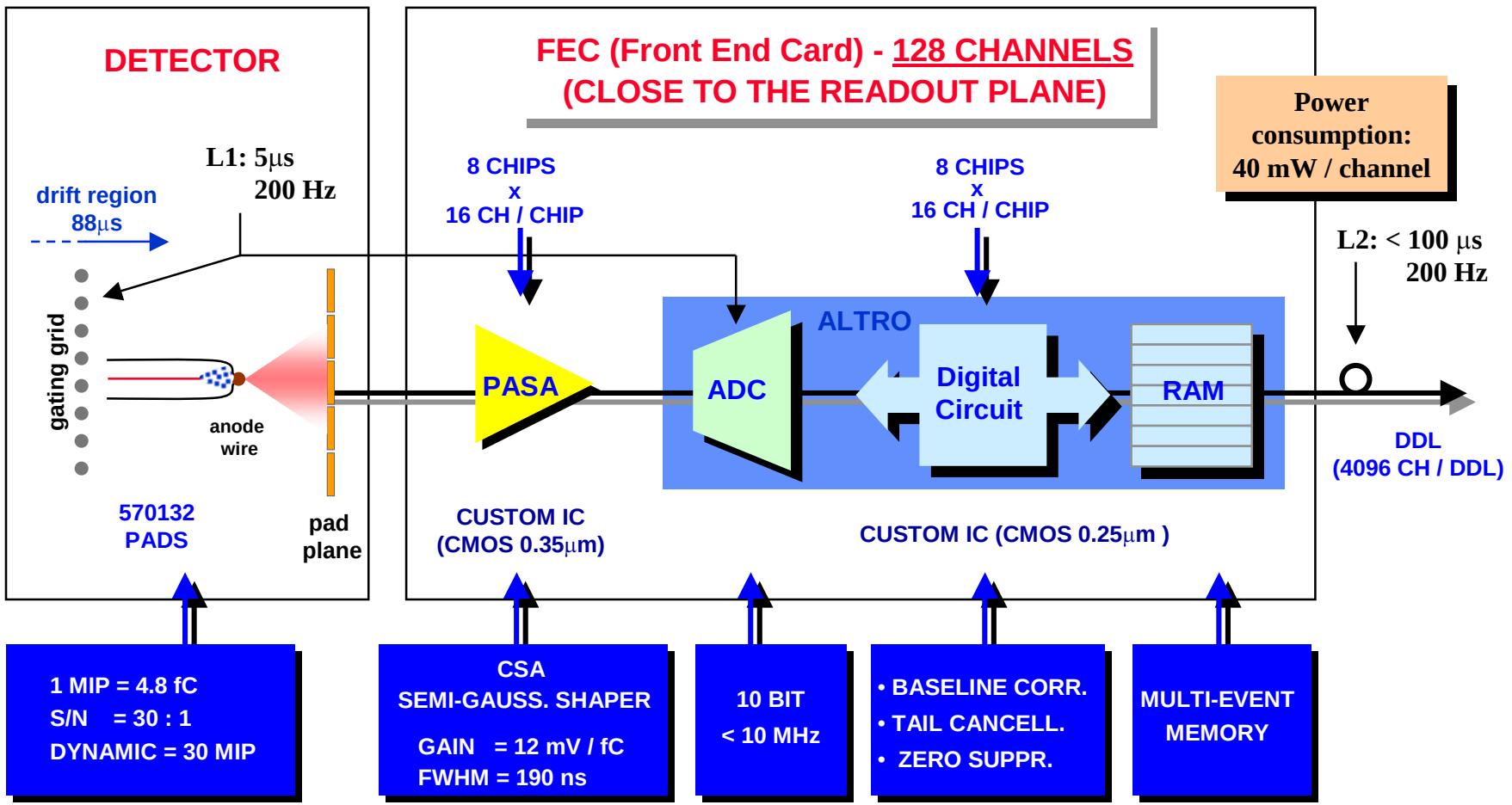
CERN – 21 June 2002

FEE TEAM: **Bergen**
CERN
Darmstadt TU
Darmstadt GSI
Frankfurt
Heidelberg
Lund
Oslo



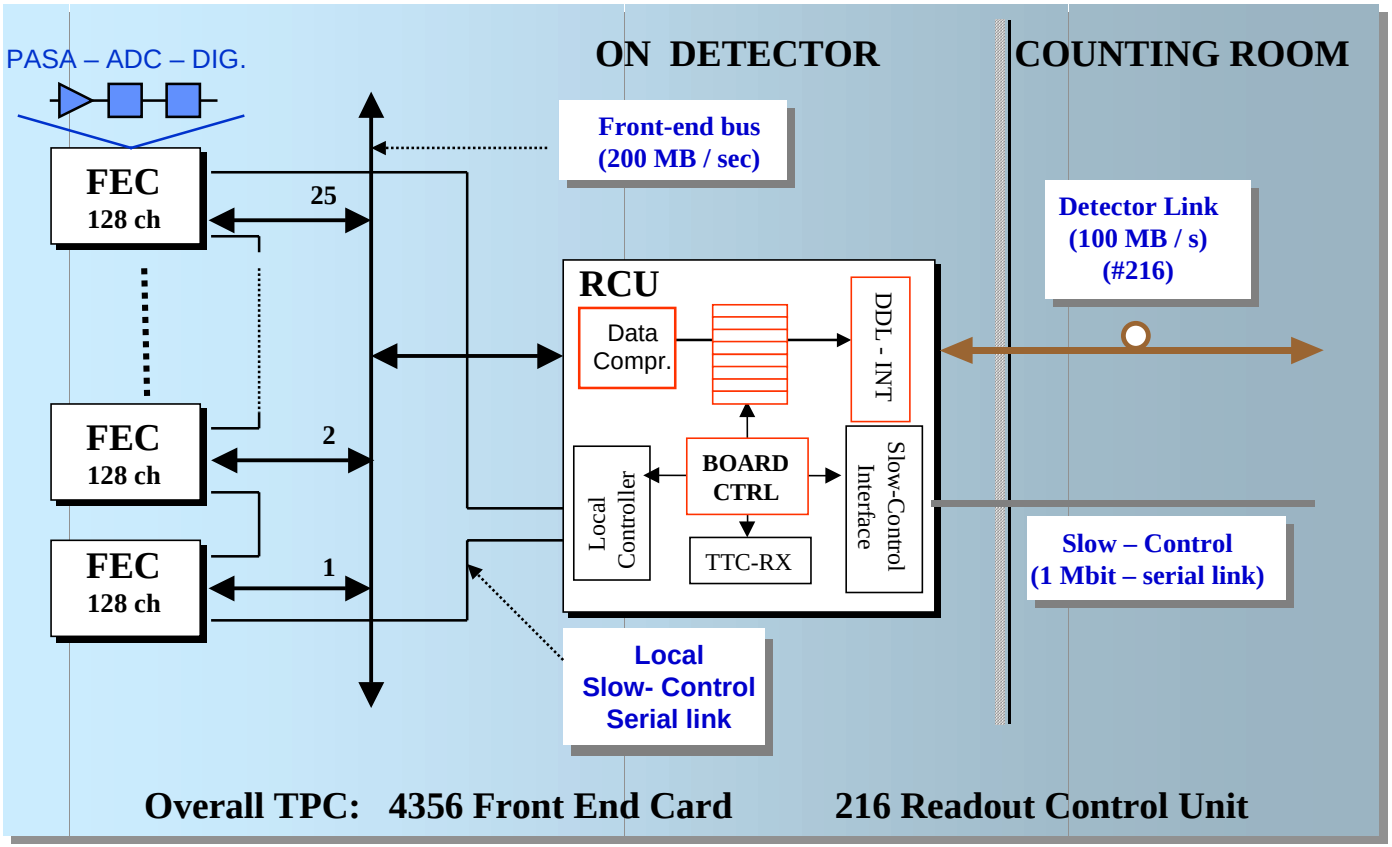
Luciano Musa - CERN

FEE ARCHITECTURE

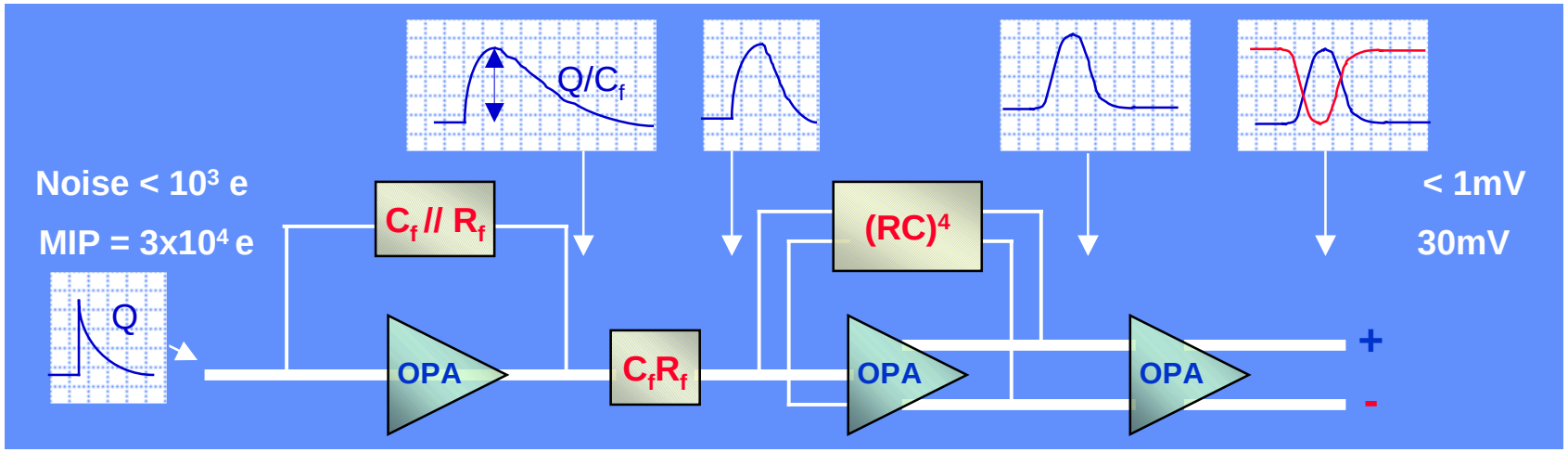


GLOBAL ARCHITECTURE

Each TPC Sector is served by 6 Readout Subsystems

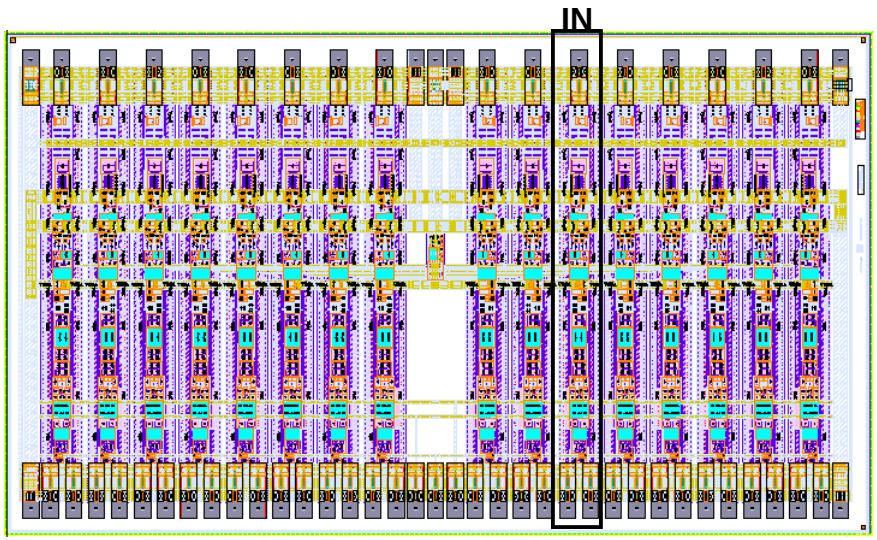


PRE-AMPLIFIER SHAPING AMPLIFIER (PASA) MAIN FEATURES



16-ch Amplifier / Shaper (PASA)

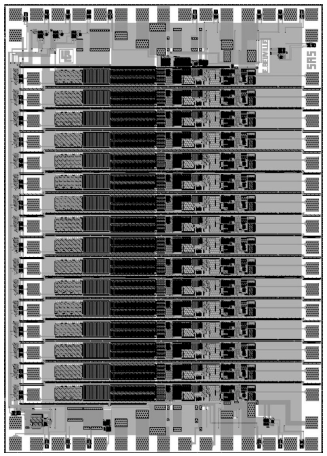
- CMOS 0.35 μm (AMS)
- Area: 16.7 mm²
- Power: 12 mW / ch
- Gain: 12mV / fC
- Noise: 400 e
- Crosstalk: < 0.4%



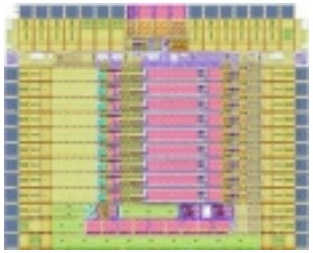
CHIP LAYOUT

THE PASA CONTEST

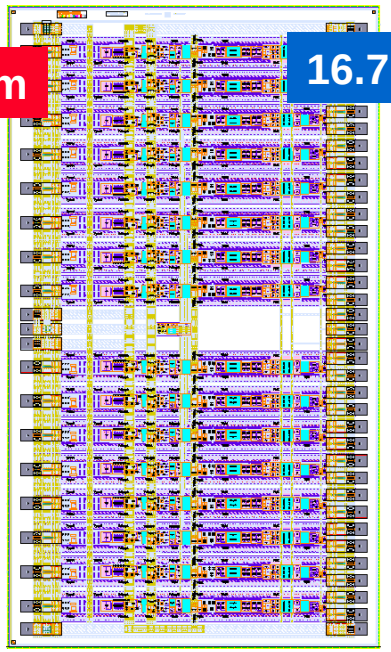
1.2μm 9.36 mm²



0.35μm 5 mm²

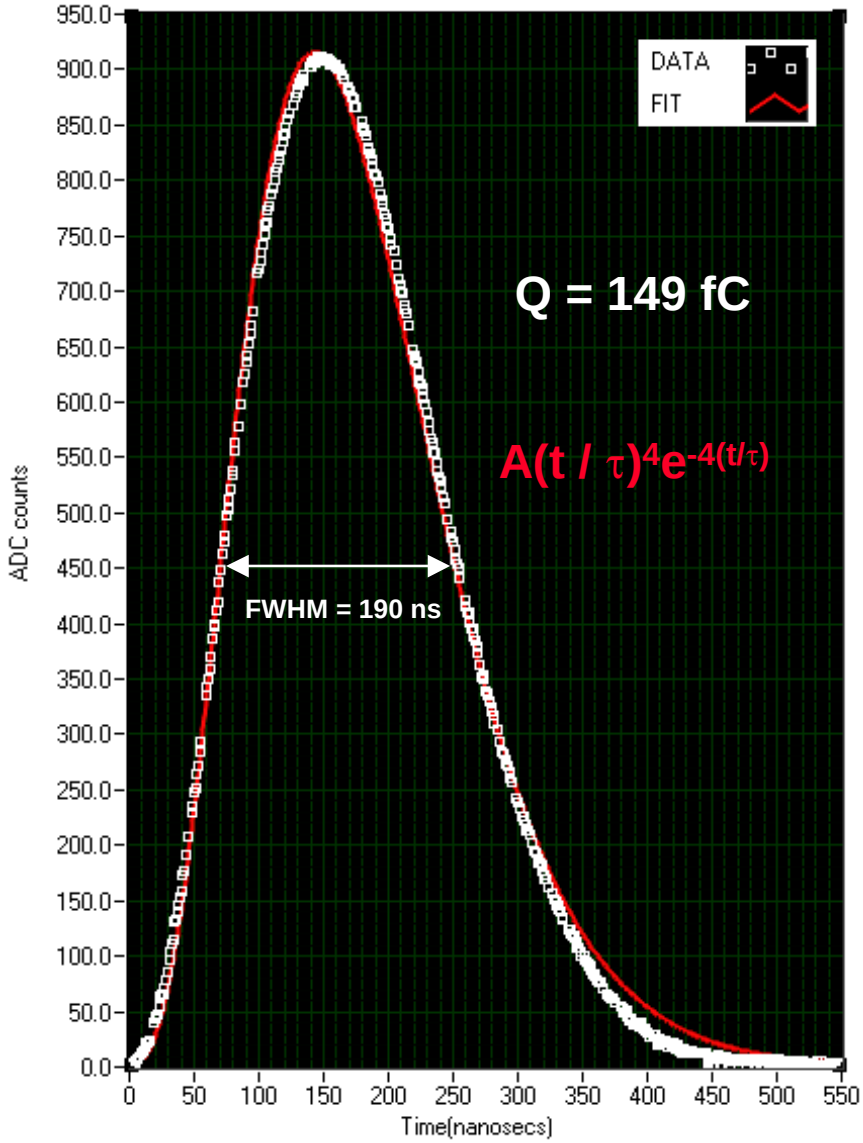


0.35μm 16.7 mm²



Nr. CH: 16	Nr. CH: 9	Nr. CH: 16
POWER/CH: 47mW	POWER/CH: 7.25mW	POWER/CH: 12mW
NOISE (12pF): 722 e	NOISE (12pF): 670 e	NOISE (12pF): 400 e
1996	2000	2001
STAR TPC	ALICE TPC prototype	ALICE TPC final

PERFORMANCE OF PASA EMBEDDED IN FEC

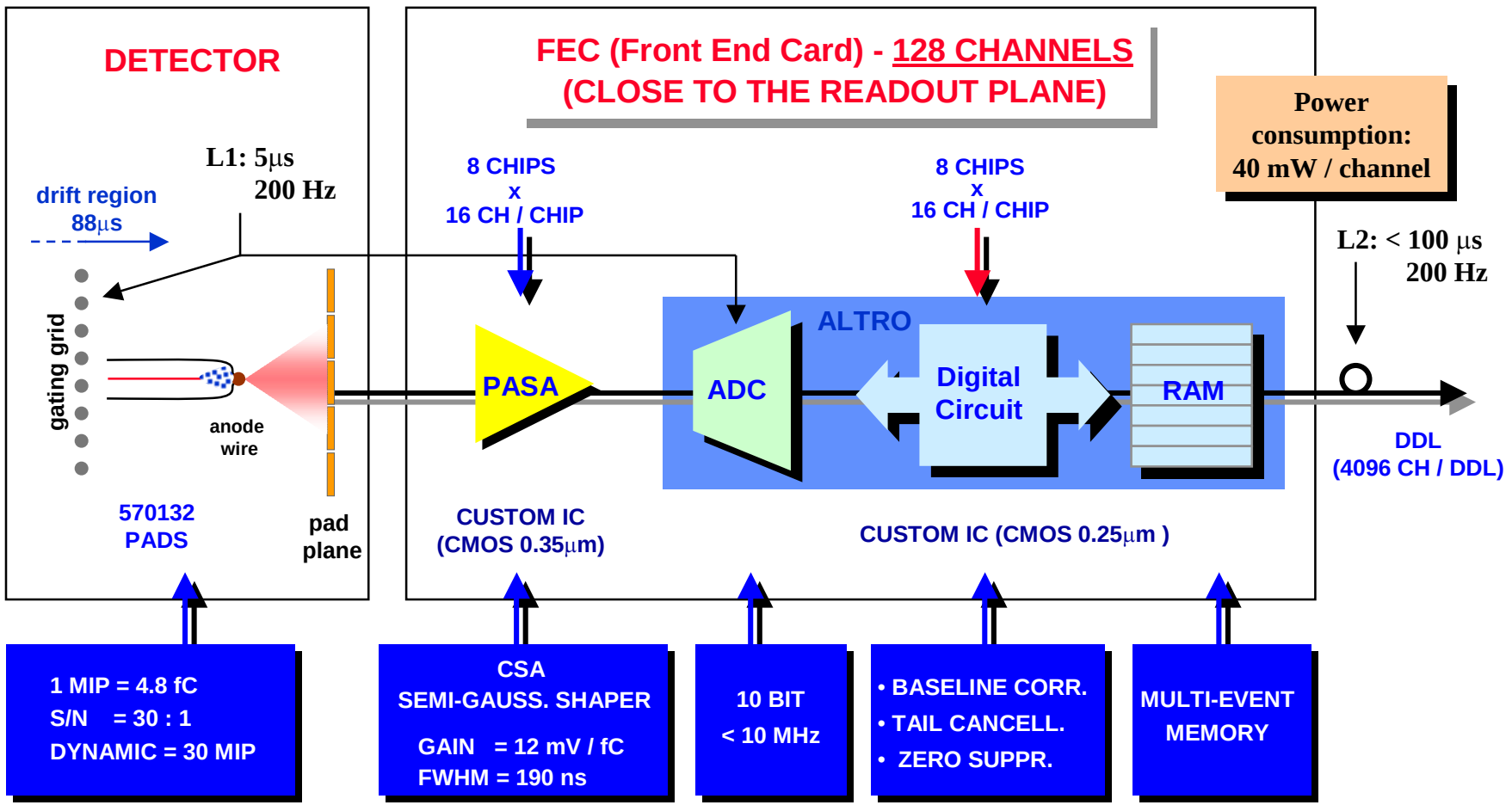


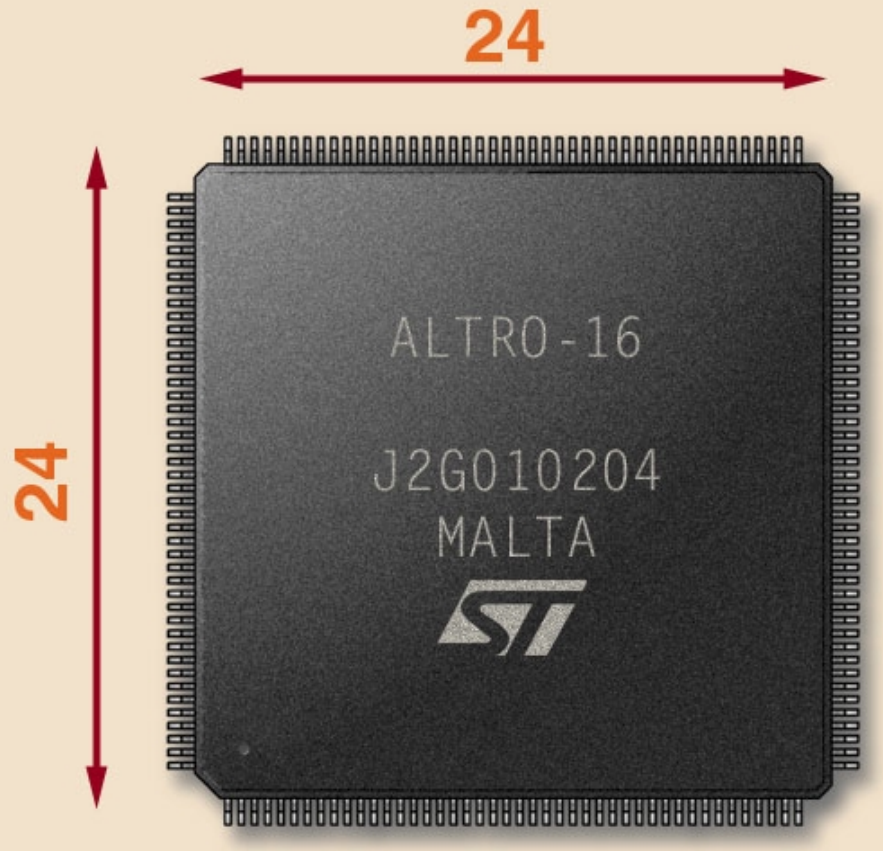
Parameter	Requirement	Measured (preliminary)
Noise	1000 e	(700 + 13/pF) e
Conversion gain	12mV / fC	11.8 mV / fC
Shaping time	190ns	190ns
Non linearity	<1%	< 0.35%
Crosstalk	<0.3%	<0.4%
Power consumption	< 20mW / ch	12mW / ch
Area		16.7mm^2

MILESTONES

- ✦ **January '02:** delivery of 40 samples of final PASA
- ✦ **Feb - Apr '02:** test of PASA in stand-alone mode
- ✦ **May '02:** integration of PASA in the FEC
- ✦ **June '02:** test of PASA connected to the IROC
- ✦ **July '02:** delivery of additional 200 samples
- ✦ **July '02:** engineering run
- ✦ **October '02:** full production

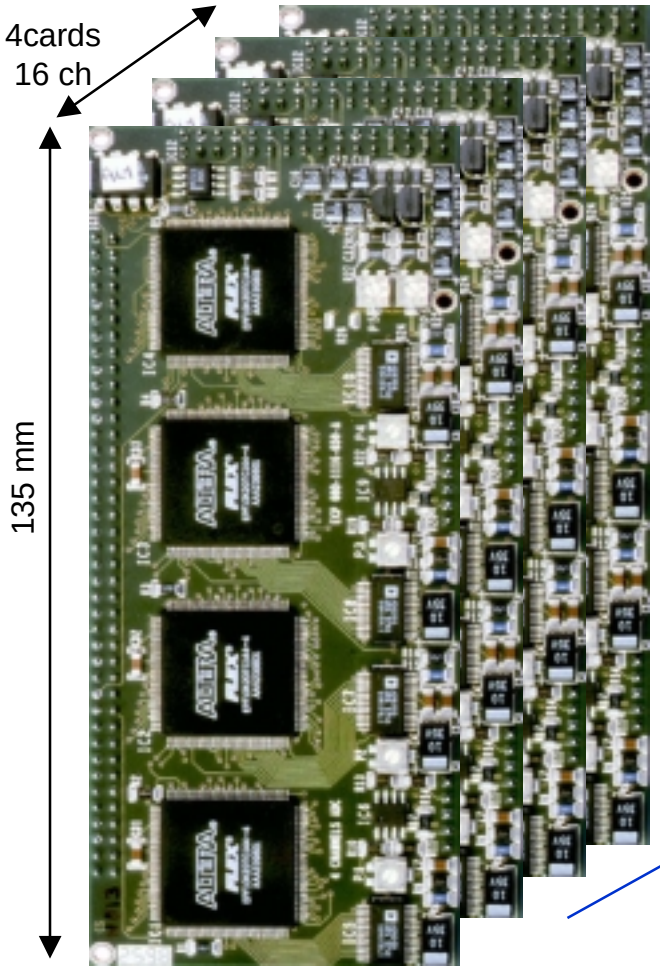
FEE ARCHITECTURE



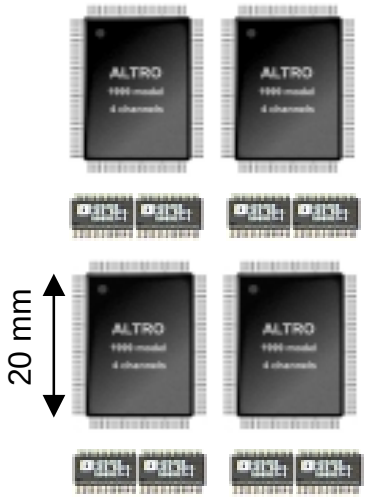


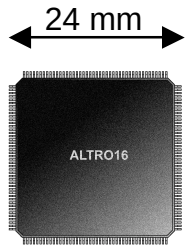
16 channels in 2002

TPC FEE – ALTRO: SUMMARY OF THE PROTOTYPING ACTIVITIES



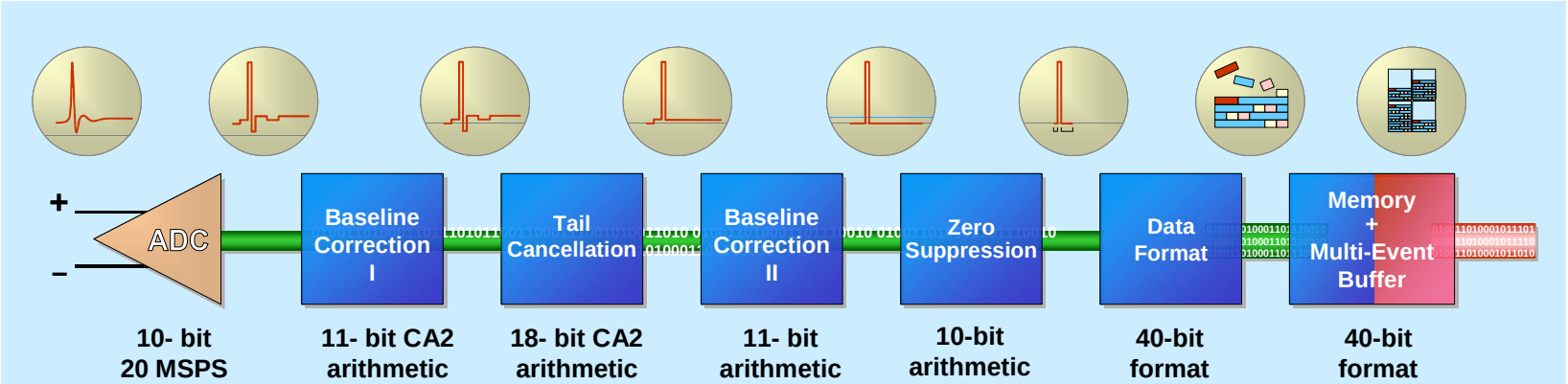
4 PQFP 100
8 SSOP 28





Integrated ADCs

1998	1999	2001
CHANNELS / CHIP: 1	CHANNELS / CHIP: 4	CHANNELS / CHIP: 1
POWER / CH: 120mW	POWER / CH: 80mW	POWER / CH: 16mW
PRICE / CH: 50CHF	PRICE / CH: 8CHF	PRICE / CH: 5CHF

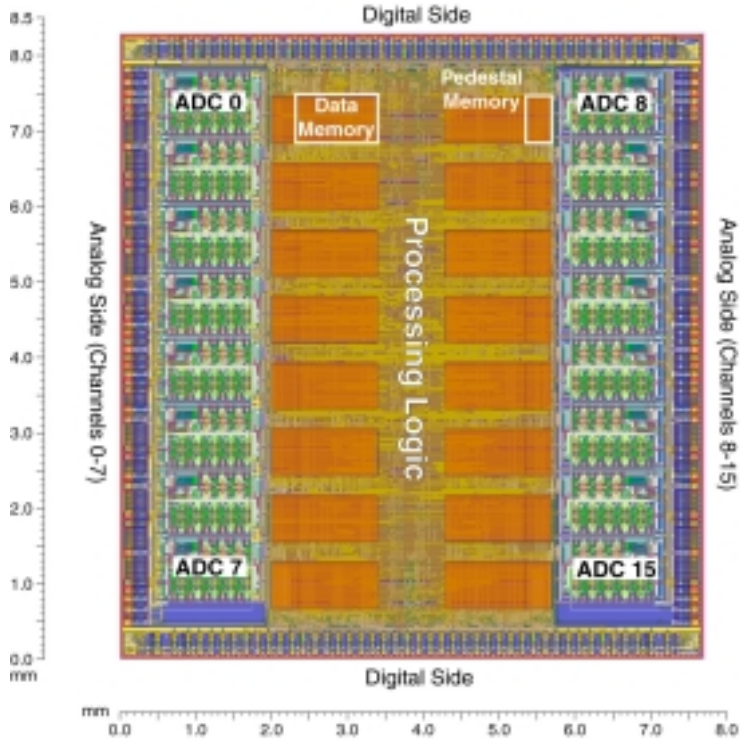


MAX SAMPLING CLOCK 40 MHz

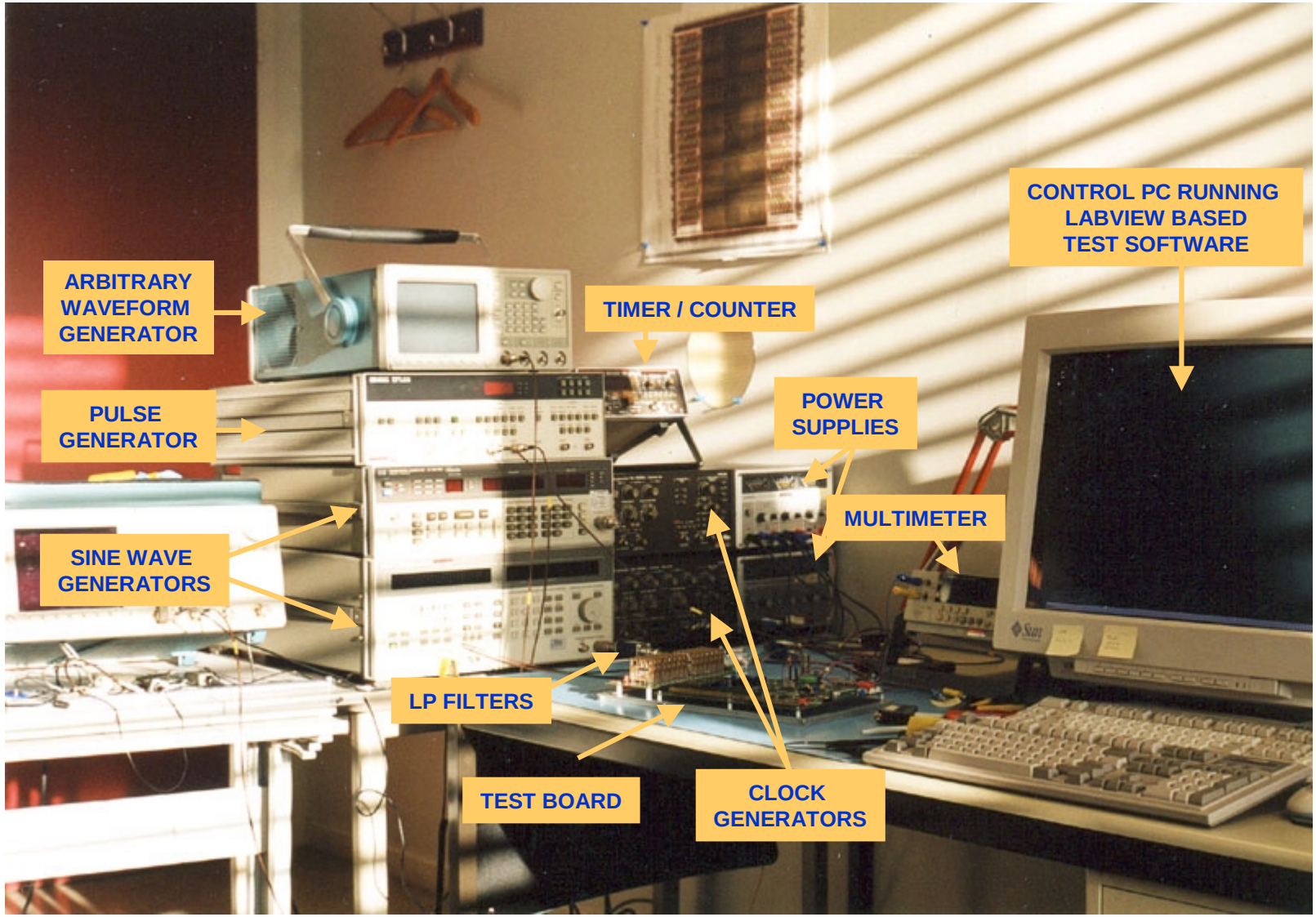
MAX READOUT CLOCK 60 MHz

16-ch signal digitizer and processor

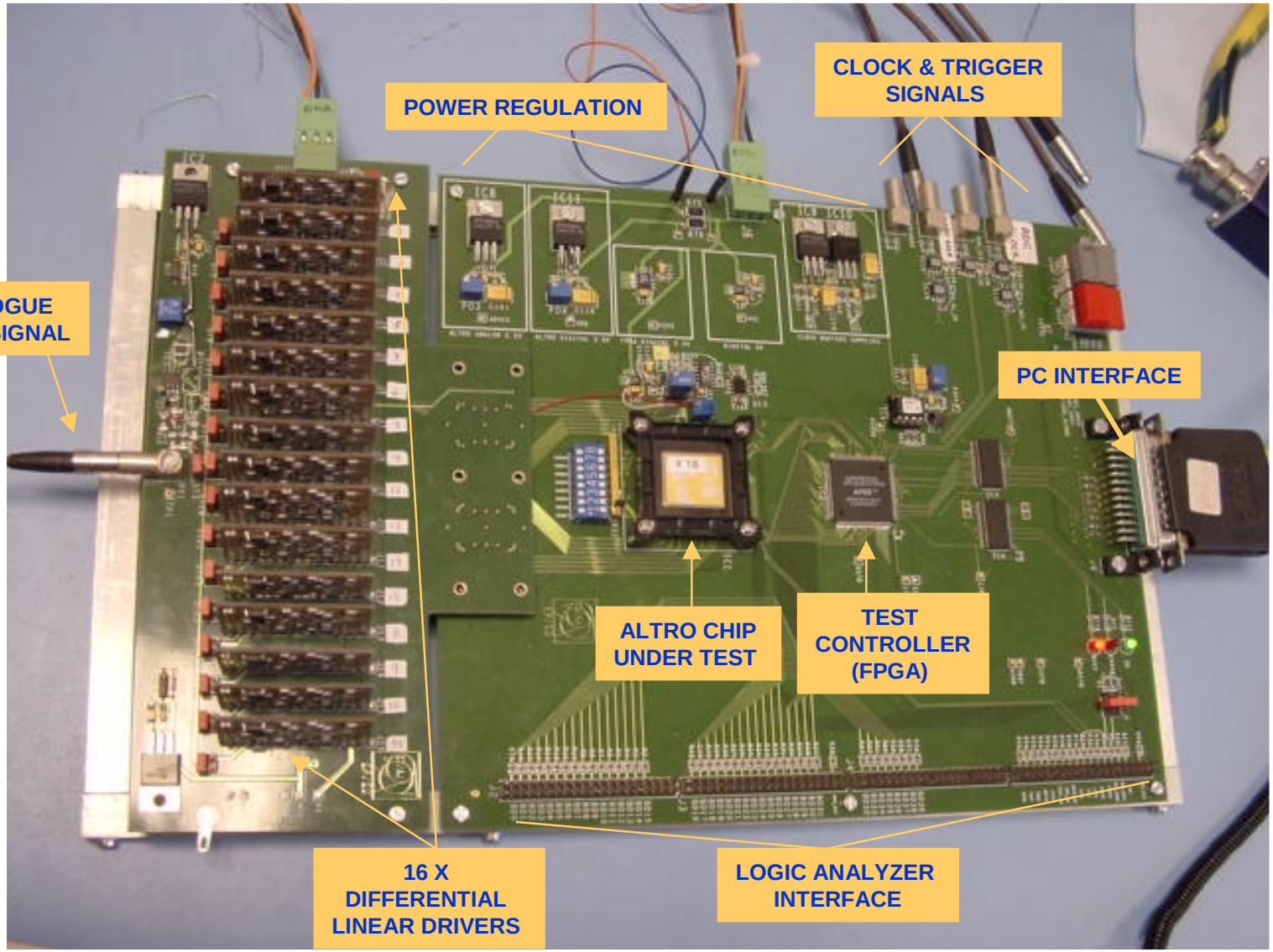
- HCMOS7 0.25 μm (ST)
- area: 64 mm^2
- power: 16 mW / ch
- prototype delivery: Feb ‘02
- 300 samples fully tested
- delivery of 4x10^4 chips: Dec ‘02



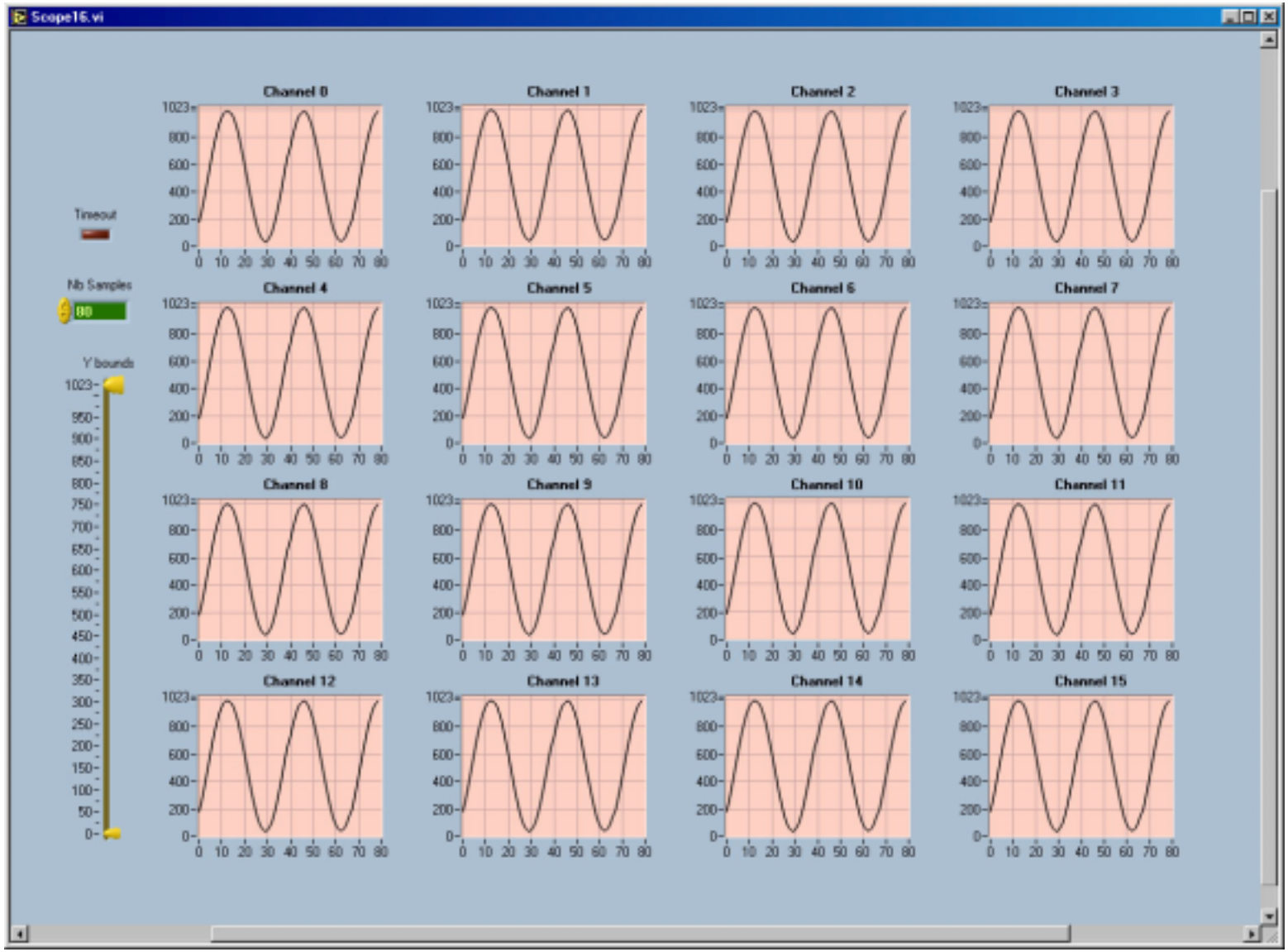
ALTRO TEST SETUP



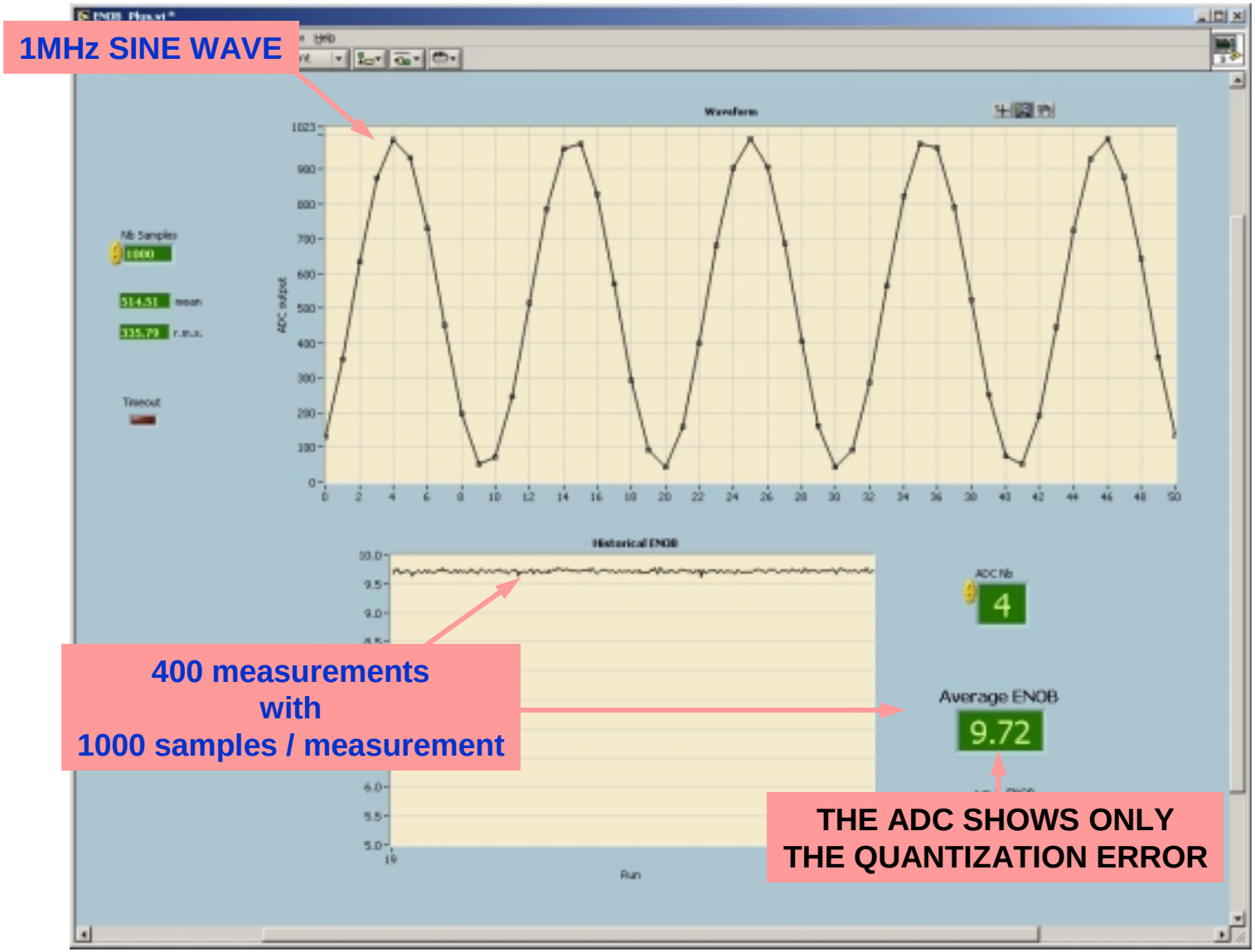
ALTRO TEST BOARD



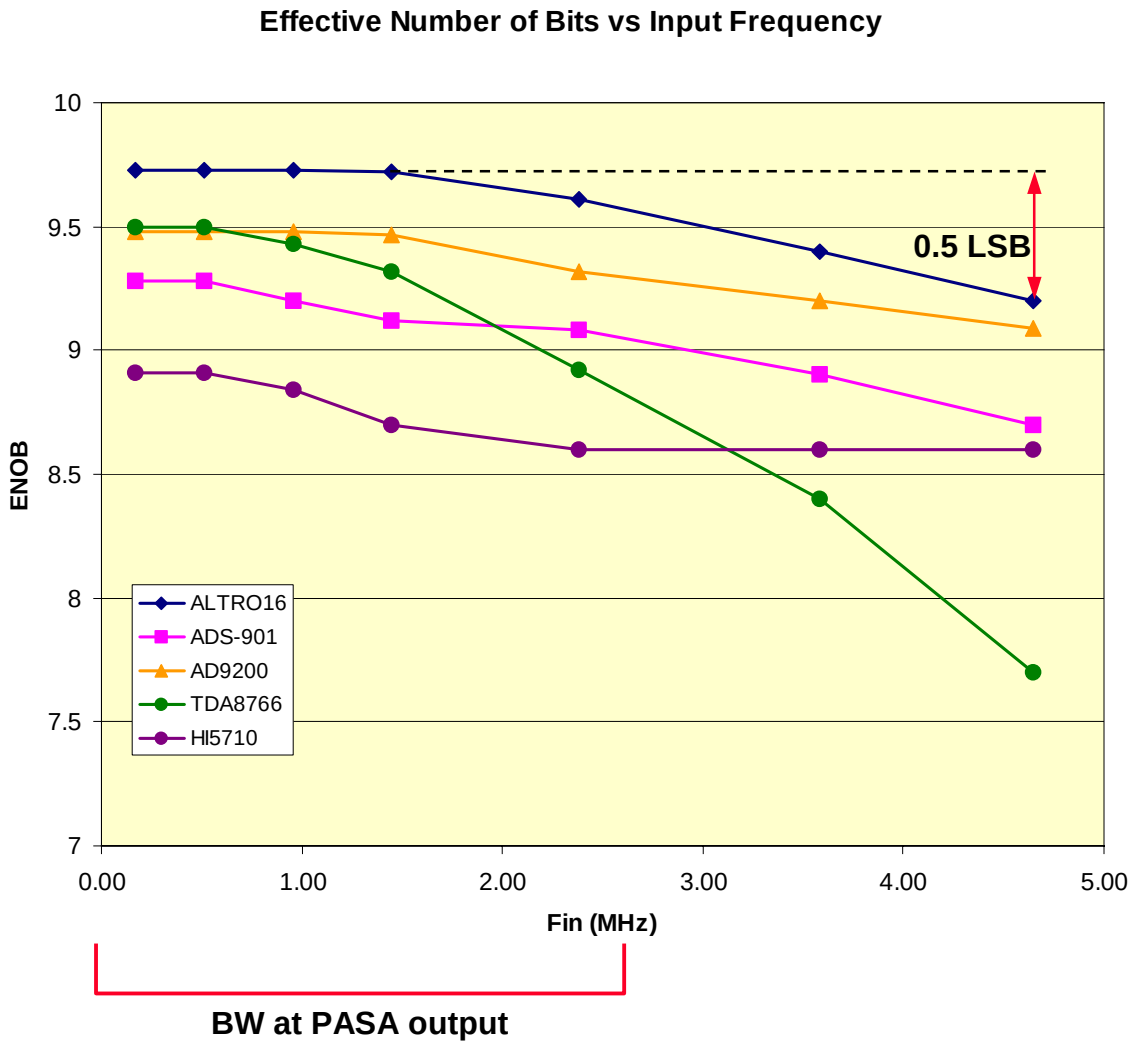
16 CHANNELS IN ONE SHOT



EFFECTIVE NUMBER OF BITS (ENOB)



ENOB vs Frequency



Quartz Jitter:

25ps r.m.s.

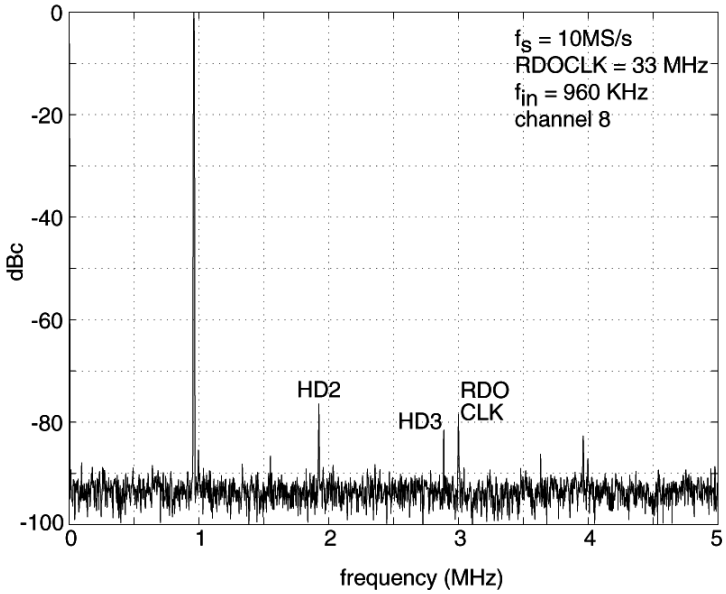
Amplitude Uncertainty:

$$4 \cdot f_{in} \cdot \text{jitter} \cdot 2^{10}$$

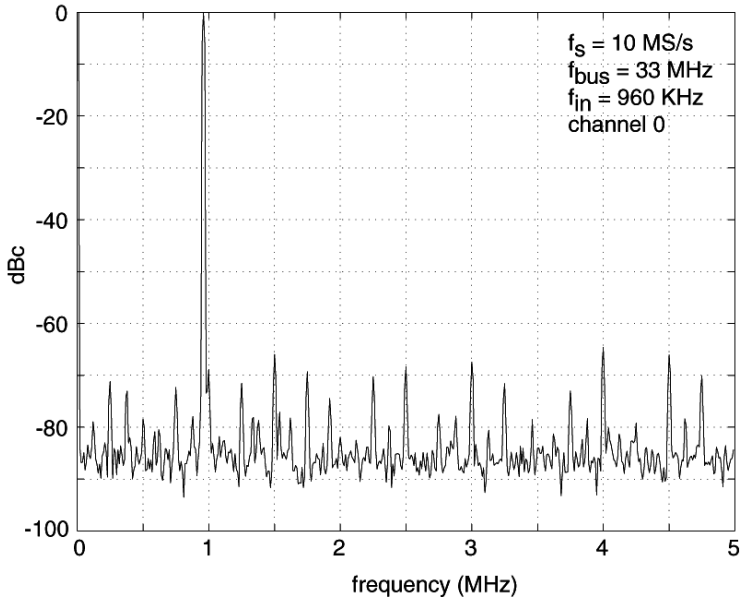
0.5 bits at 4.8 MHz

Crosstalk and Digital Noise

DIGITAL NOISE



Readout Clock below -78 dBc (WC)



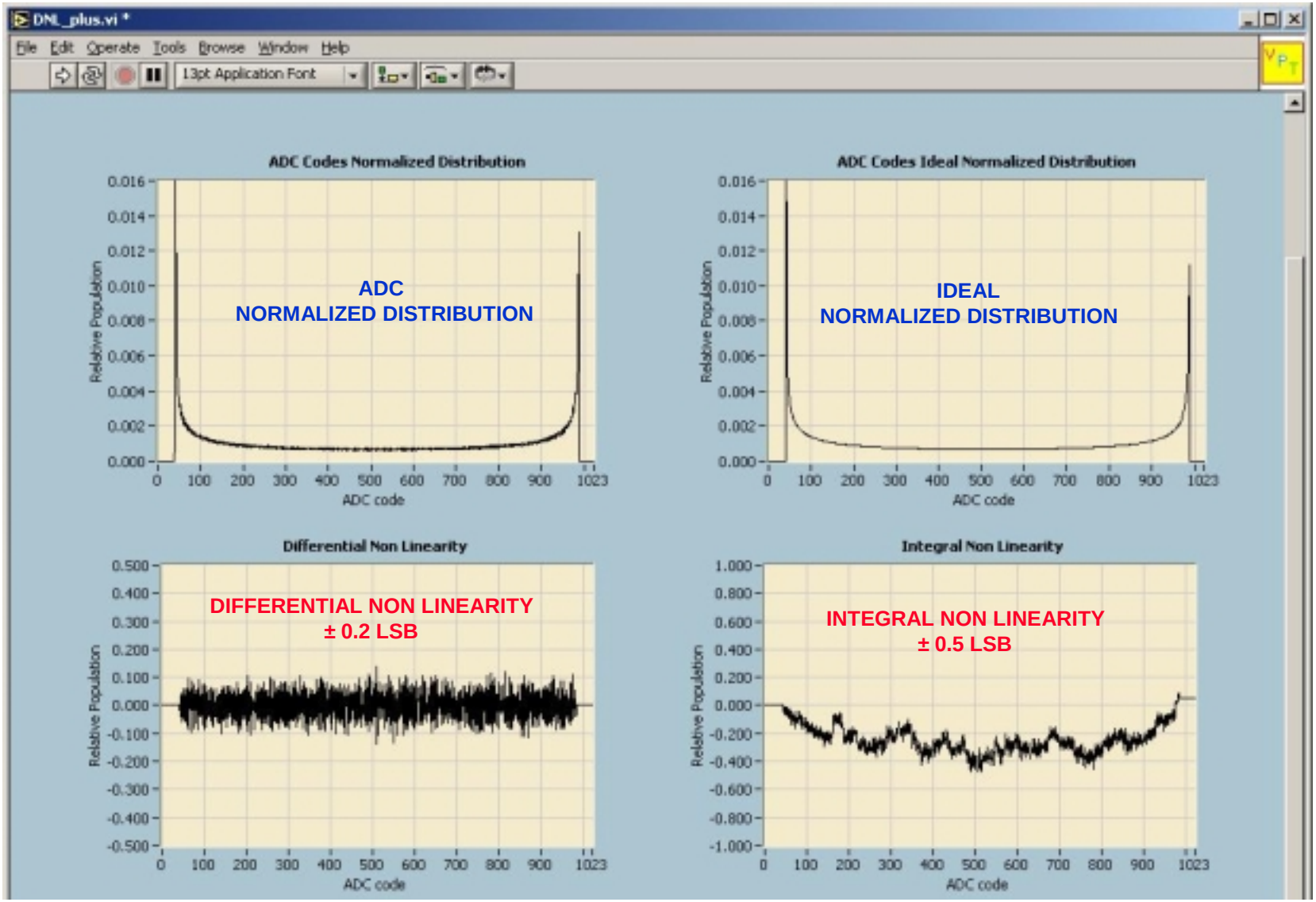
Bus interference below -65 dBc (WC)

CHANNEL-TO-CHANNEL CROSSTALK

F_{in} = 1 MHz 0.05 LSB rms (-80 dBc)
F_{in} = 5 MHz 0.2 LSB rms (-68 dBc)

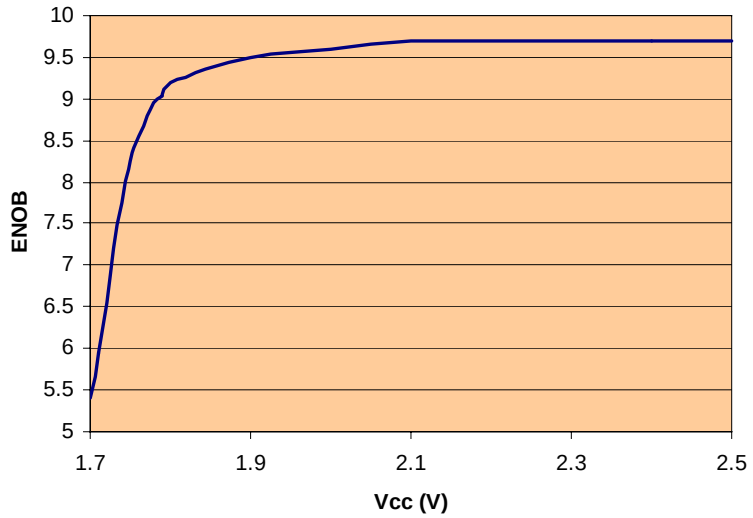
Dynamic Range of a 10-bit ADC: 60 dB

Differential and Integral Non-Linearity

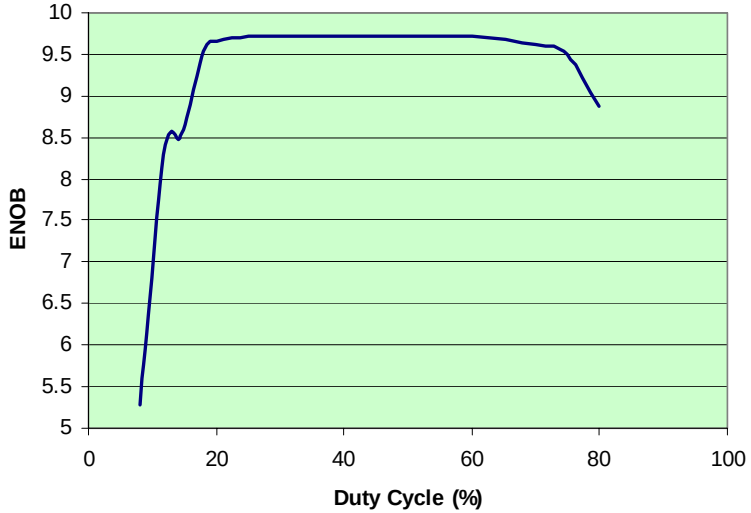


Chip performance

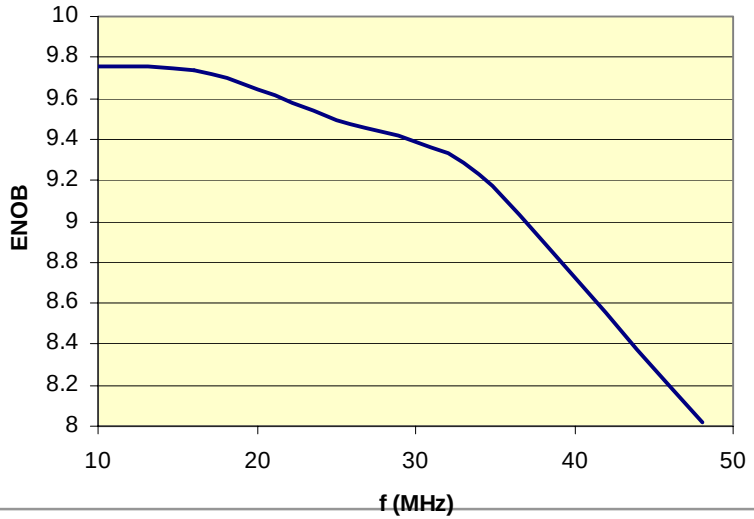
ENOB vs Analog Vcc



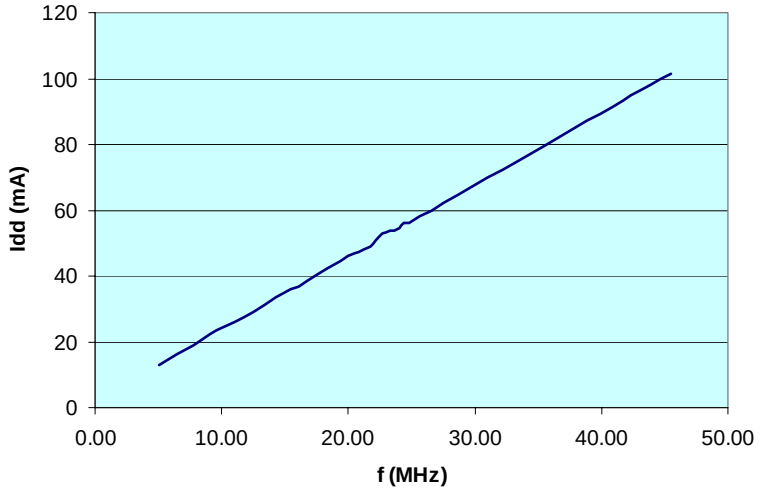
ENOB vs Duty Cycle



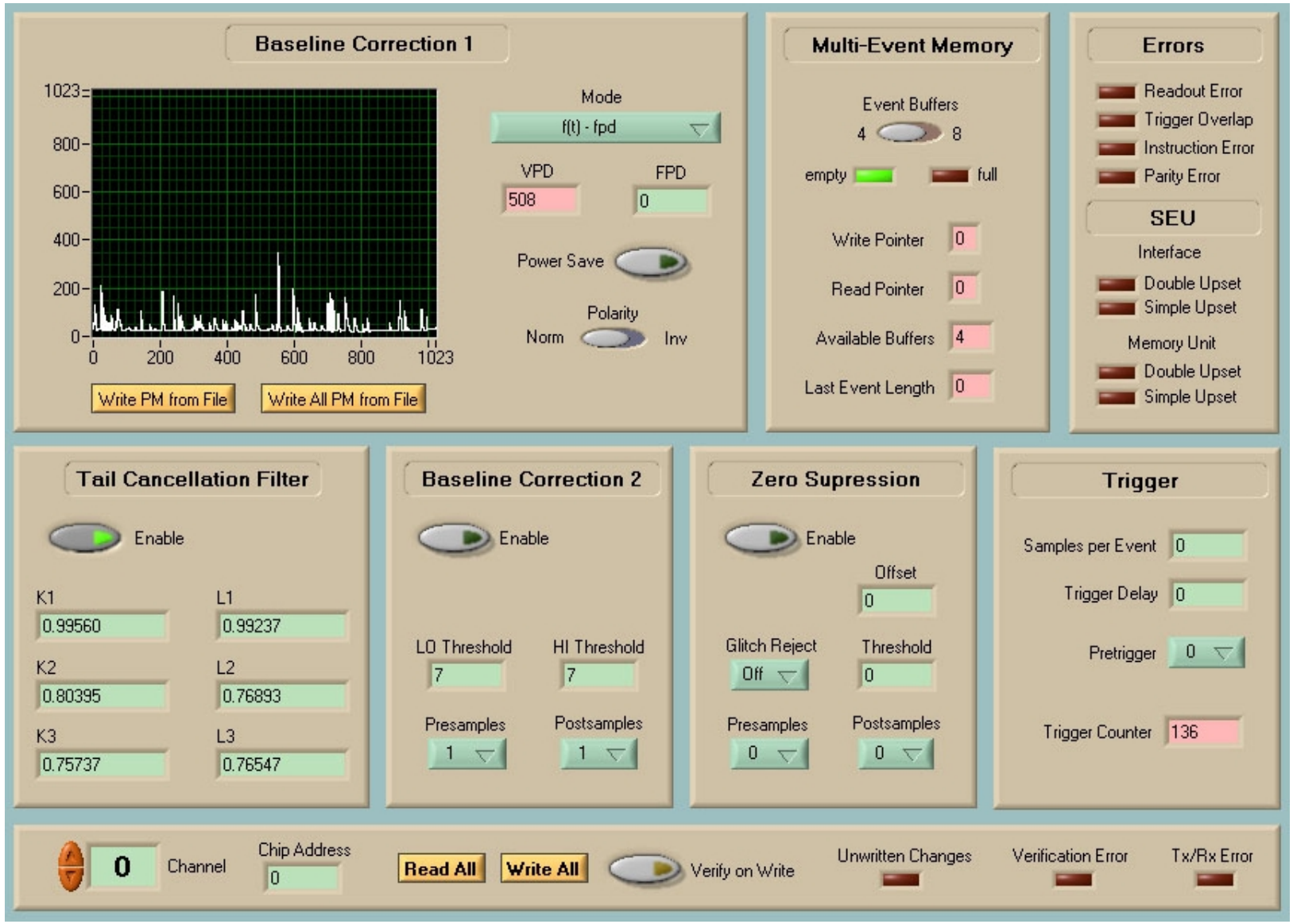
ENOB vs Sampling Frequency



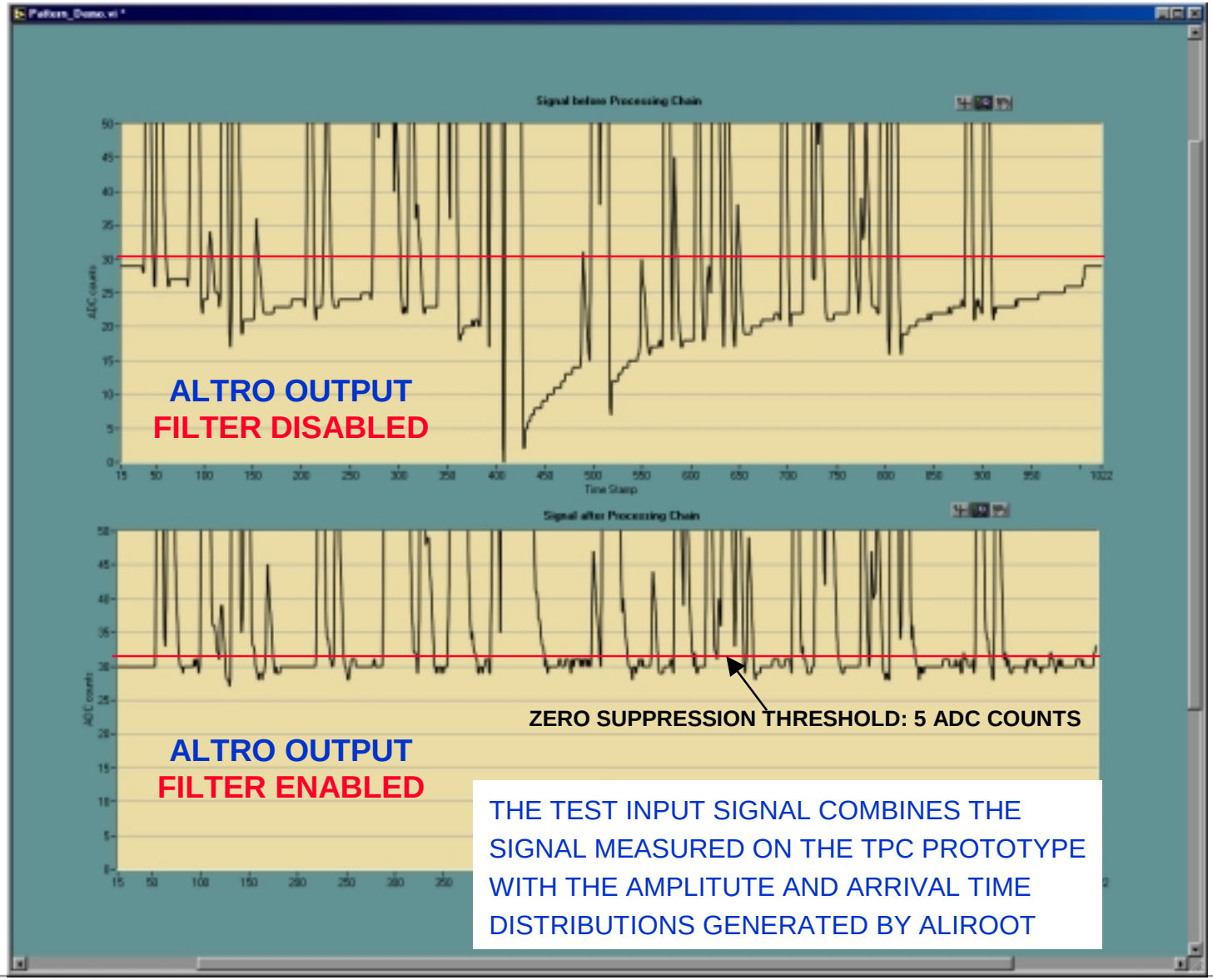
Digital Power Consumption vs Sampling Frequency



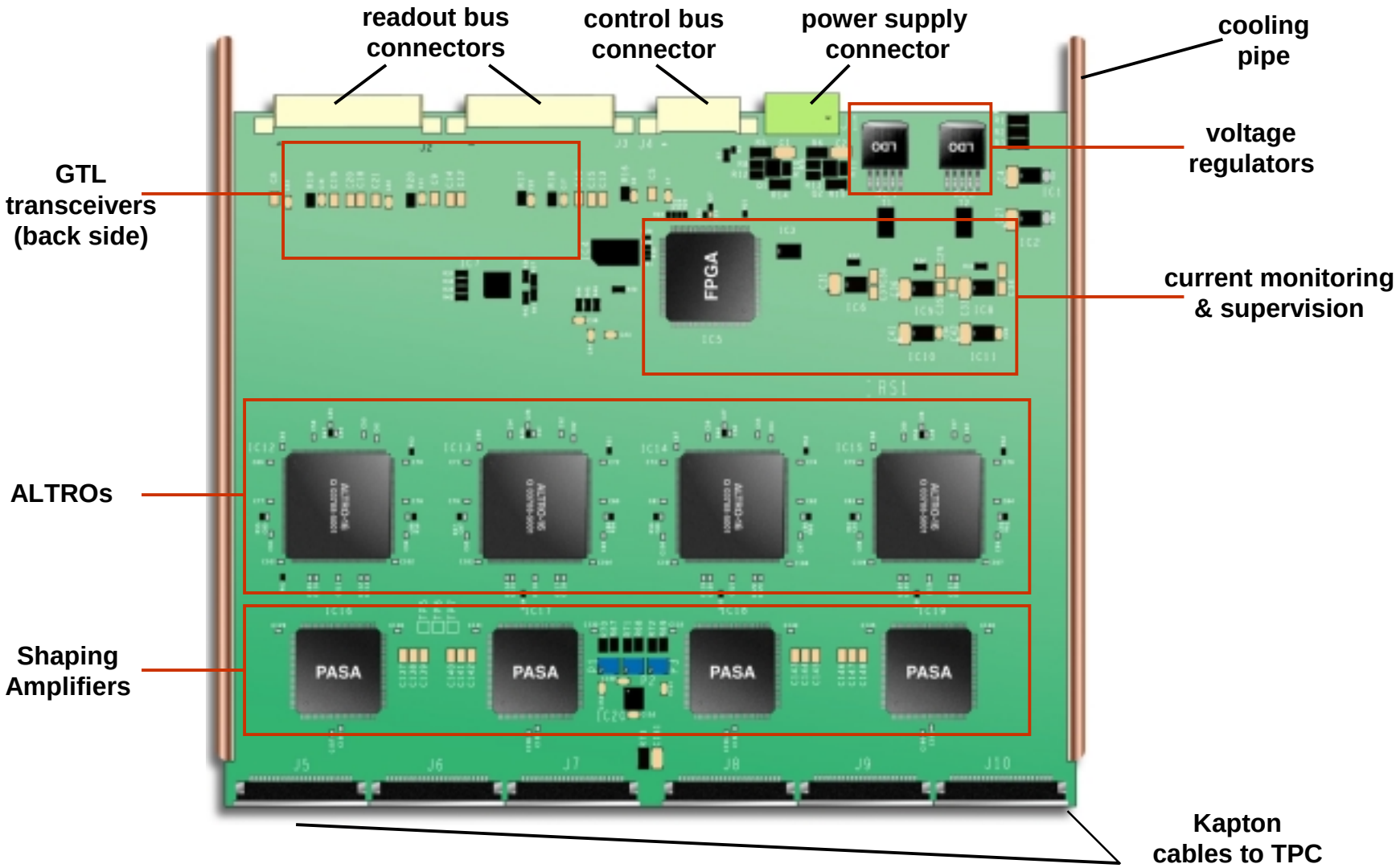
FUNCTIONAL VALIDATION: ALTRO CONTROL PANNEL



FUNCTIONAL VALIDATION

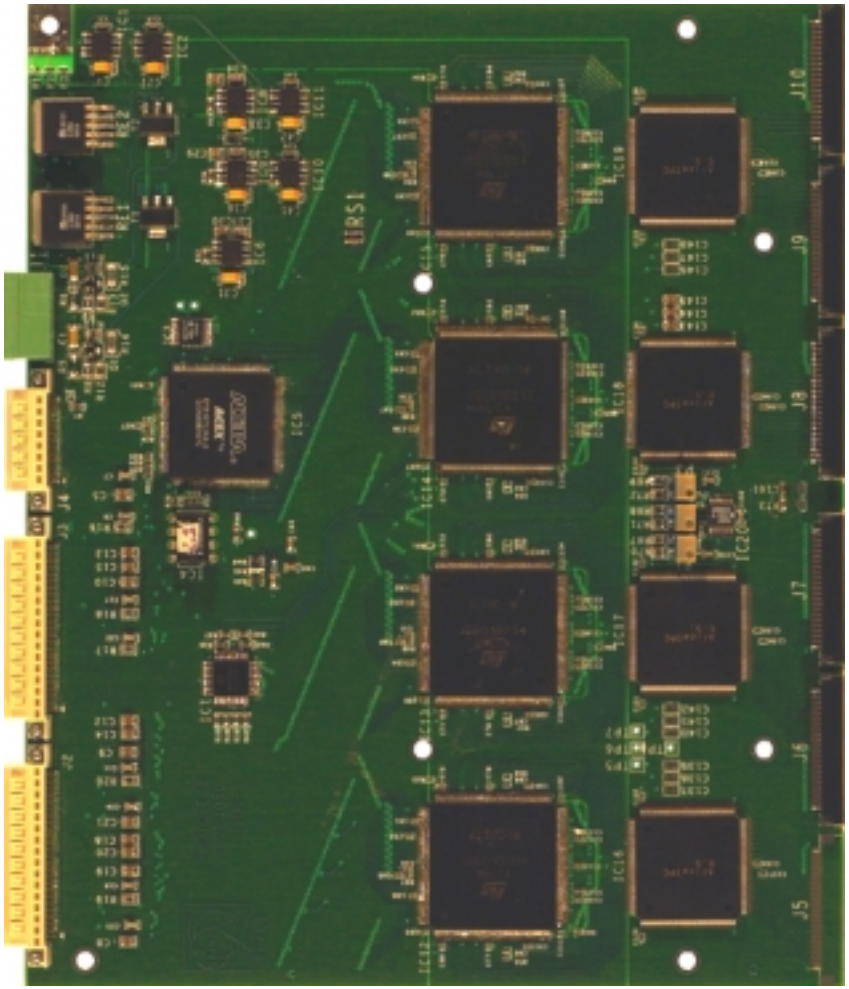


FRONT END CARD
(128 CHANNELS)

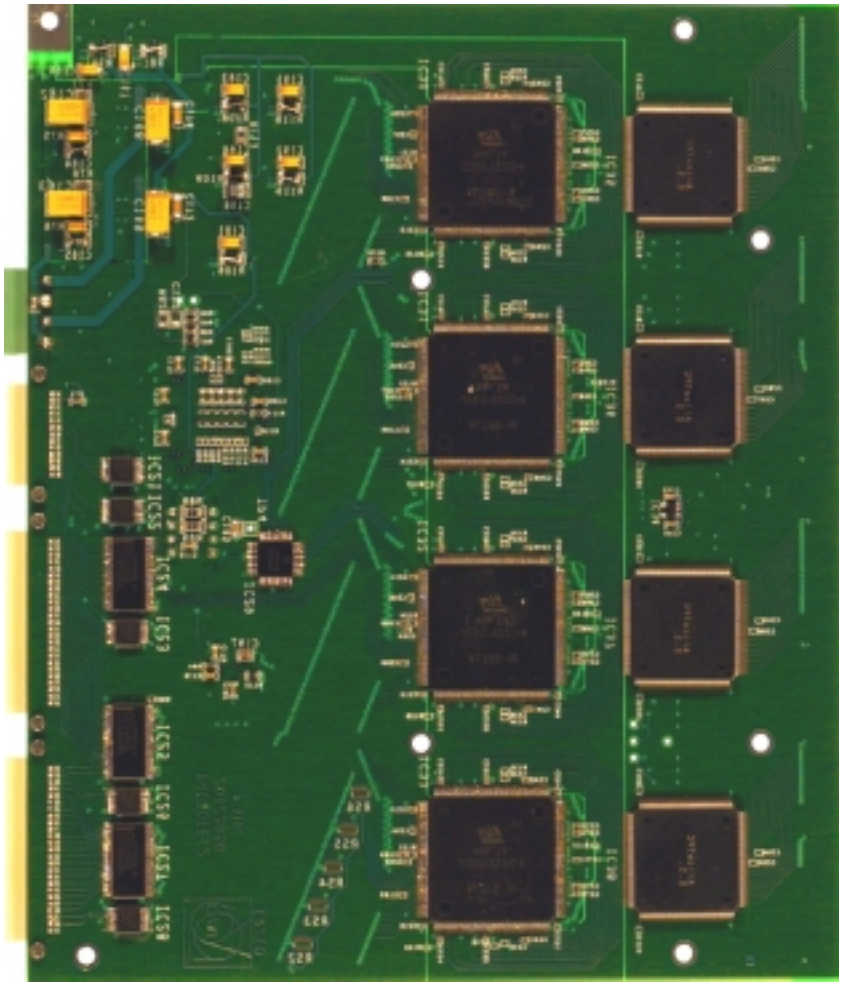


FRONT END CARD

TOP SIDE

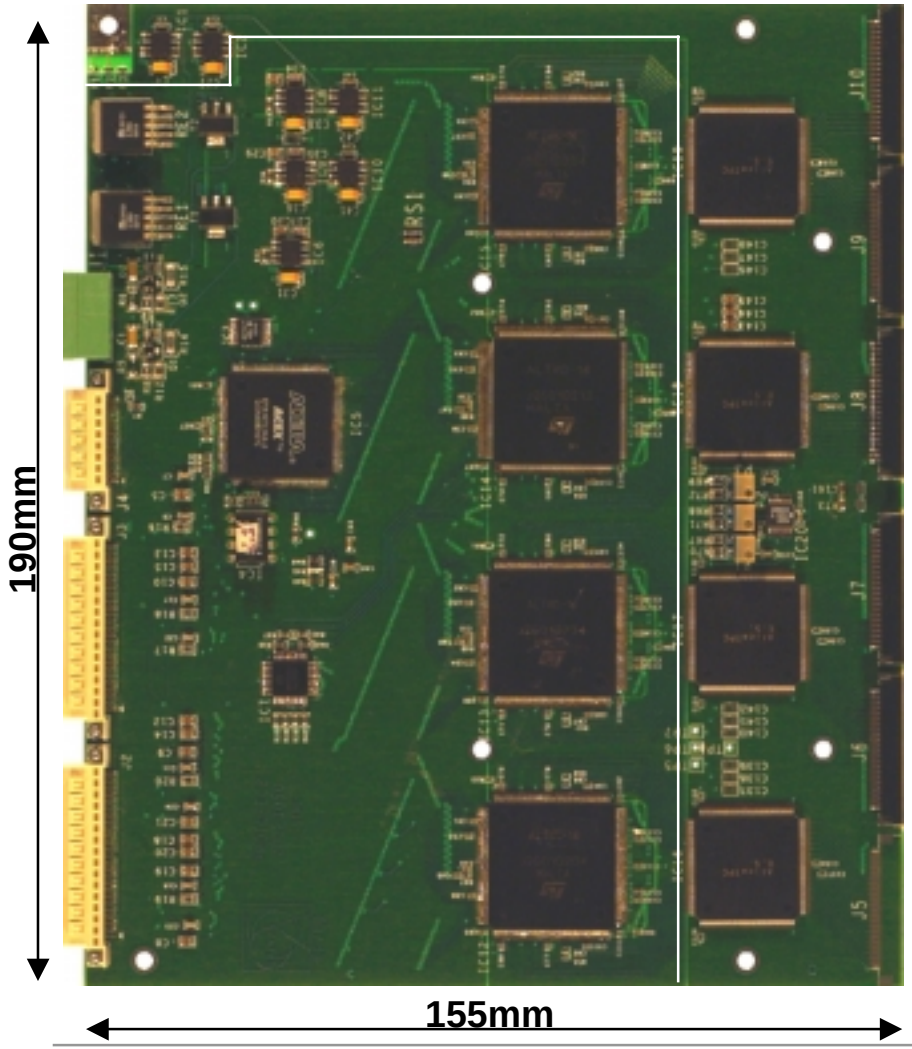


BOTTOM SIDE



FRONT END CARD

TOP SIDE



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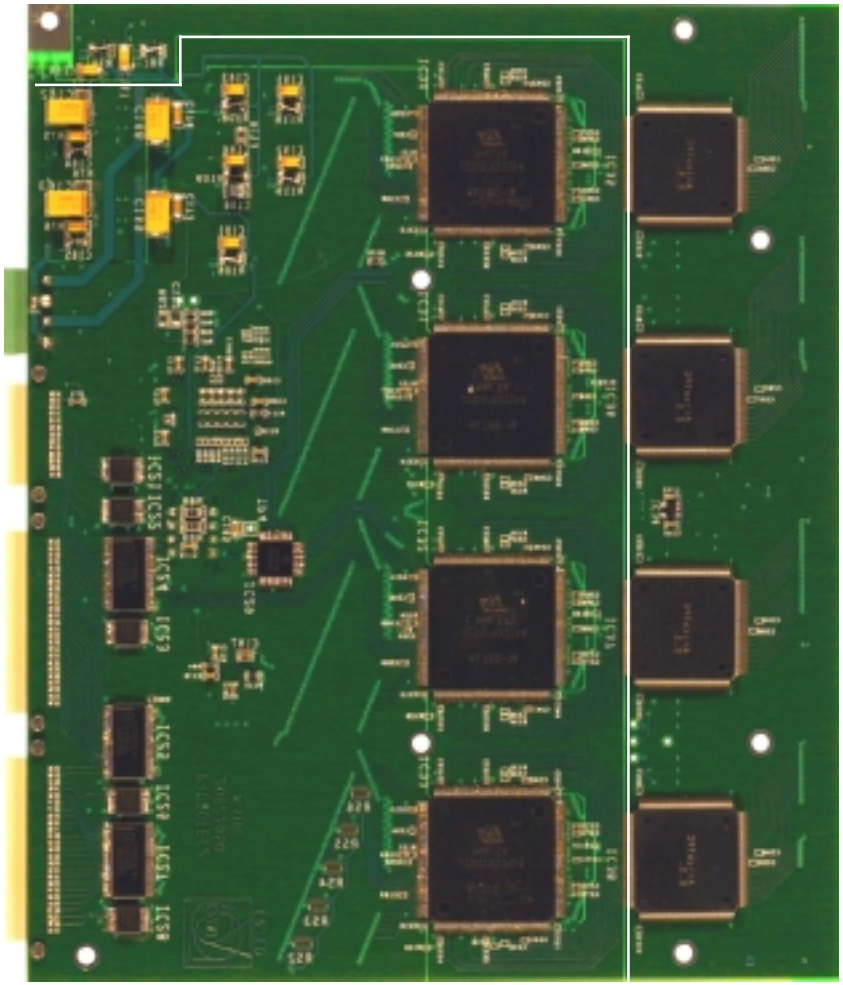
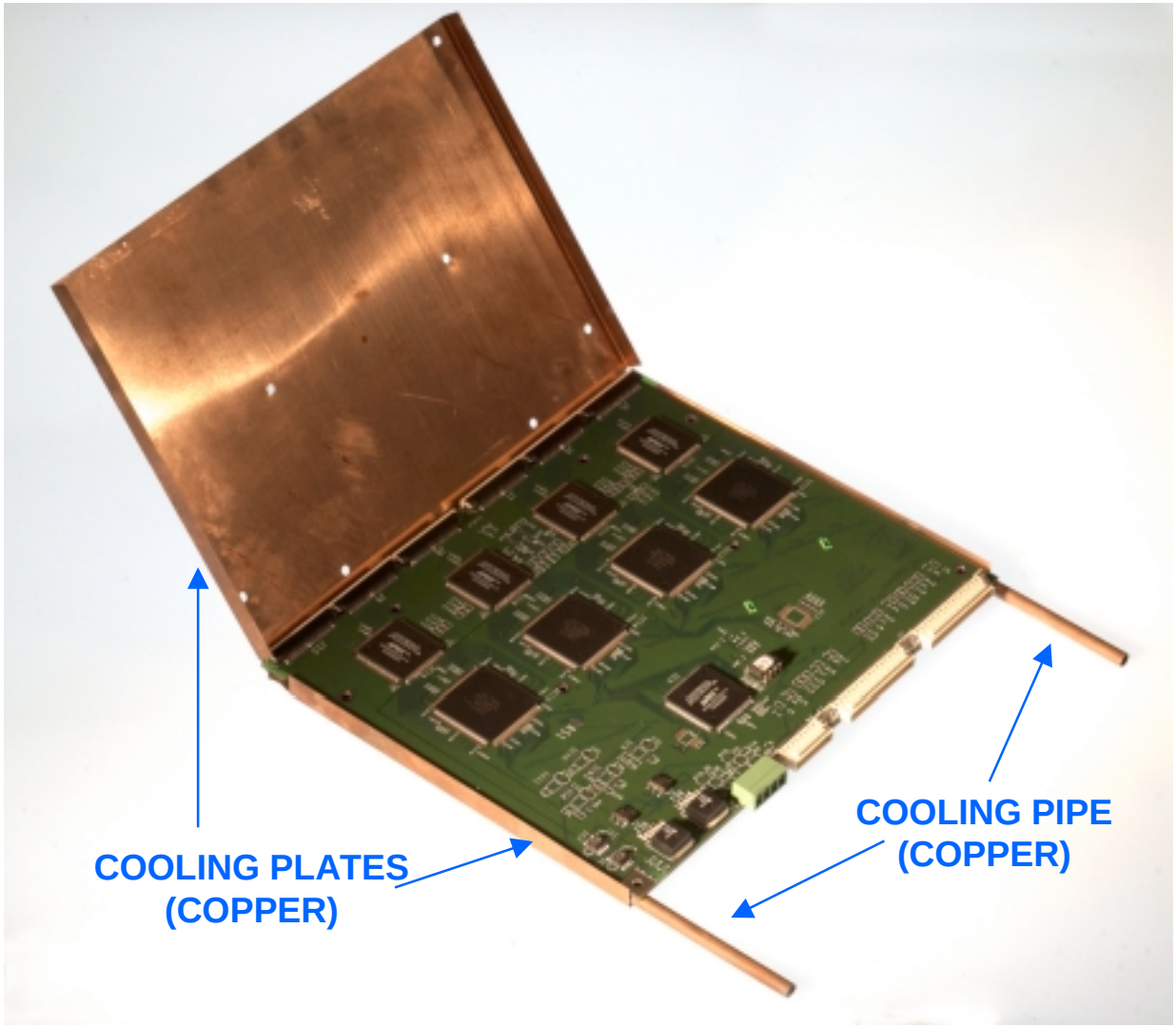
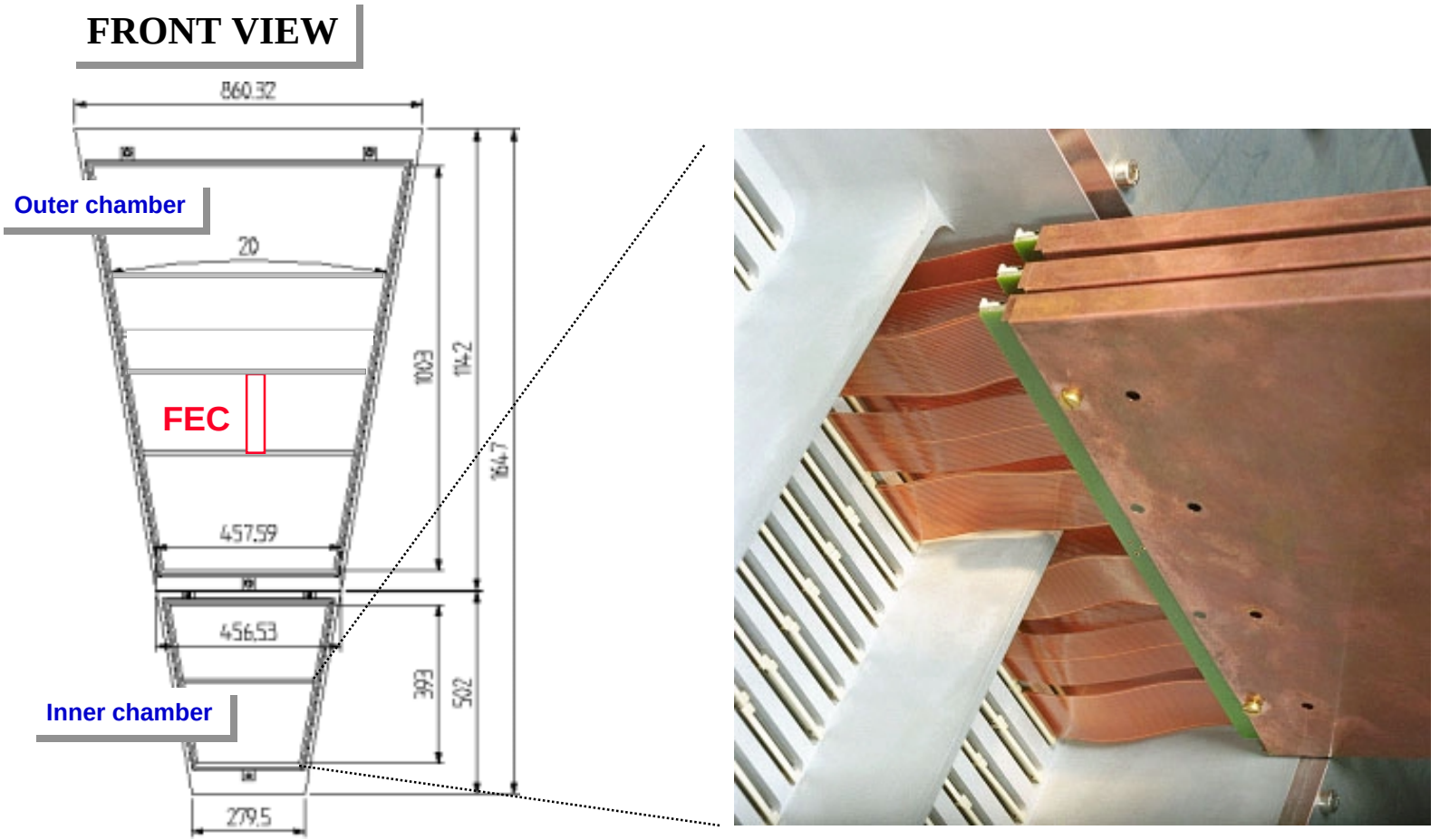


FRONT END CARD

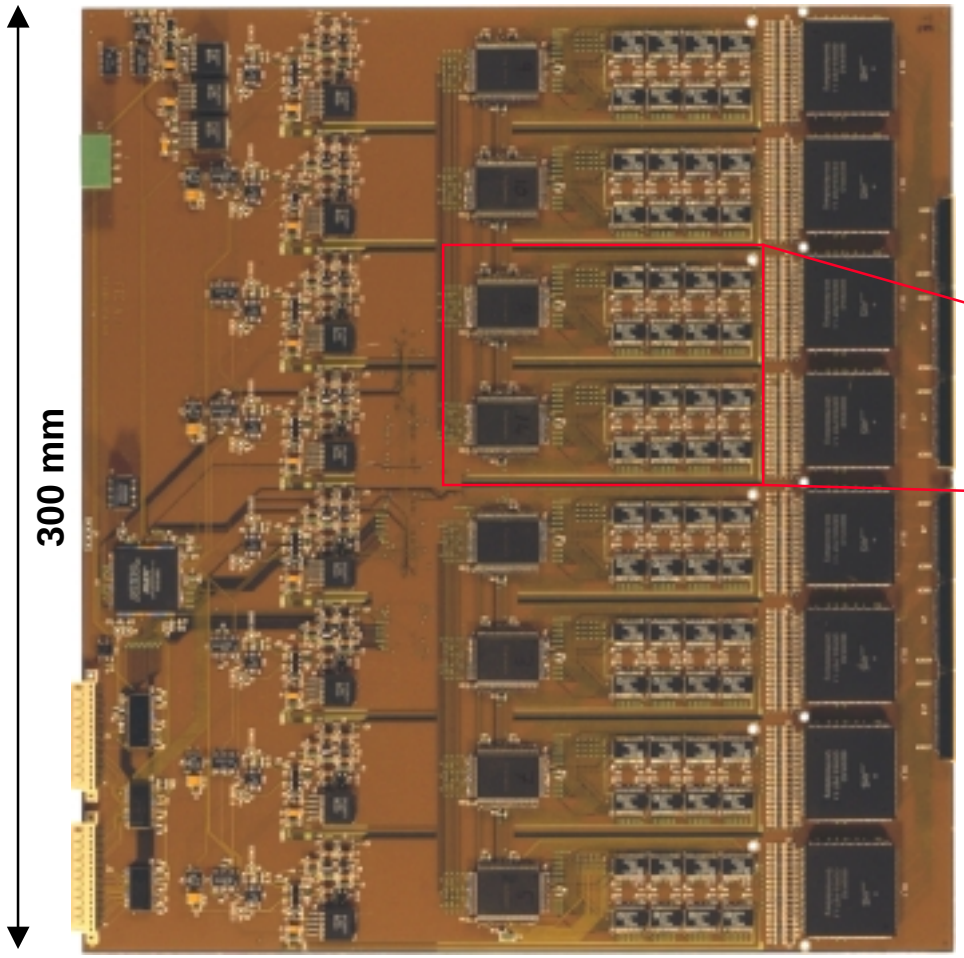


INTEGRATION IN THE READOUT CHAMBER



FRONT END CARD

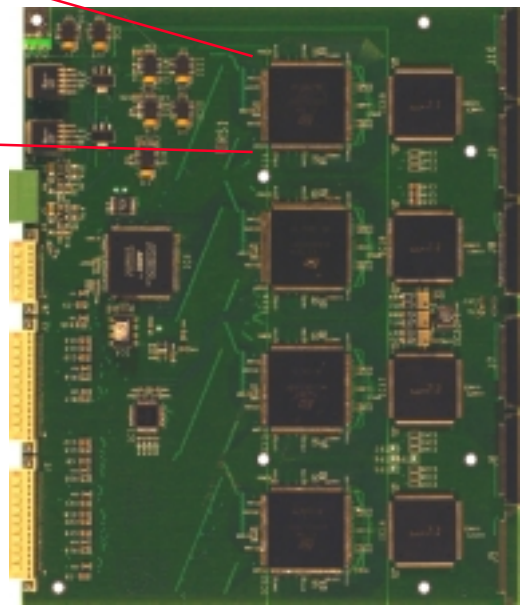
FIRST PROTOTYPE



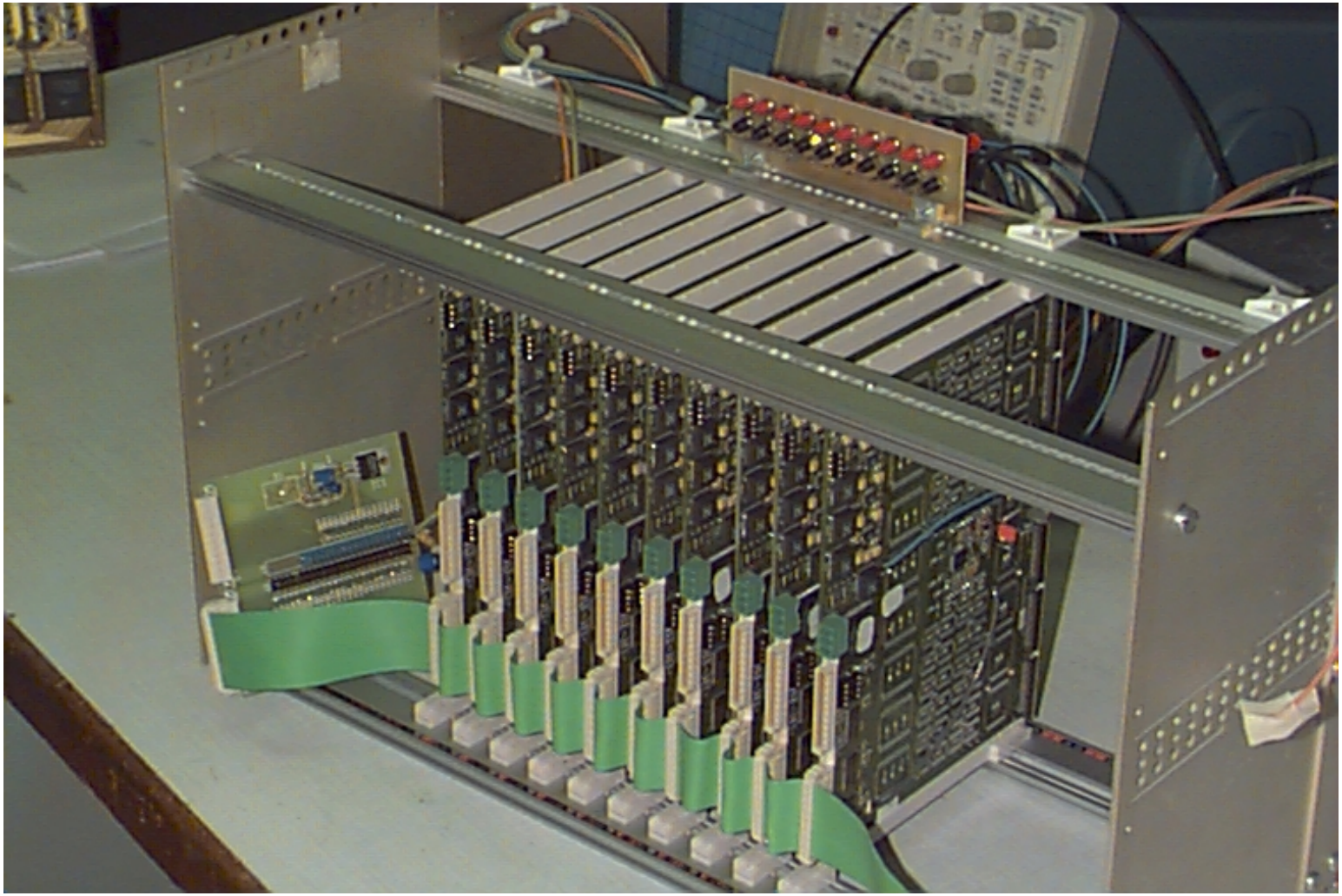
FINAL DESIGN

Pre-series production of 30 FEC (60% of one IROC) started.

Market survey for mass production will be concluded by end of June



FRONT END CARD



GLOBAL ARCHITECTURE

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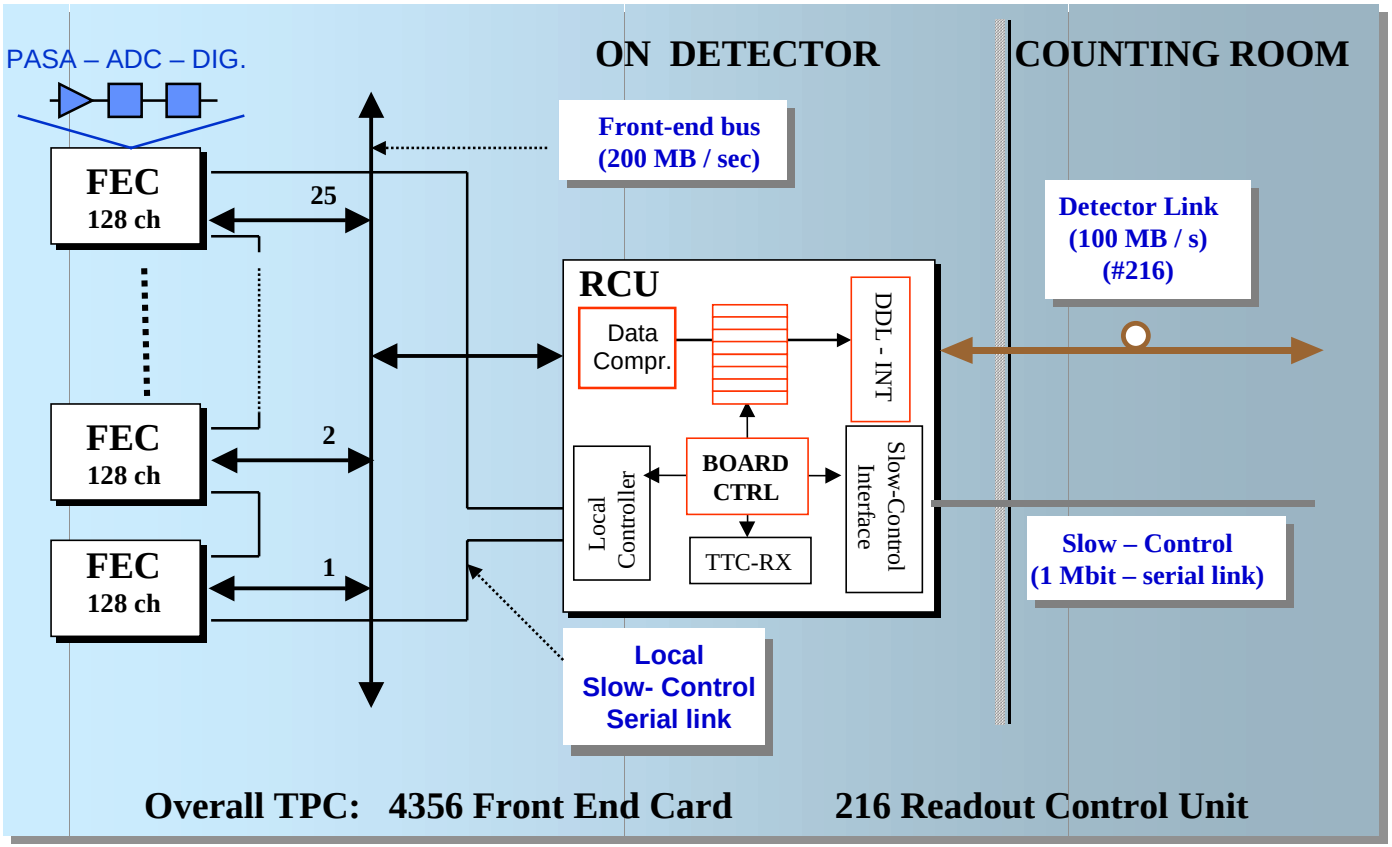
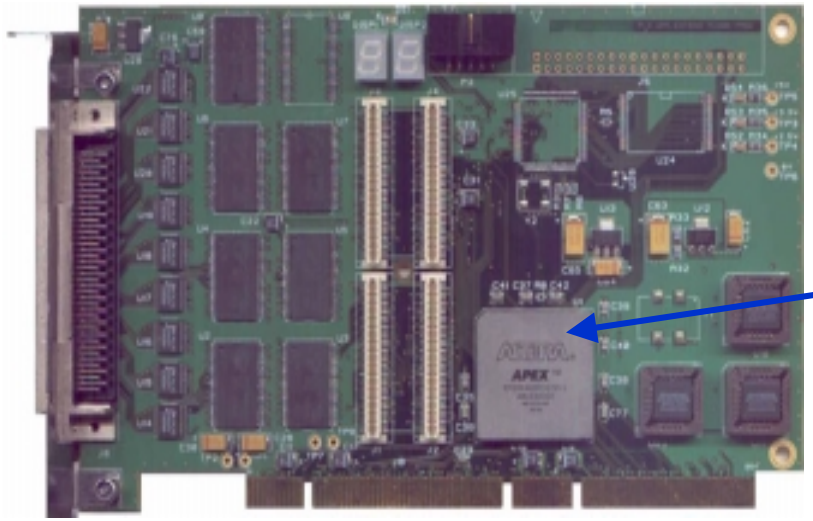


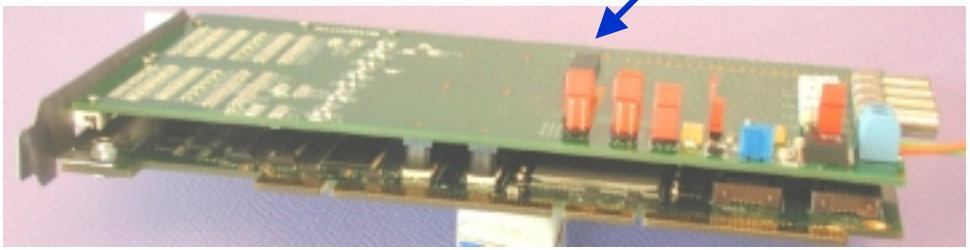
READOUT CONTROL UNIT
FIRST PROTOTYPE

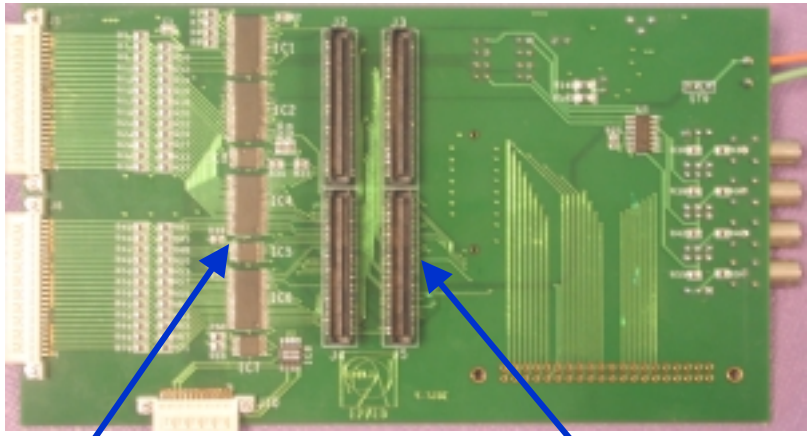


PCI CARD (PLDa)

FPGA with PCI-core

DDL-SIU CONNECTOR





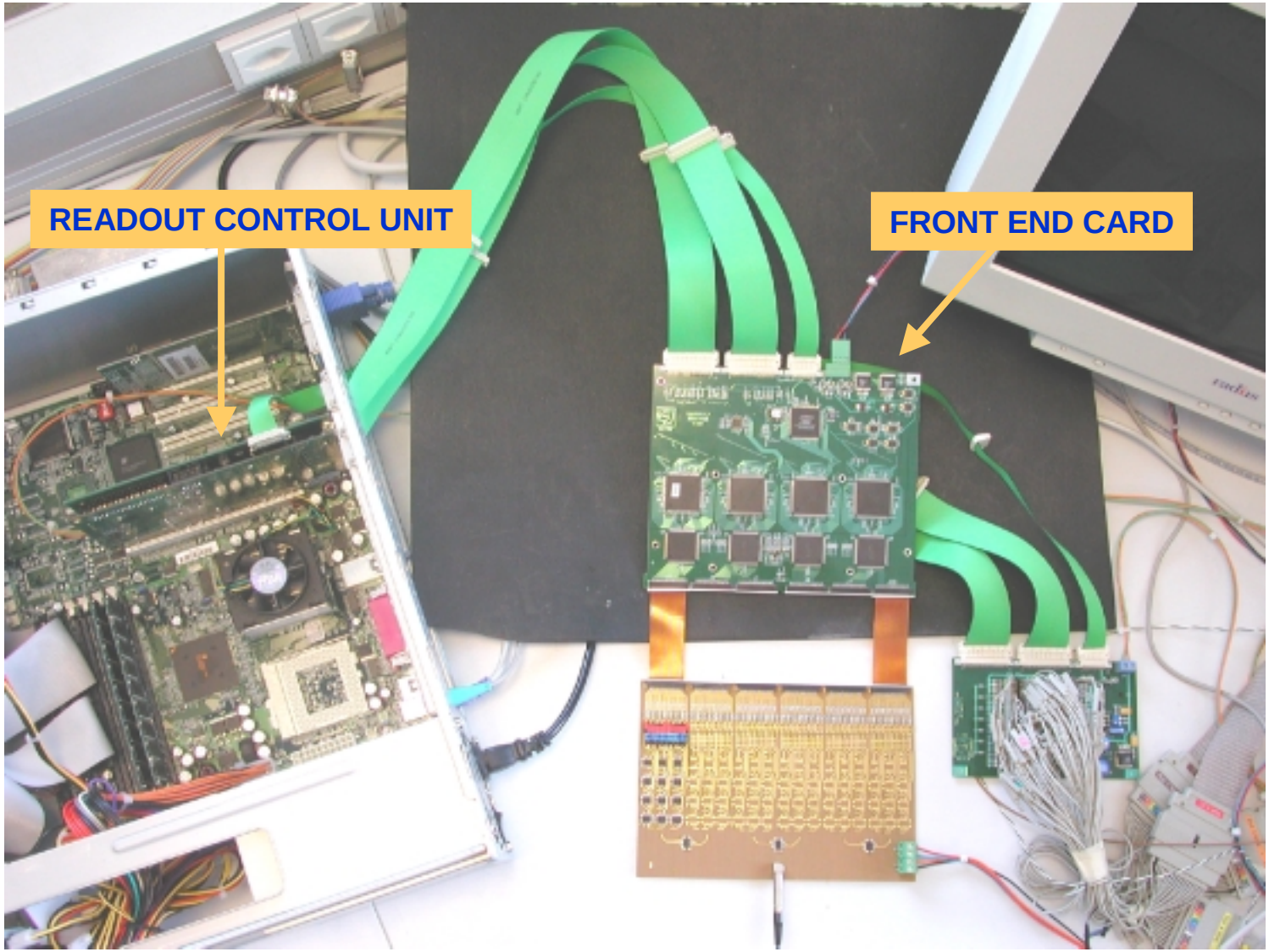
LEMO CONNECTOR
(L1, L2, RDOCLK, ADCCLK)

PMC CARD

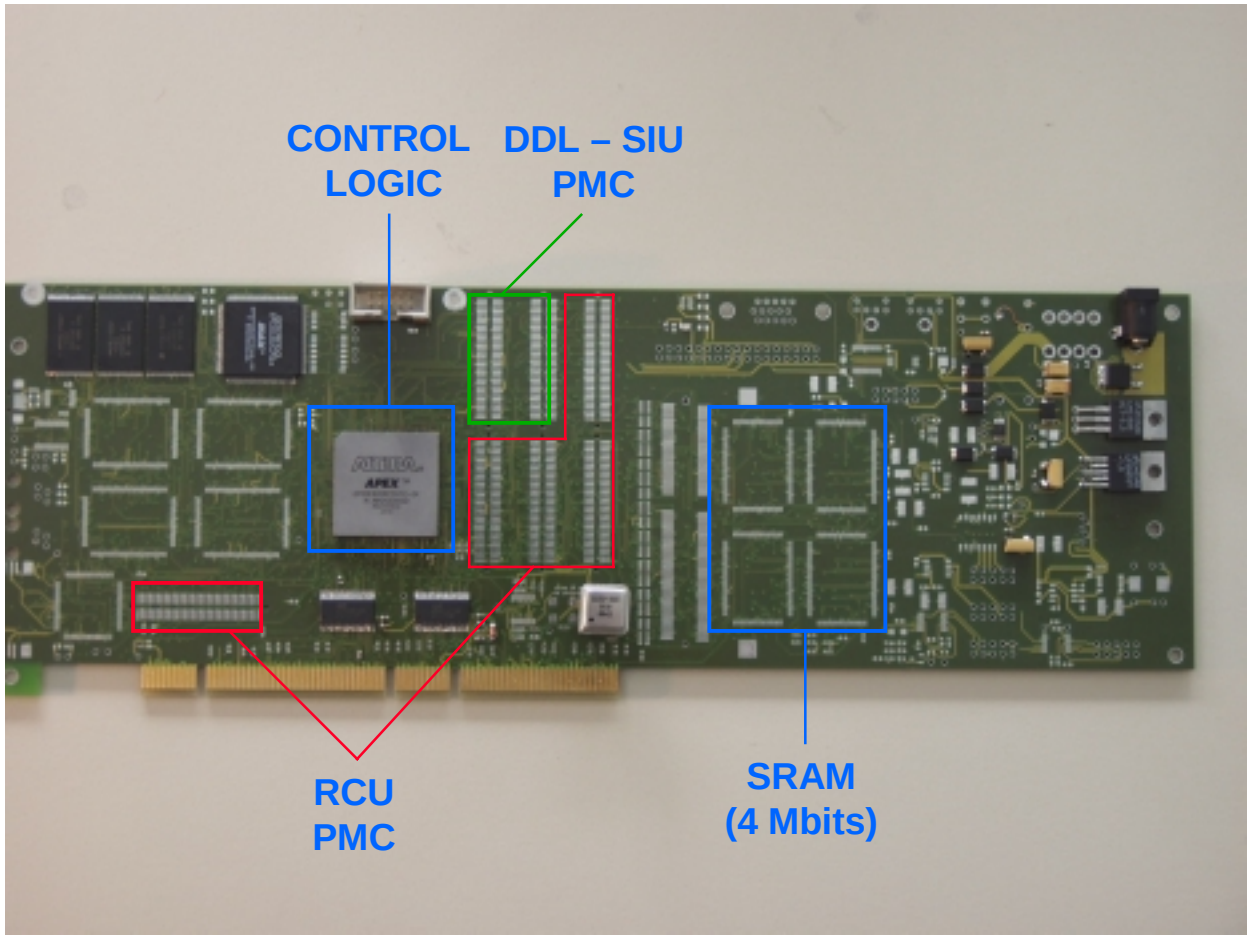
GTL Transceivers

PMC connectors

FRONT END CARD + READOUT CONTROL UNIT



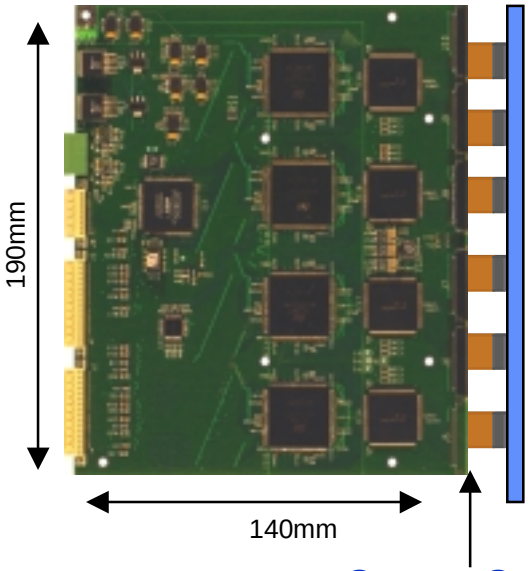
READOUT CONTROL UNIT
SECOND PROTOTYPE



MOUNTING

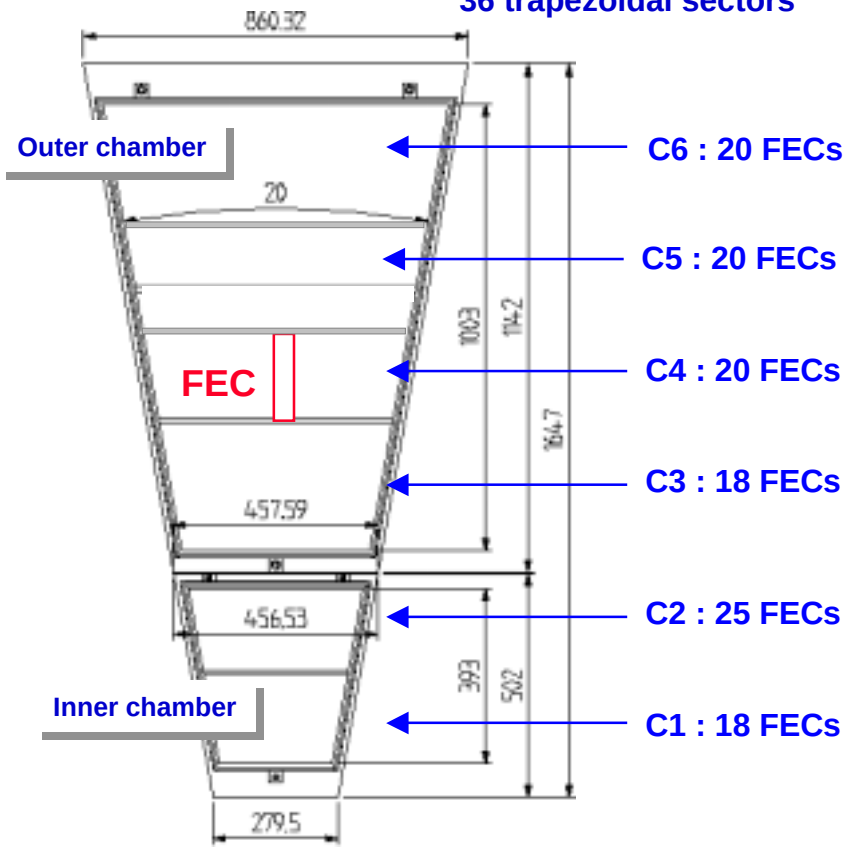
SIDE VIEW

128 channels
Front End Card (FEC)



FRONT VIEW

36 trapezoidal sectors



FEE POWER:

- **CHANNEL:** 40 mW
- **BOARD:** 6.9 W
- **SECTOR:** 832 W
- **TOTAL:** 30.2 KW

SUMMARY

- **The TPC FEE consists of 4 basic components:**
  - PASA (40 000 chips)
  - ALTRO (40 000 chips)
  - FEC (4500 boards)
  - RCU (220 boards)

- **Production:**
  - ALTRO: Apr ‘02
  - PASA: Nov ’02
  - FEC: Jan ’03

- **A significant fraction of the complete electronics (5.000 channels) connected to the IROC will be tested during Summer ‘02**