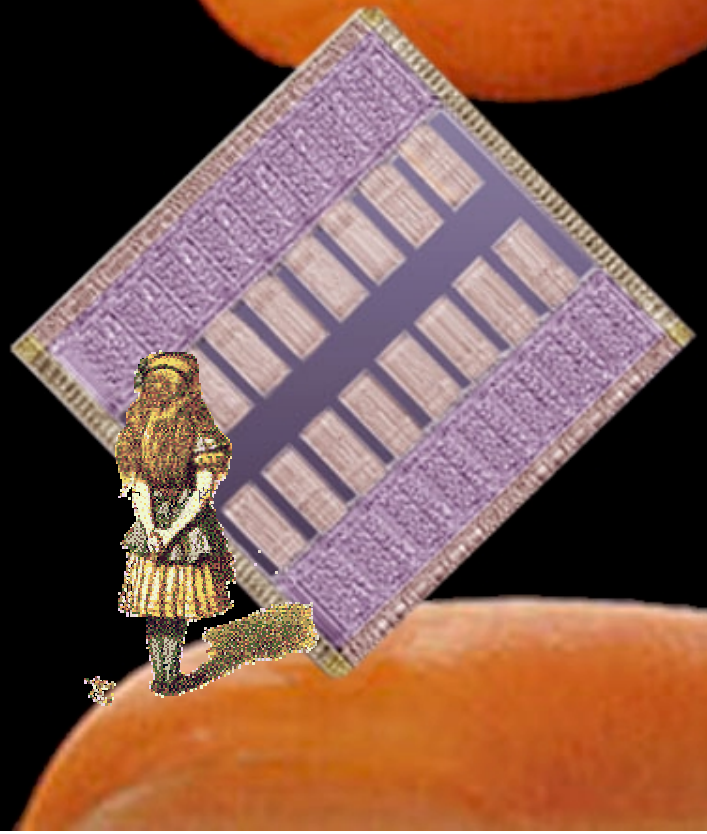
TPC FRONT END ELECTRONICS

Progress Report

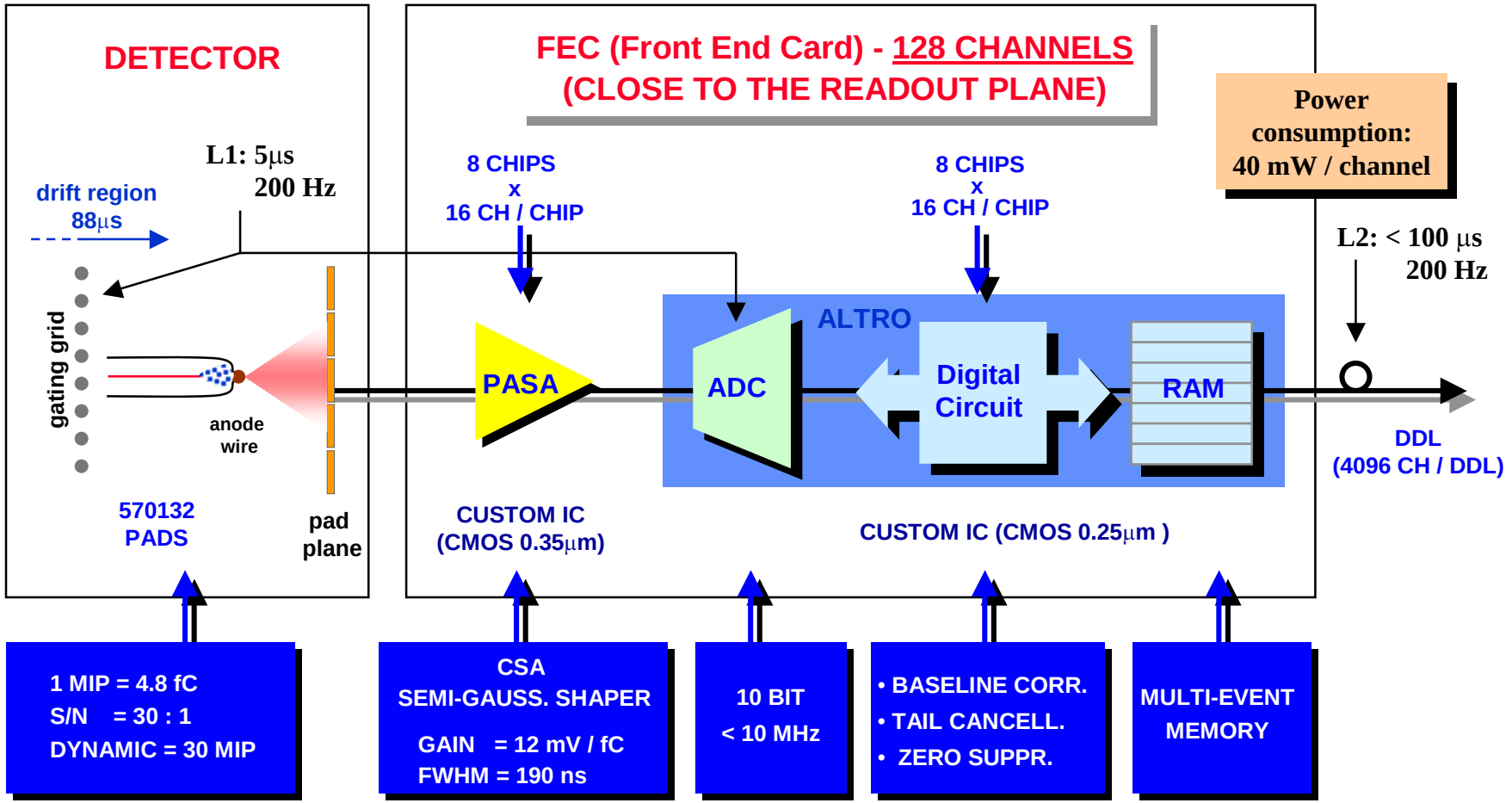
CERN – 1 July 2002

FEE TEAM: Bergen
CERN
Darmstadt TU
Frankfurt
Heidelberg
Lund
Oslo



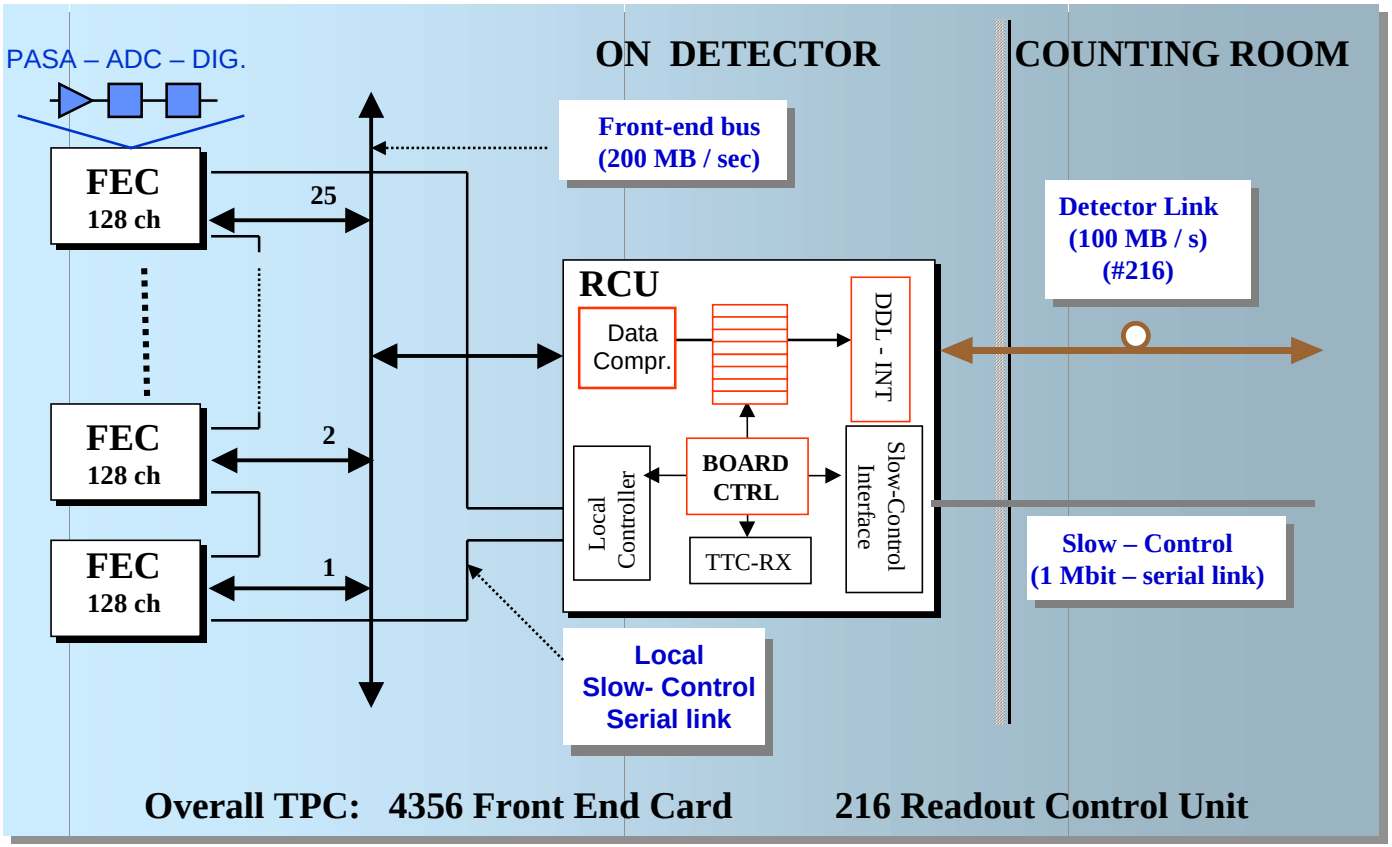
Luciano Musa - CERN

BASIC READOUT CHAIN

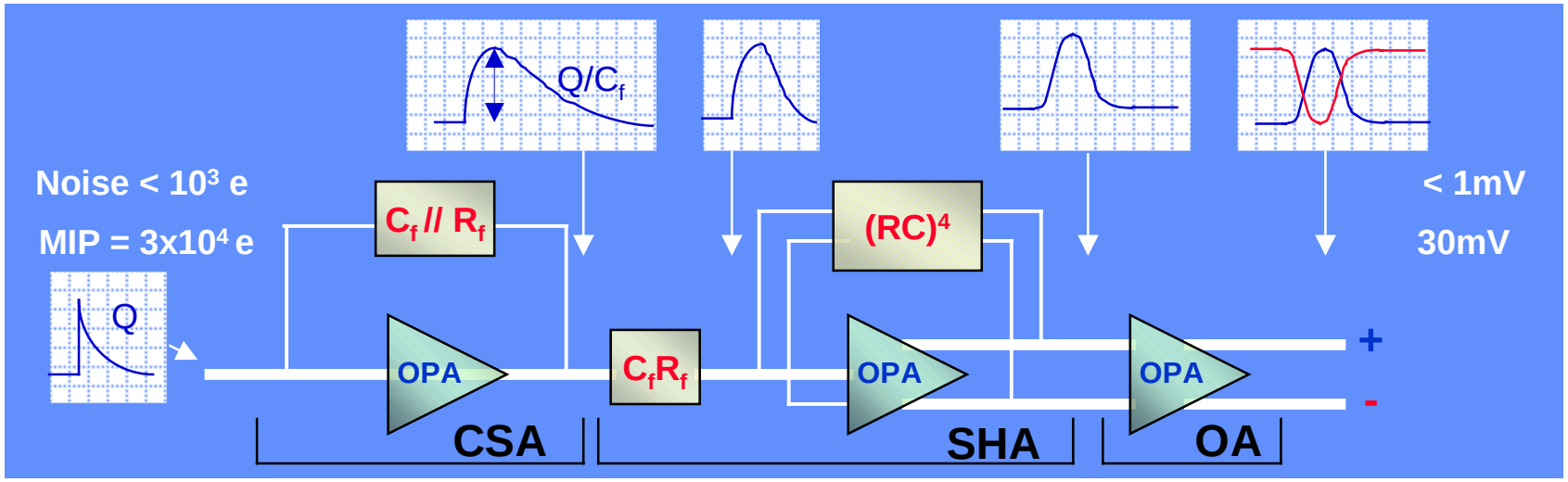


GLOBAL ARCHITECTURE

Each TPC Sector is served by 6 Readout Subsystems



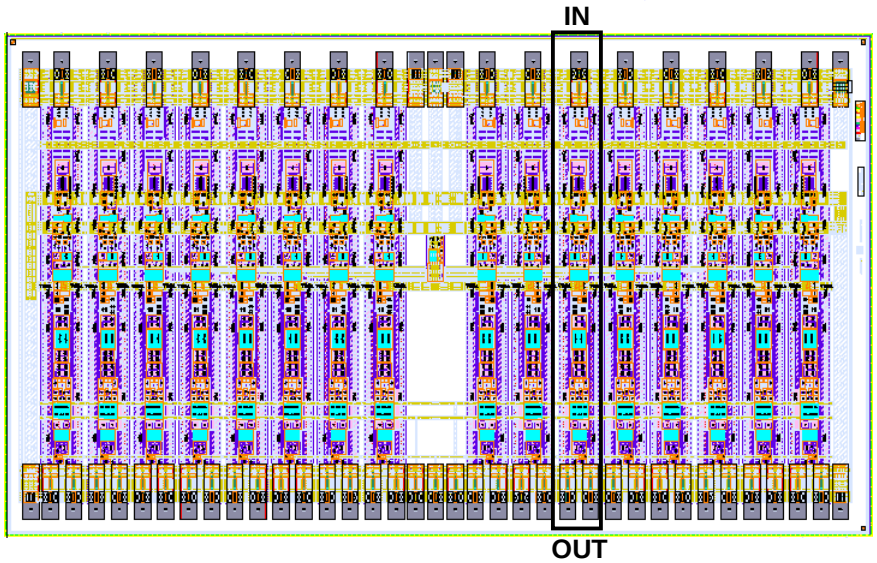
PRE-AMPLIFIER SHAPING AMPLIFIER (PASA) MAIN FEATURES



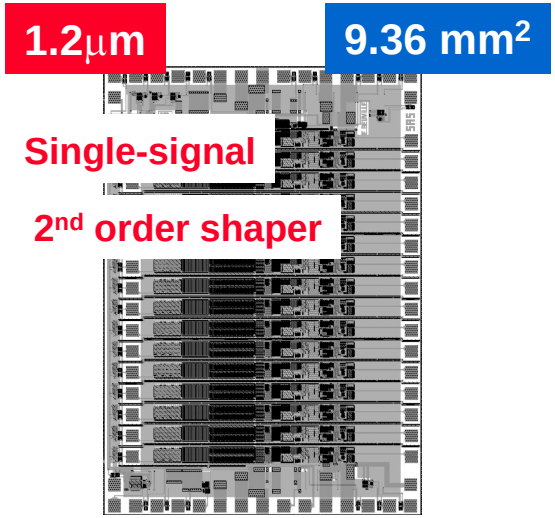
MAIN REQUIREMENTS

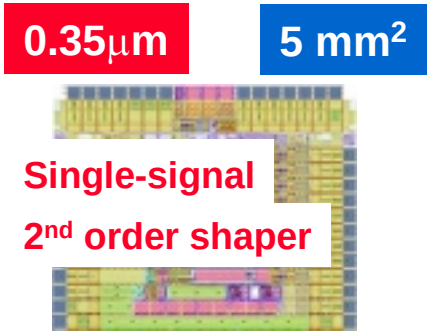
- Gain: 12mV / fC (@ 12pF)
- FWHM: 190ns
- Noise: < 1000e (@ 12pF)
- INL: < 1%
- Crosstalk: < 0.3%
- Power: < 20 mW / ch

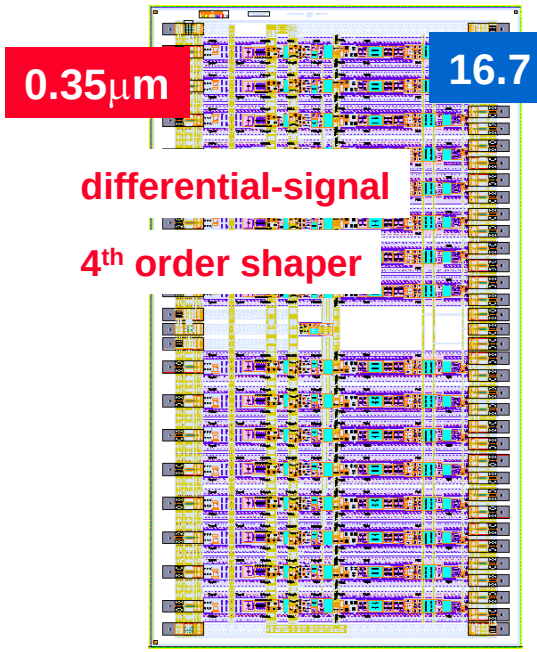
CHIP LAYOUT (AMS 0.35μm)



THE PASA CONTEST



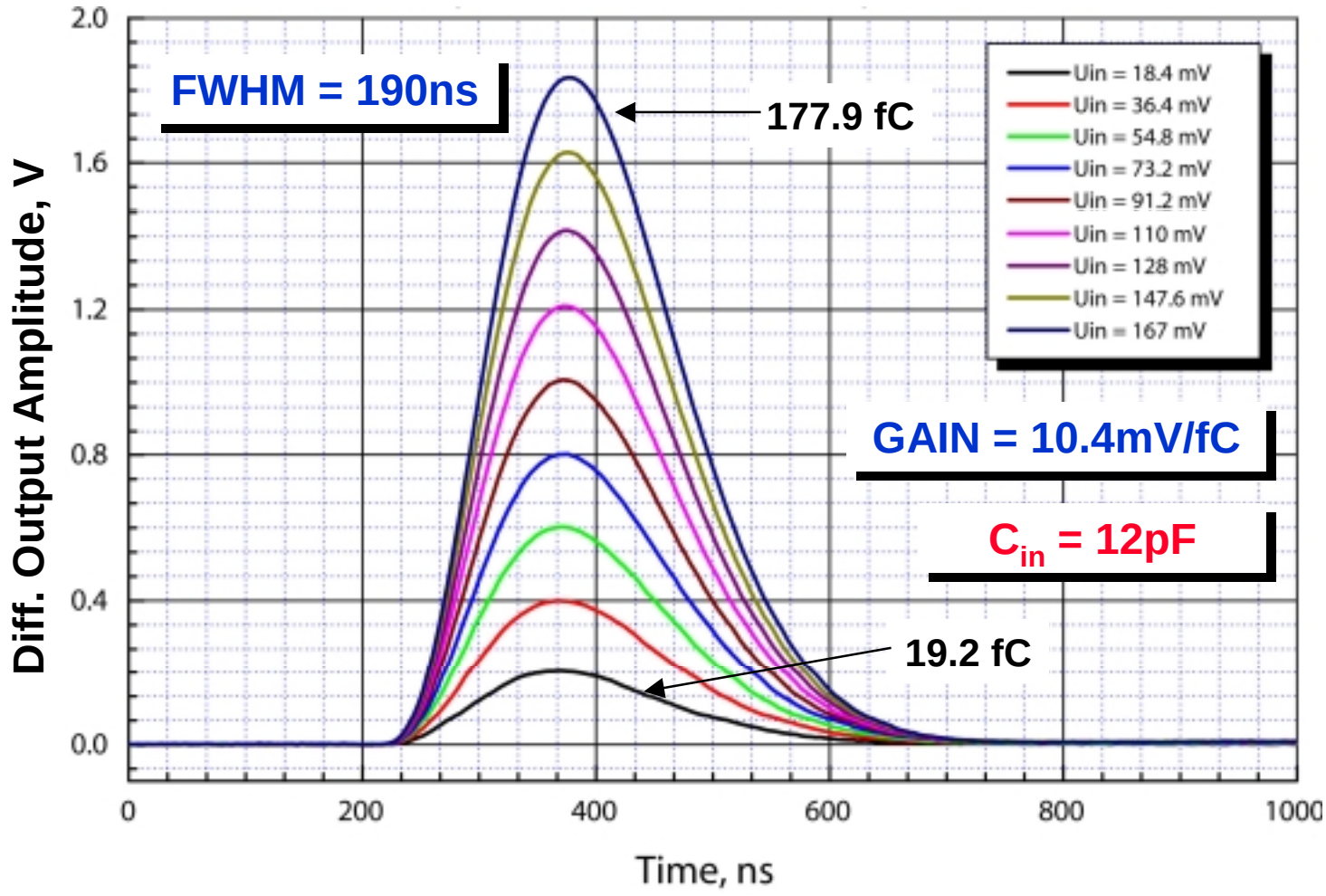




Nr. CH: 16	Nr. CH: 9	Nr. CH: 16
POWER/CH: 47mW	POWER/CH: 7.25mW	POWER/CH: 12mW
NOISE (12pF): 722 e	NOISE (12pF): 670 e	NOISE (12pF): 566 e
1996	2000	2001
STAR TPC	ALICE TPC prototype	ALICE TPC final

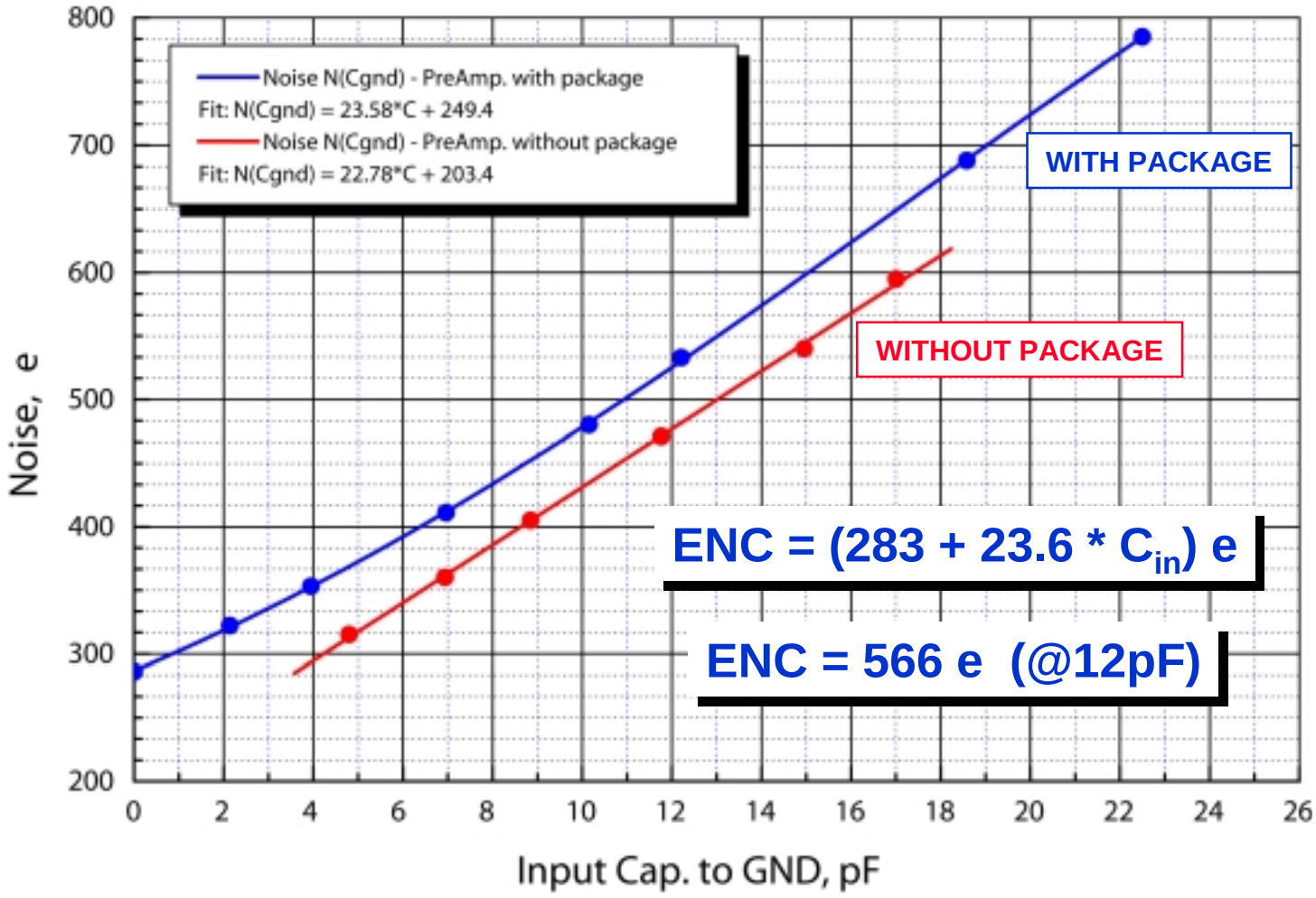
PULSE SHAPE

REQUIREMENTS: FWHM = 190ns, GAIN = 12mV/fC



EQUIVALENT NOISE CHARGE

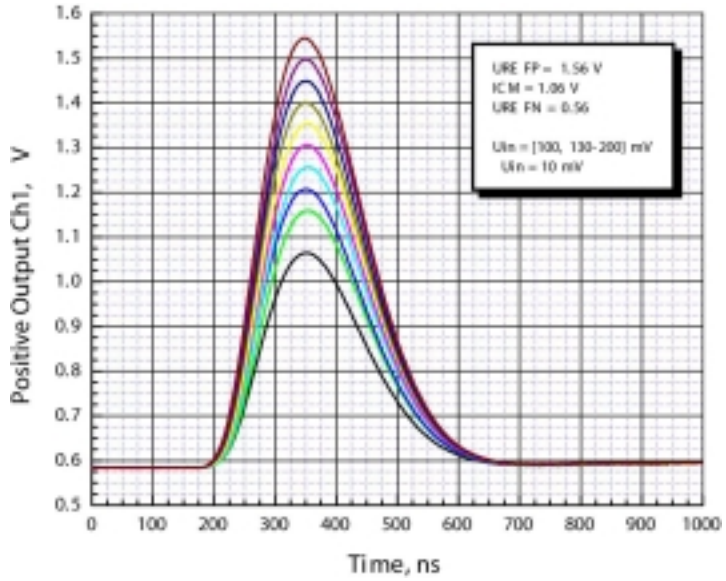
REQUIREMENT: ENC < 1000 e (@12pF)

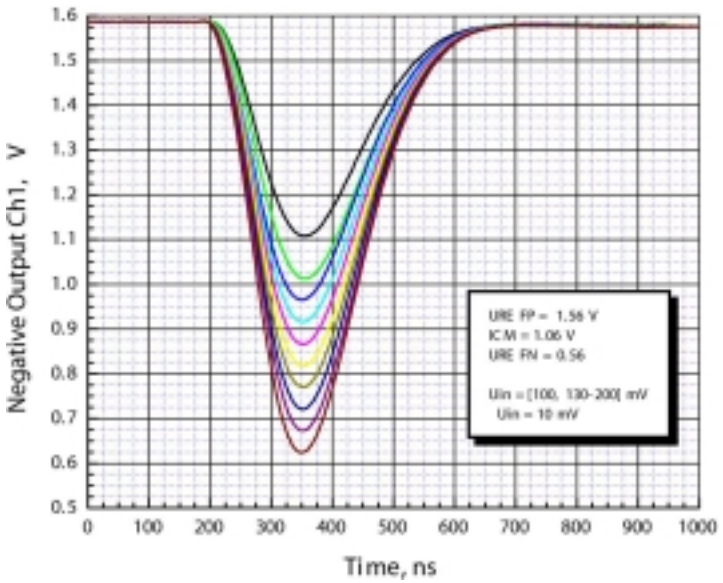


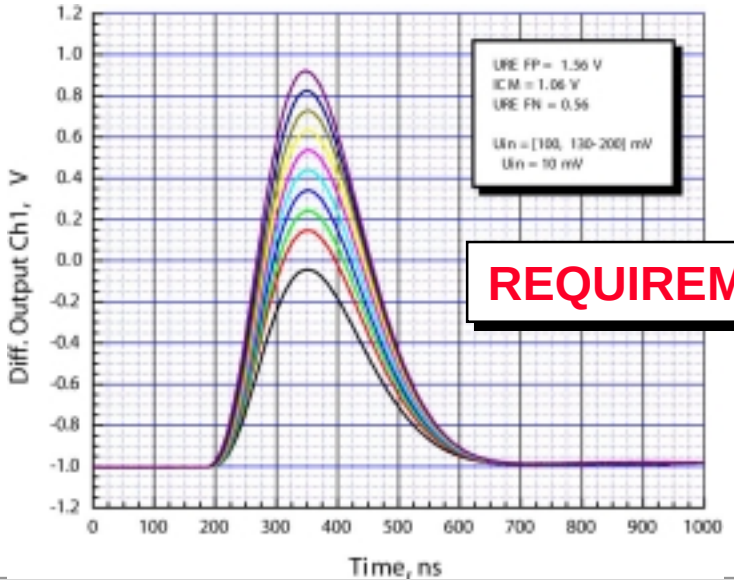
ENC = (283 + 23.6 * C_{in}) e

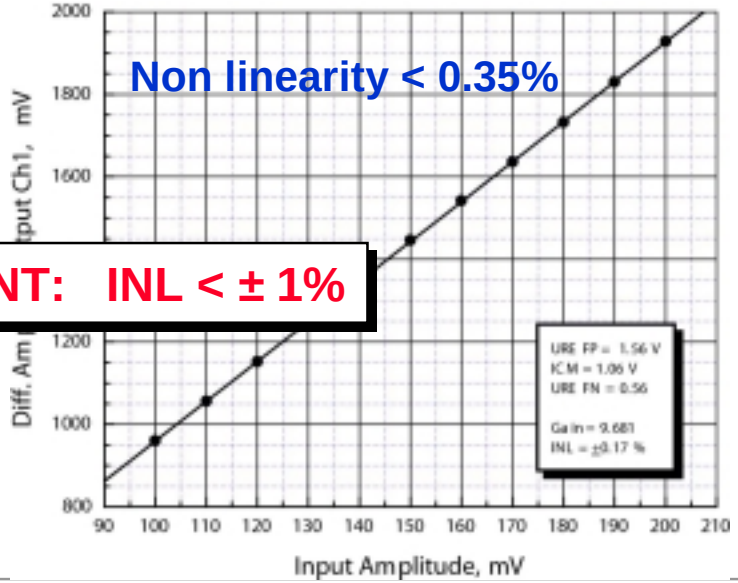
ENC = 566 e (@12pF)

LINEARITY



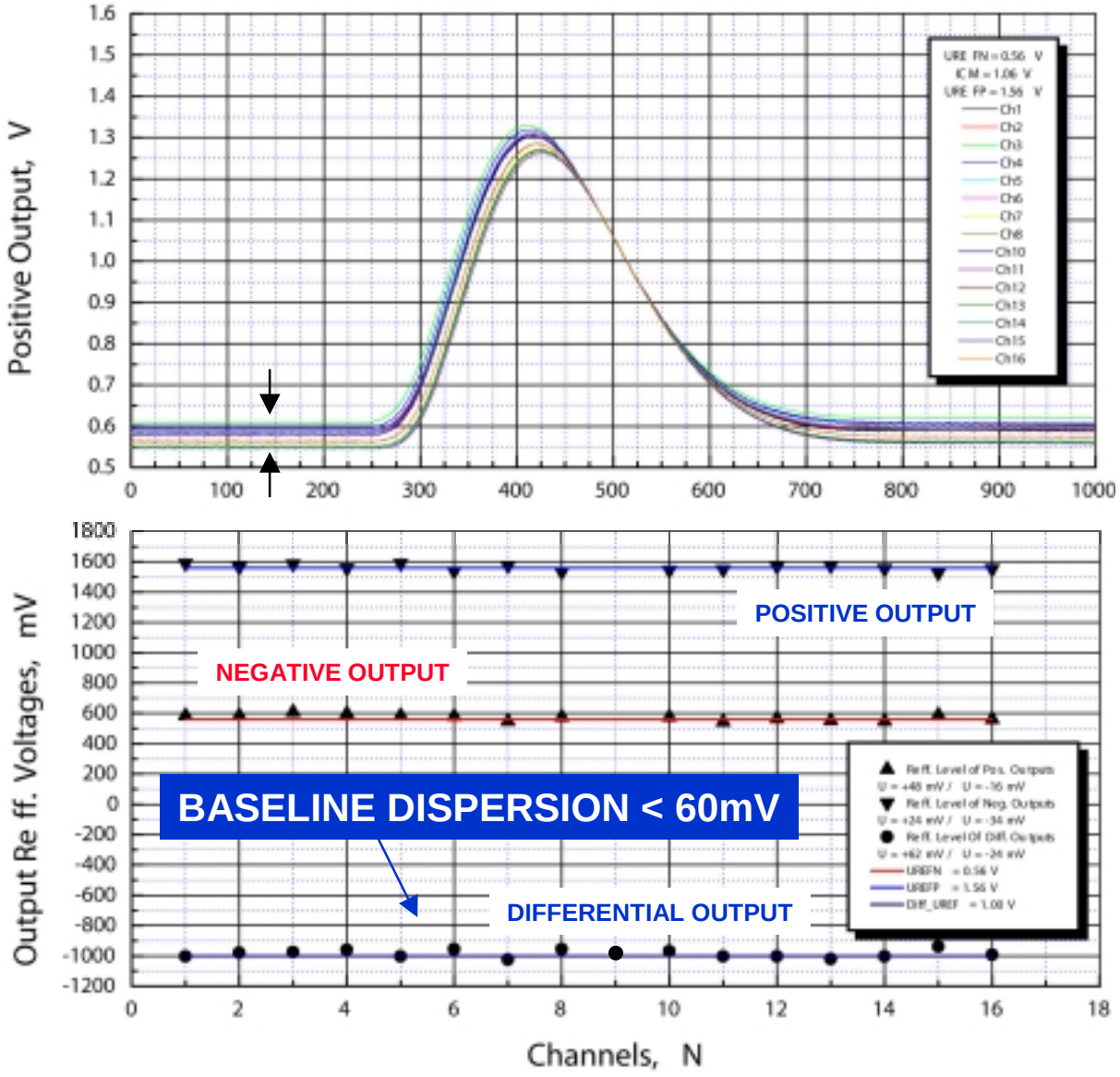




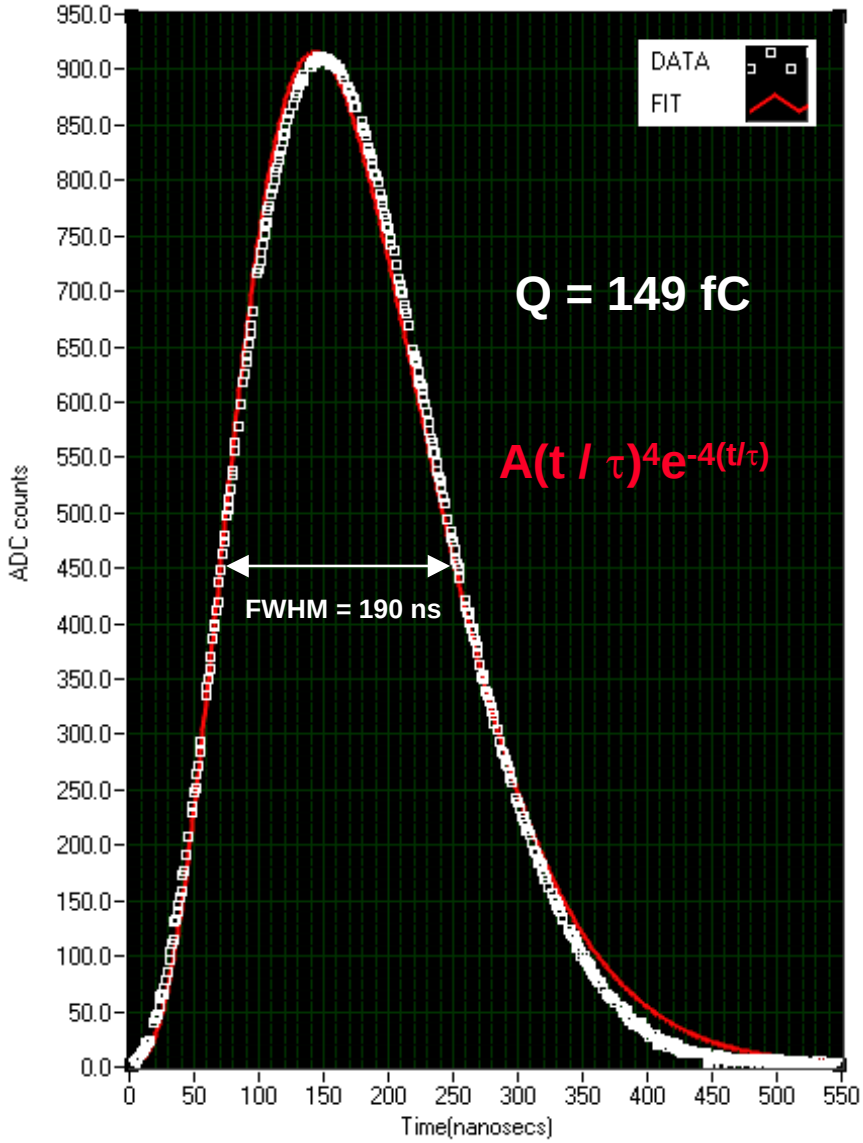


REQUIREMENT: INL < ± 1%

BASELINE DISPERSION



PERFORMANCE OF PASA EMBEDDED IN FEC



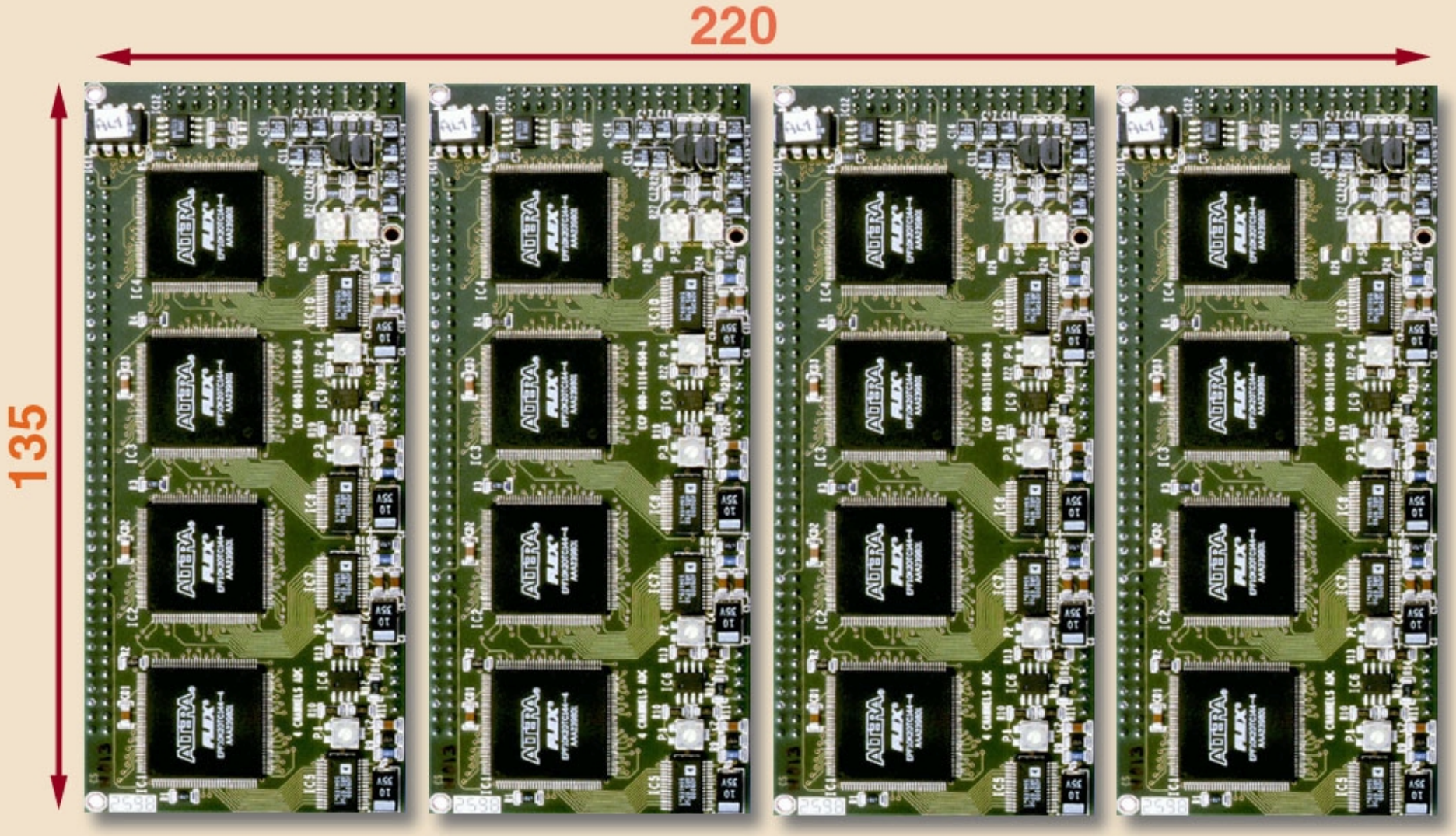
Parameter	Requirement	Measured (preliminary)
Noise	1000 e	(600 + 23/pF) e
Conversion gain	12mV / fC	10.8 mV / fC (*)
Shaping time	190ns	190ns
Non linearity	<1%	< 0.35%
Crosstalk	<0.3%	<0.4%
Power consumption	< 20mW / ch	12mW / ch
Area		16.7mm^2

(*) to be corrected in the ER

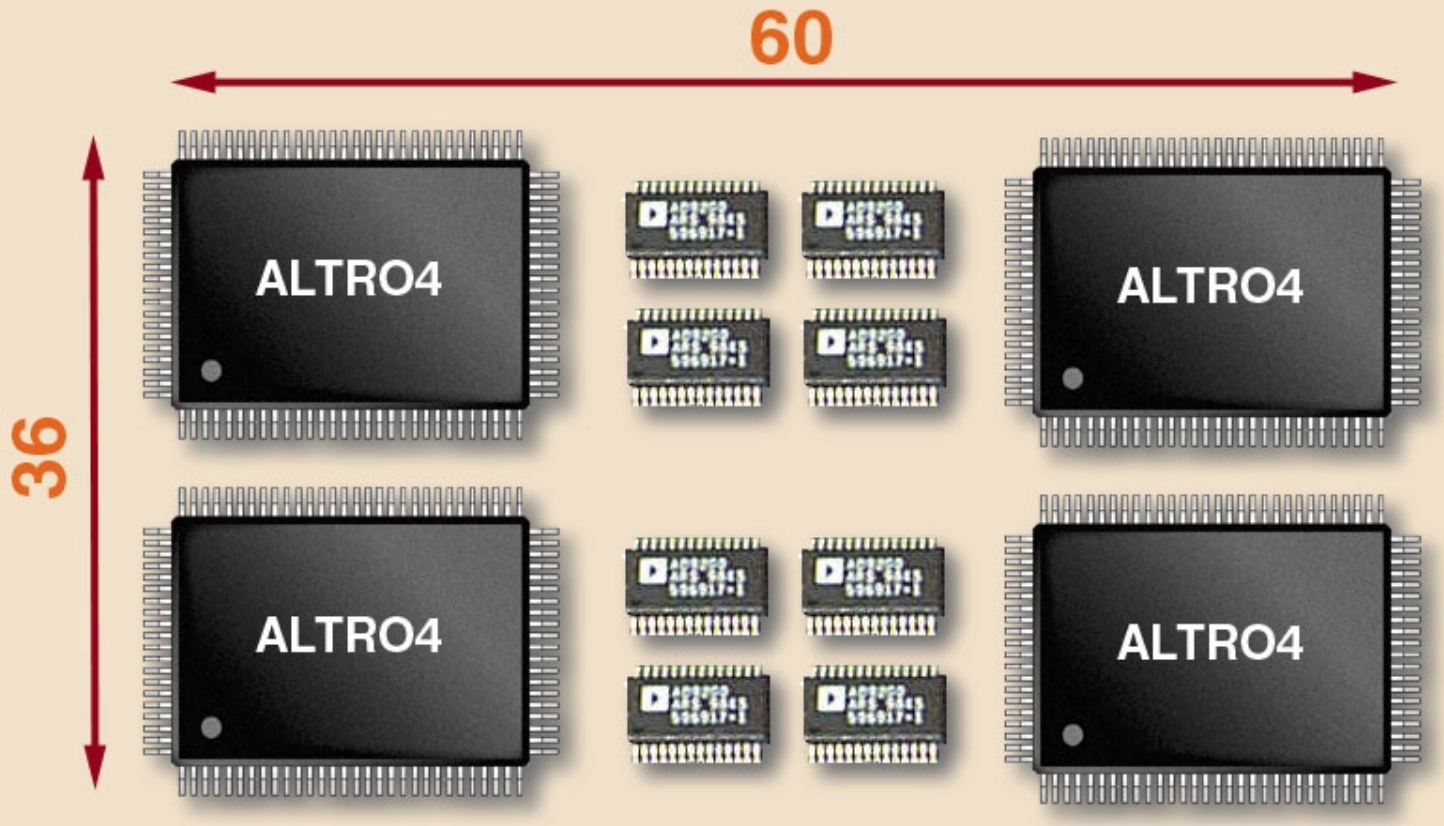
MILESTONES

- ✦ **January '02:** delivery of 40 samples of final PASA
- ✦ **Feb - Apr '02:** test of PASA in stand-alone mode
- ✦ **May '02:** integration of PASA in the FEC
- ✦ **July '02:** test of PASA connected to the IROC
- ✦ **July '02:** delivery of additional 200 samples
- ✦ **July '02:** engineering run (*)
- ✦ **October '02:** full production

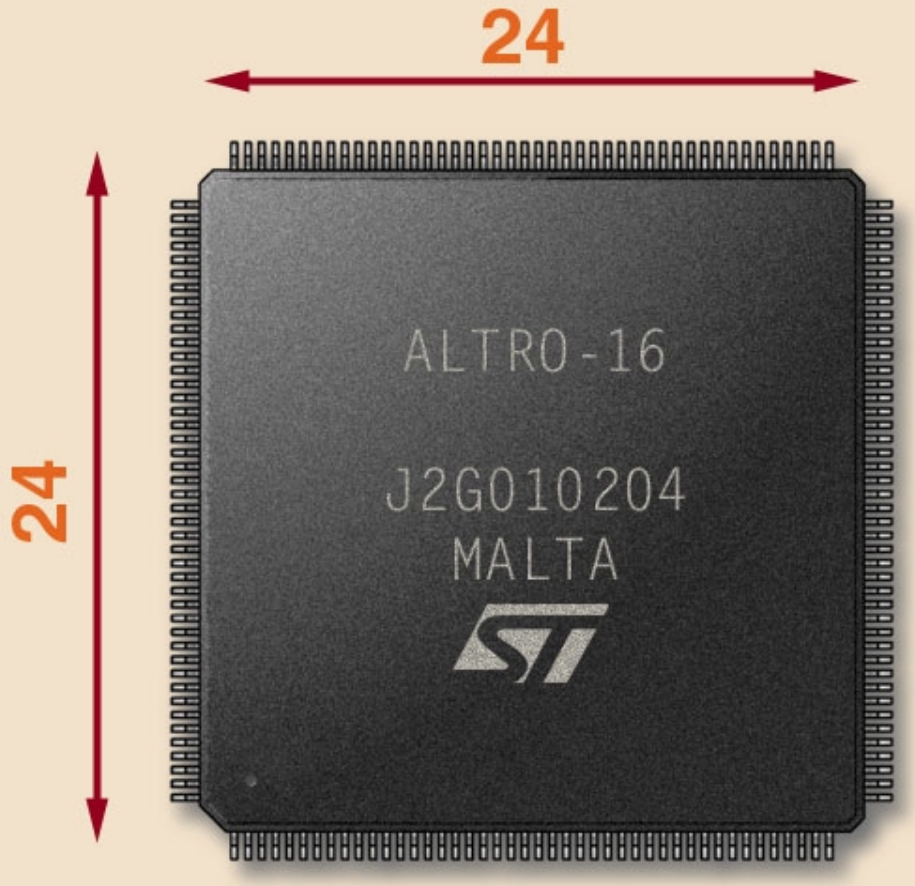
BASIC COMPONENTS - ALTRO



16 channels in 1998

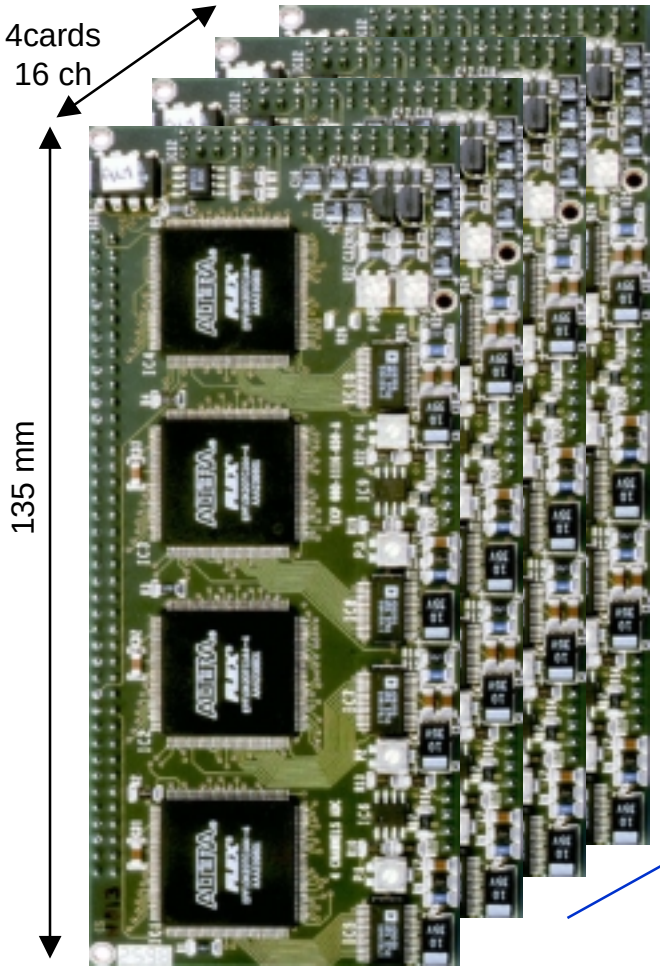


16 channels in 1999

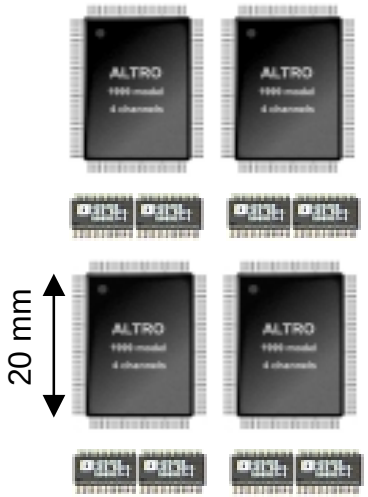


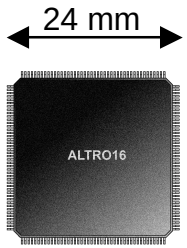
16 channels in 2002

ALTRO - SUMMARY OF THE PROTOTYPING ACTIVITIES



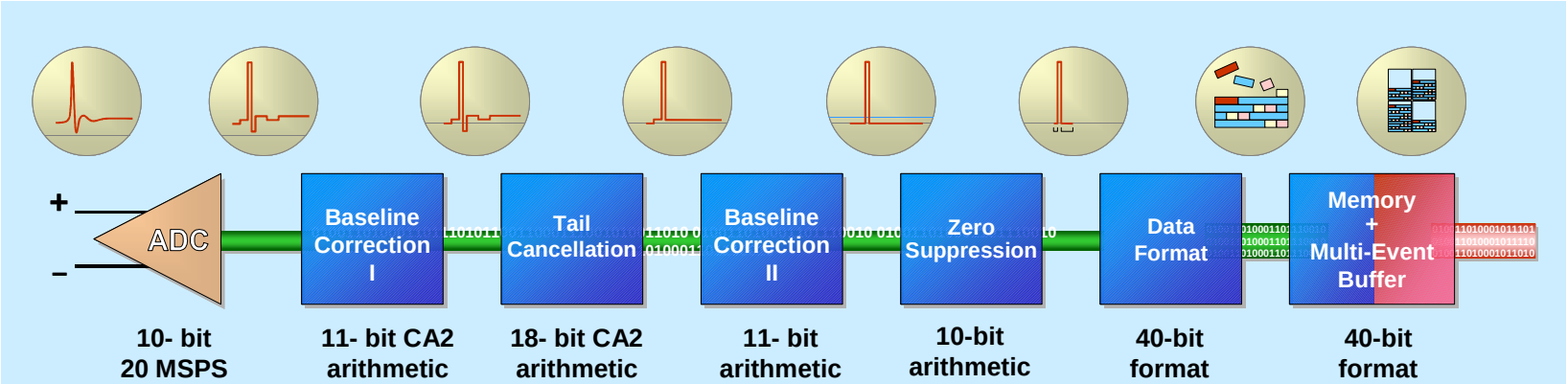
4 PQFP 100
8 SSOP 28





Integrated ADCs

1998	1999	2001
CHANNELS / CHIP: 1	CHANNELS / CHIP: 4	CHANNELS / CHIP: 1
POWER / CH: 120mW	POWER / CH: 80mW	POWER / CH: 16mW
PRICE / CH: 50CHF	PRICE / CH: 8CHF	PRICE / CH: 5CHF

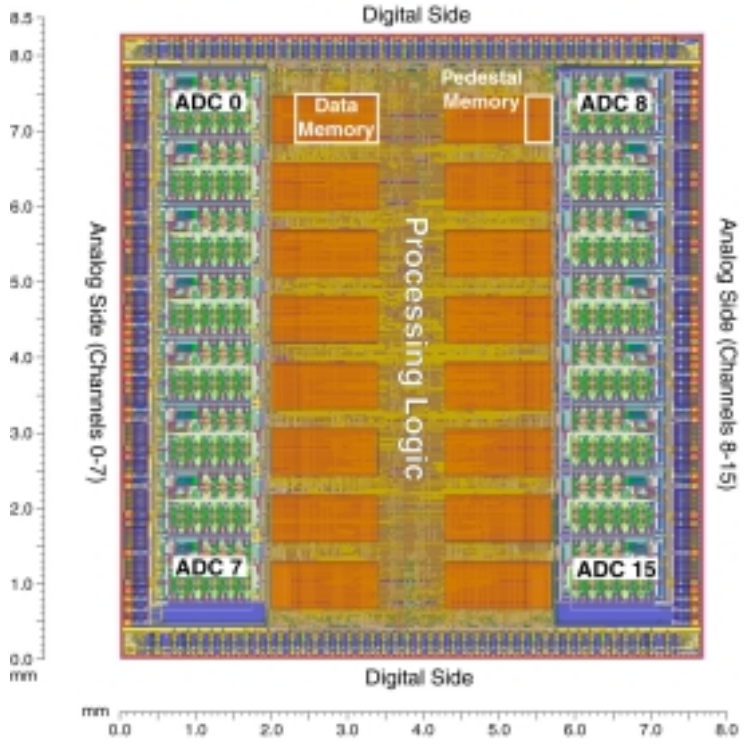


MAX SAMPLING CLOCK 40 MHz

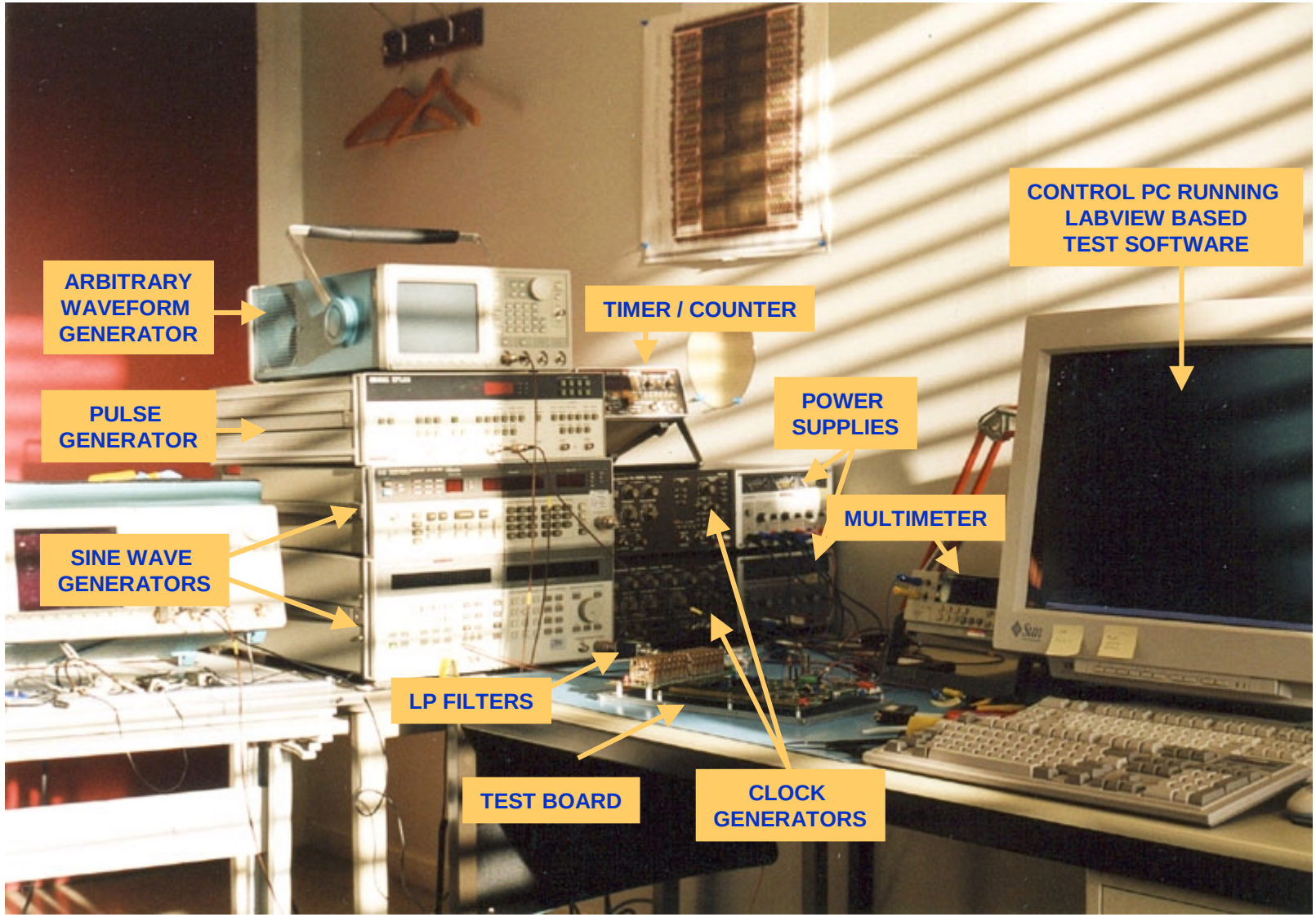
MAX READOUT CLOCK 60 MHz

16-ch signal digitizer and processor

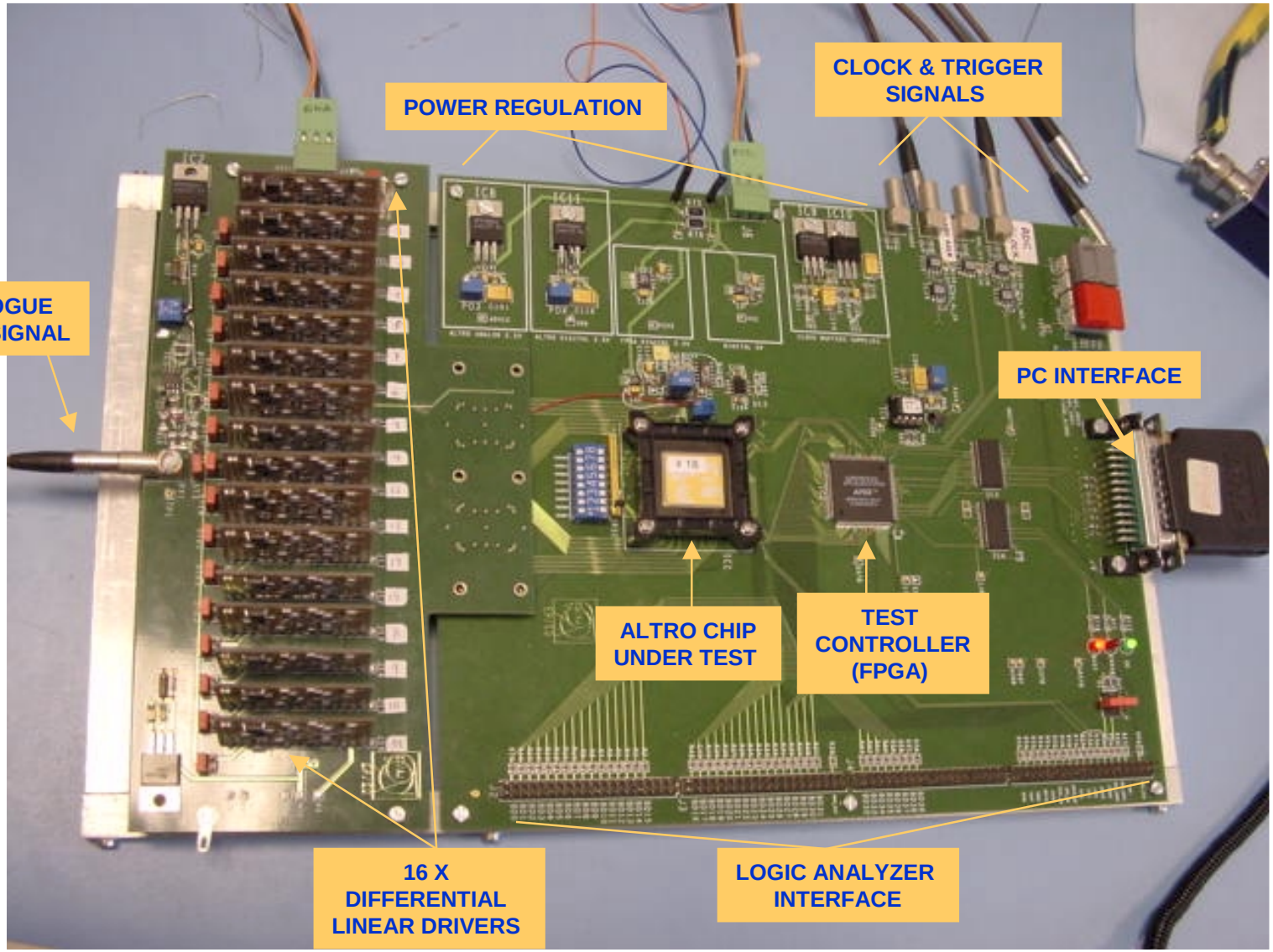
- HCMOS7 0.25 μm (ST)
- area: 64 mm^2
- power: 16 mW / ch
- prototype delivery: Feb ‘02
- 300 samples fully tested
- delivery of 4x10^4 chips: Dec ‘02



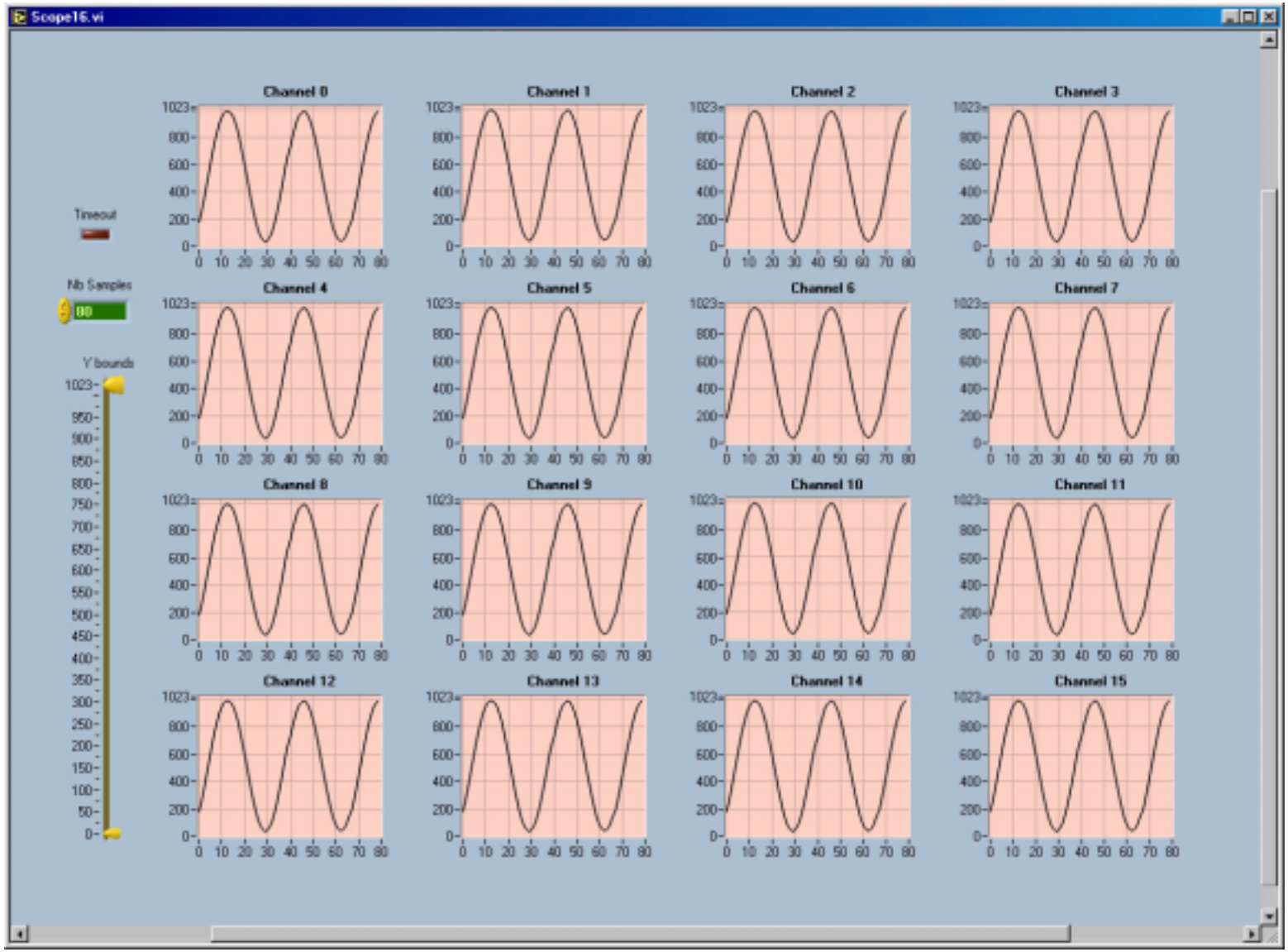
ALTRO TEST SETUP



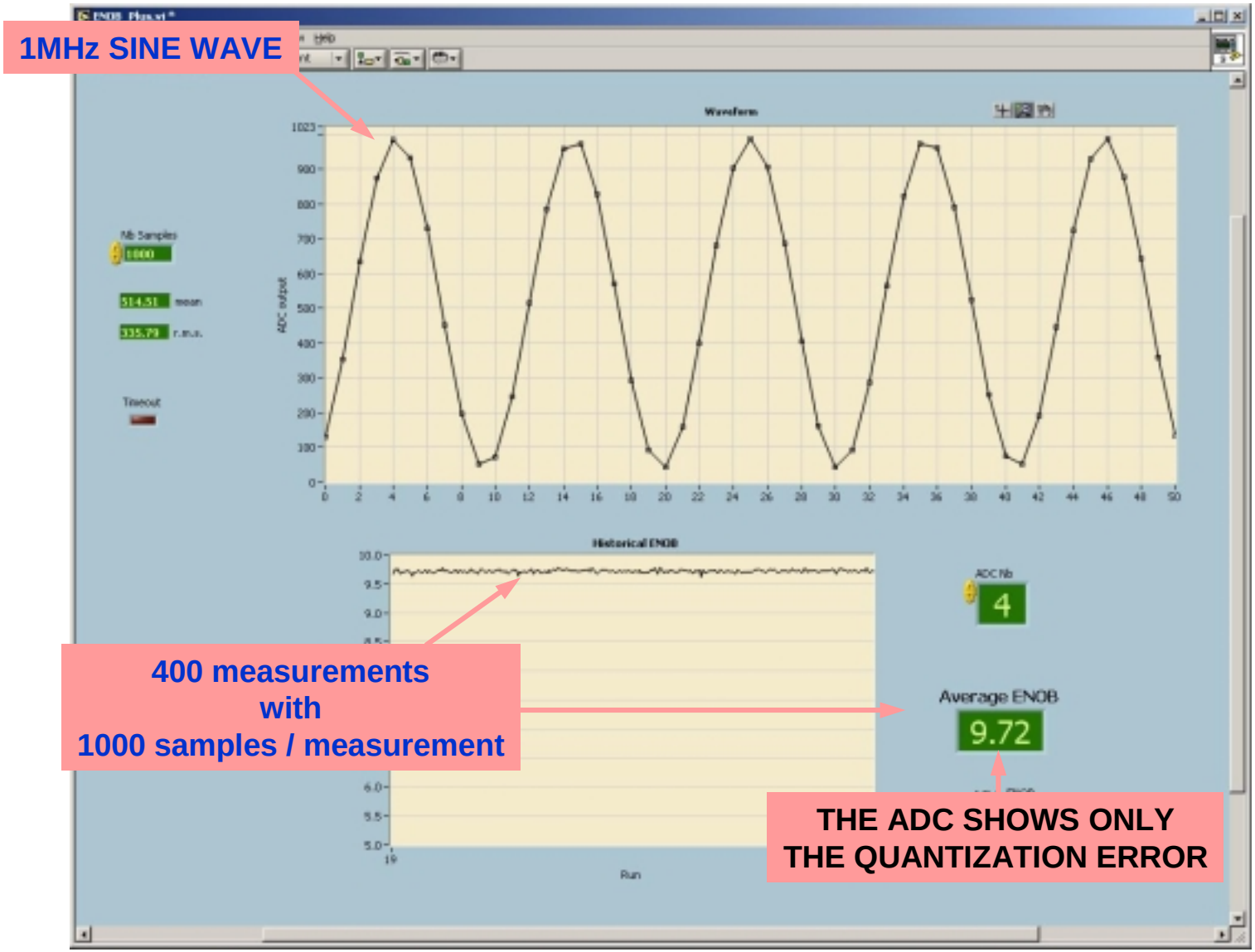
ALTRO TEST BOARD



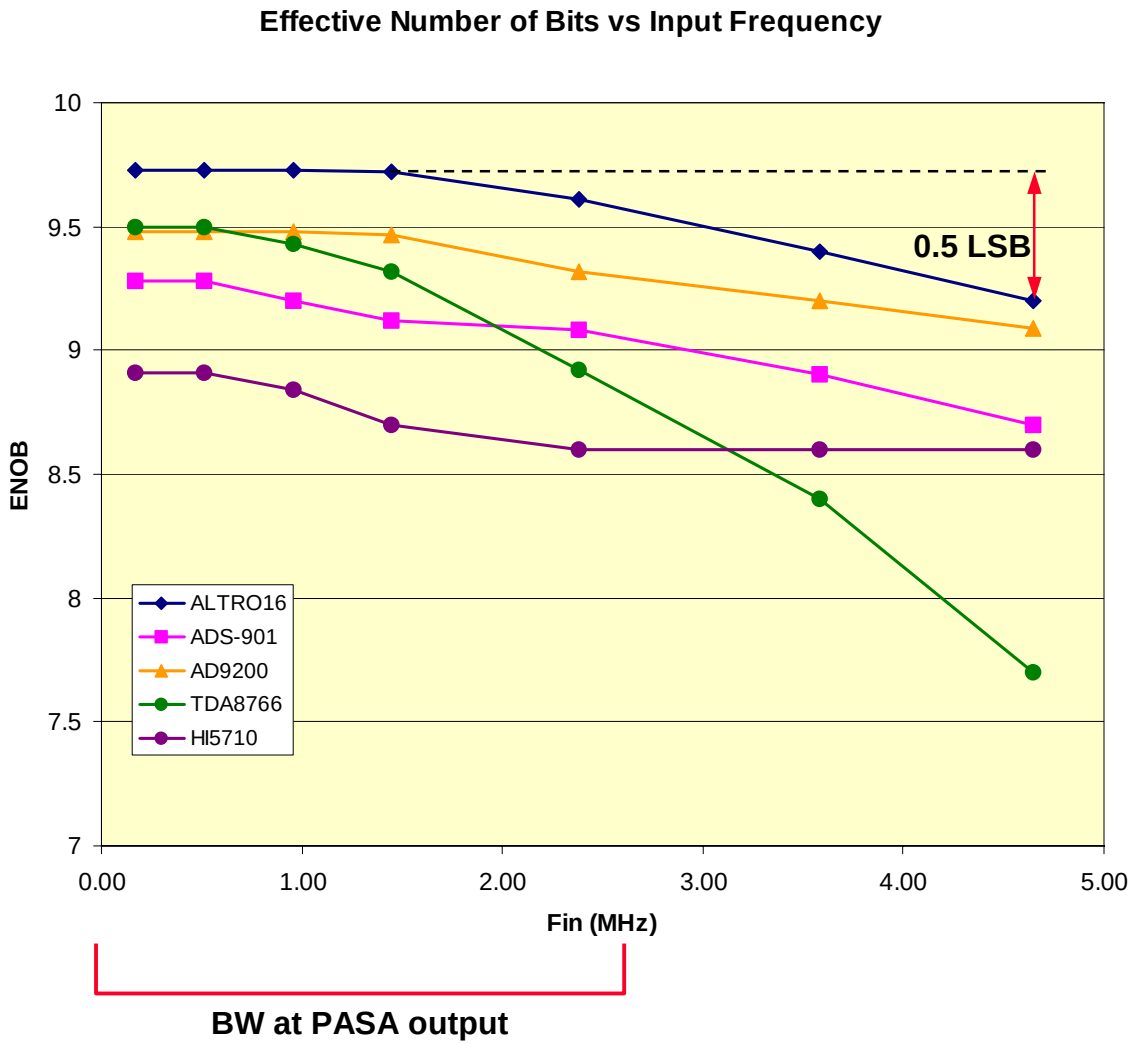
16 CHANNELS IN ONE SHOT



EFFECTIVE NUMBER OF BITS (ENOB)



ENOB vs Frequency



Quartz Jitter:

25ps r.m.s.

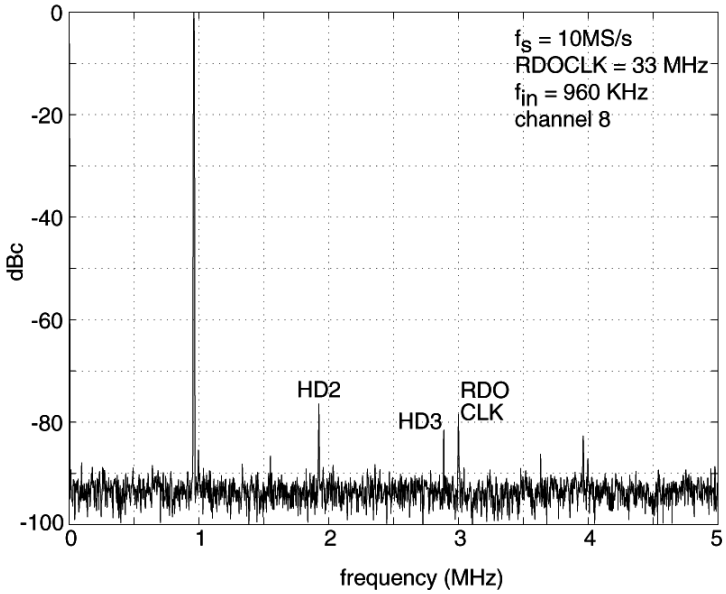
Amplitude Uncertainty:

$$4 \cdot f_{in} \cdot \text{jitter} \cdot 2^{10}$$

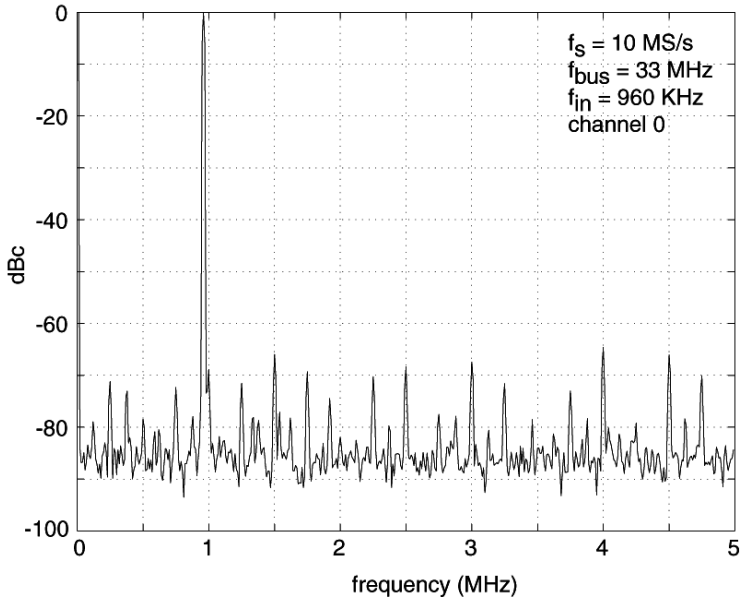
0.5 bits at 4.8 MHz

Crosstalk and Digital Noise

DIGITAL NOISE



Readout Clock below -78 dBc (WC)



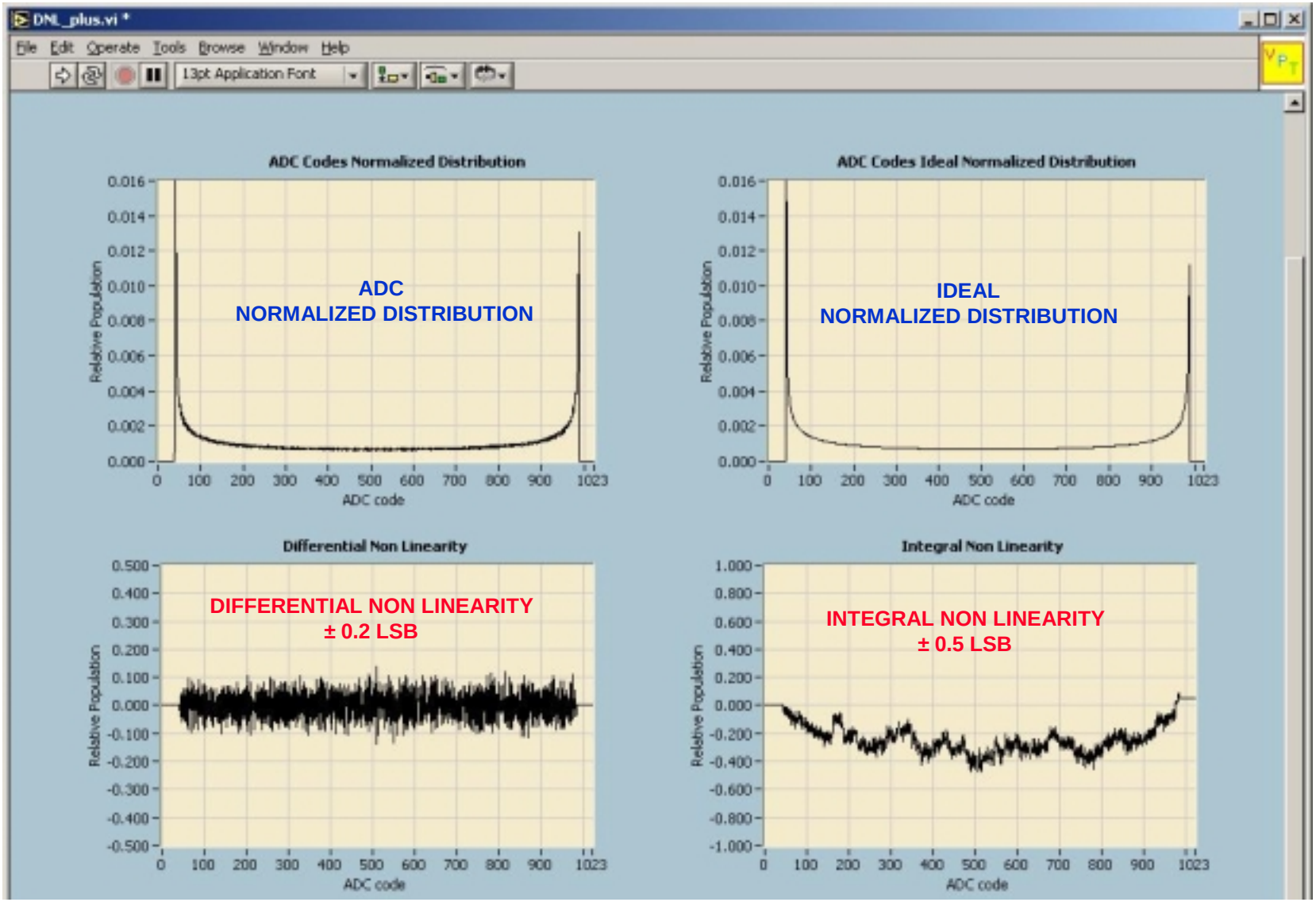
Bus interference below -65 dBc (WC)

CHANNEL-TO-CHANNEL CROSSTALK

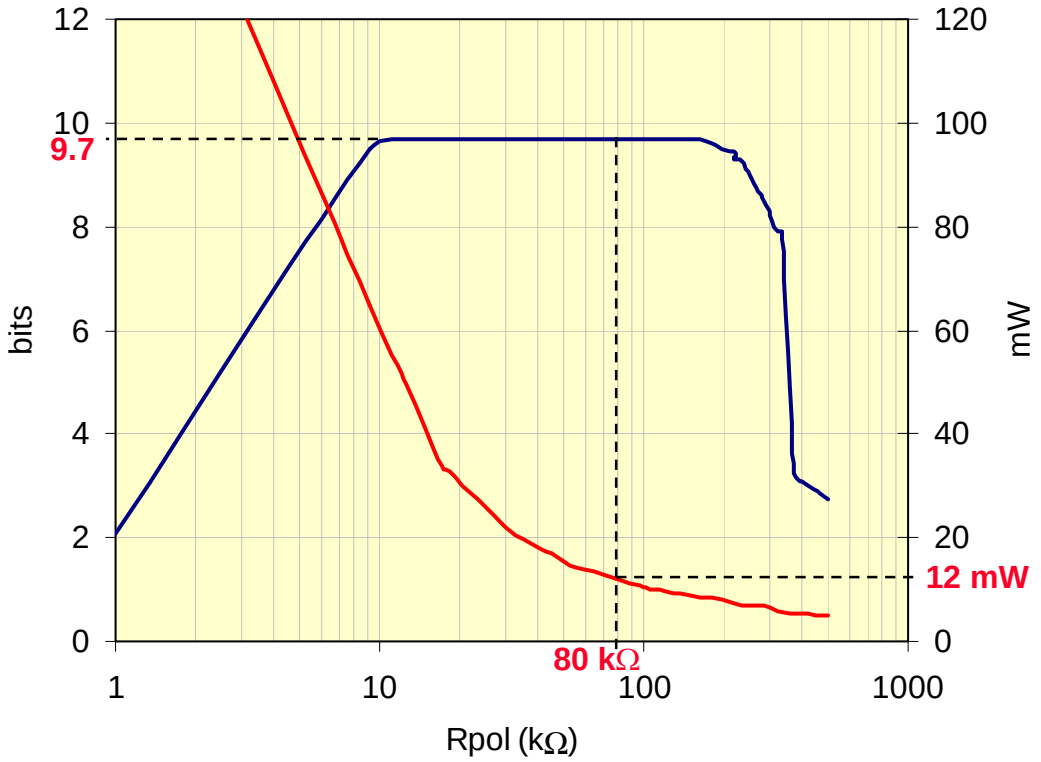
F_{in} = 1 MHz 0.05 LSB rms (-80 dBc)
F_{in} = 5 MHz 0.2 LSB rms (-68 dBc)

Dynamic Range of a 10-bit ADC: 60 dB

Differential and Integral Non-Linearity



POWER CONSUMPTION



Effective Number of Bits

Power Consumption per Channel

ONE CHIP		
	Digital leakage current	1.2 mA
	ADC Clock Tree (10 MHz)	23 mA
	Readout Clock Tree (40 MHz)	1.4 mA
	Processing Logic during Trigger (1%)	28 mA
	16 ADCs at 10 MS/s	77 mA

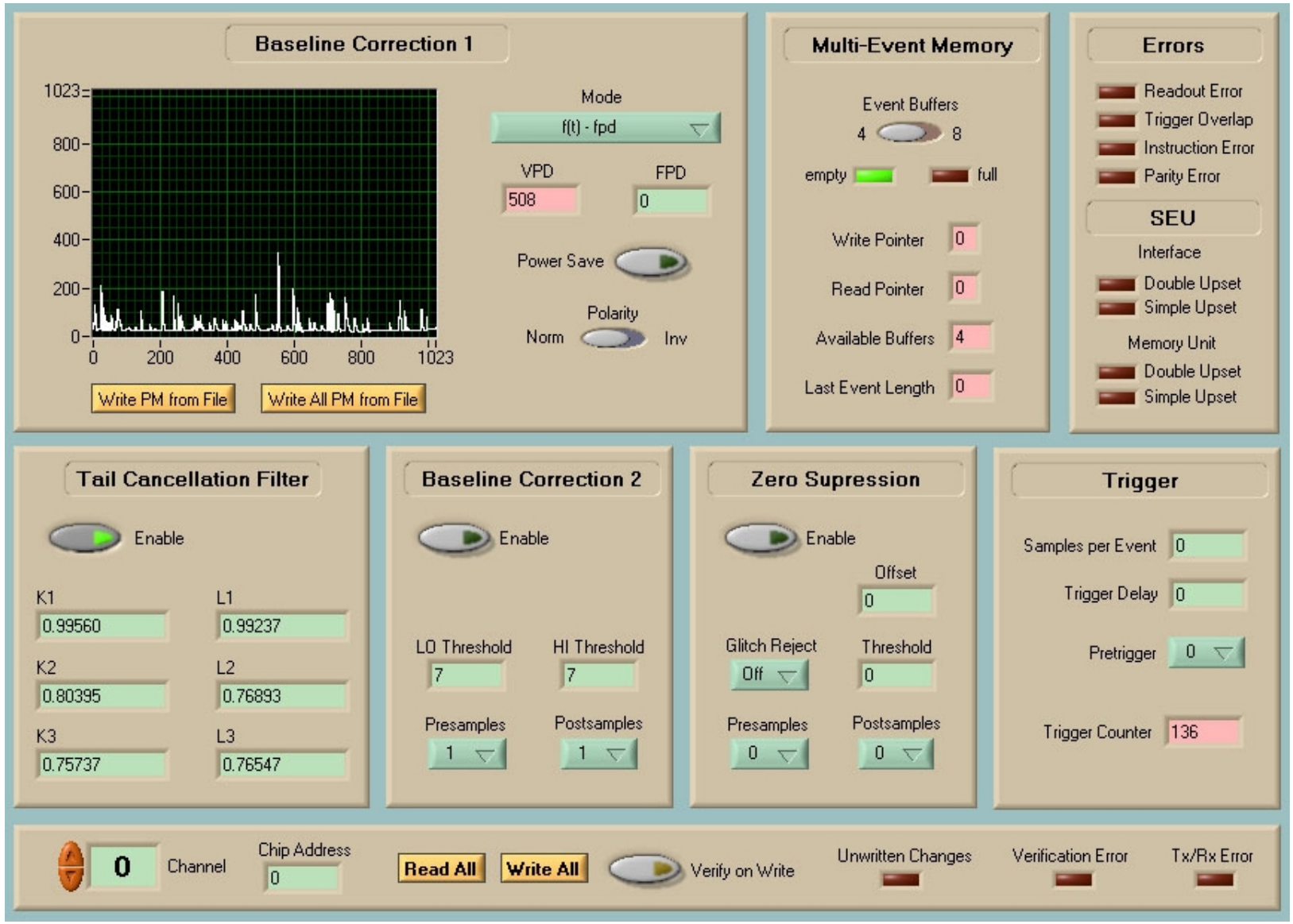
Average Power Per Chip

257 mW

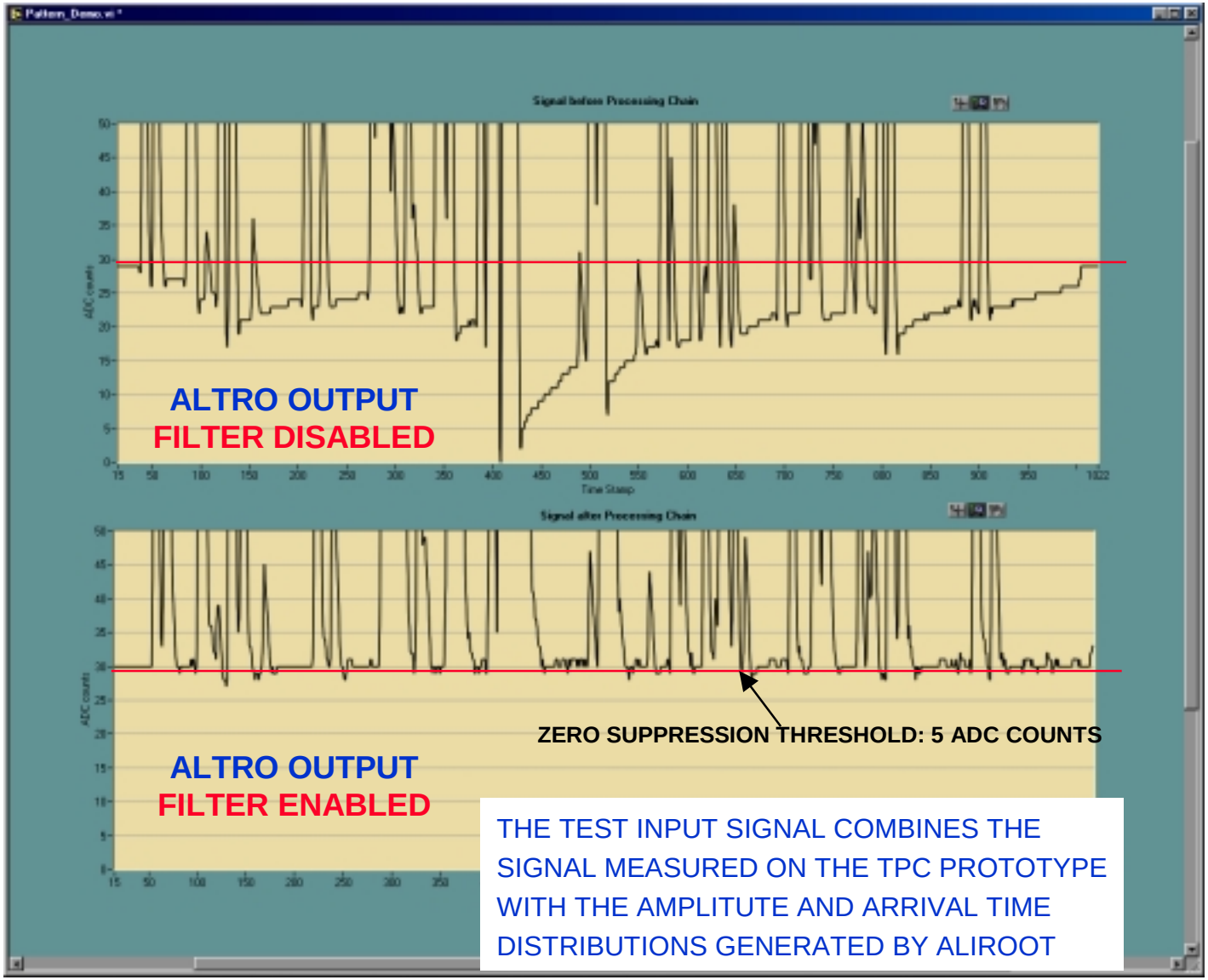
Average Power Per Channel

16 mW

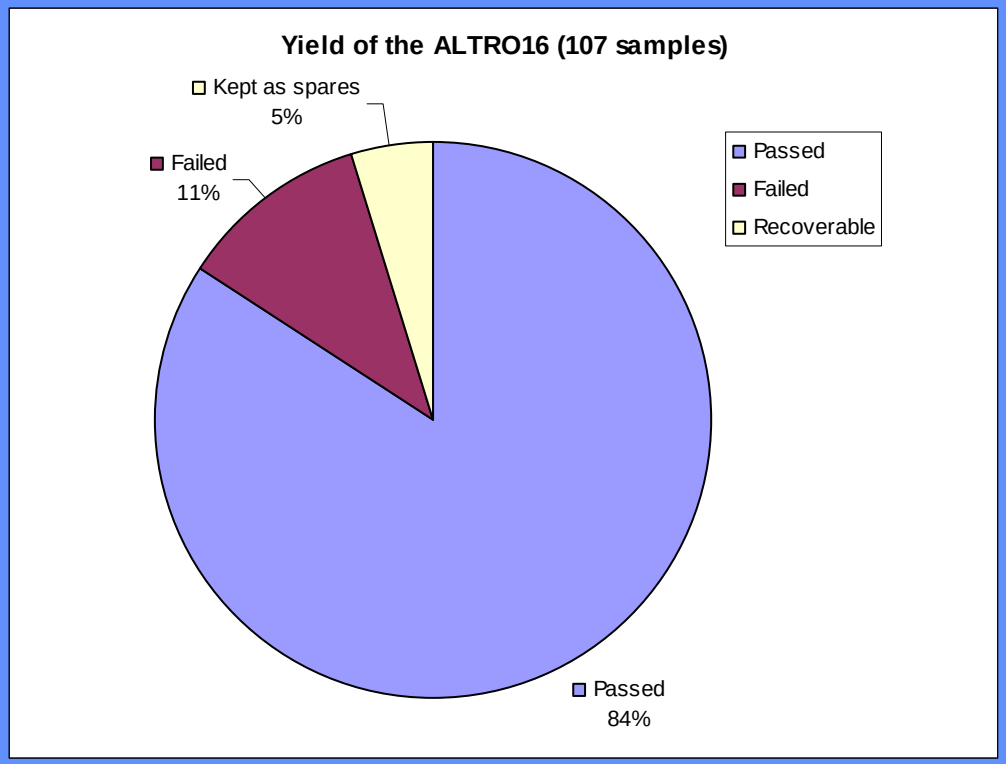
FUNCTIONAL VALIDATION - ALTRO CONTROL PANNEL



FUNCTIONAL VALIDATION



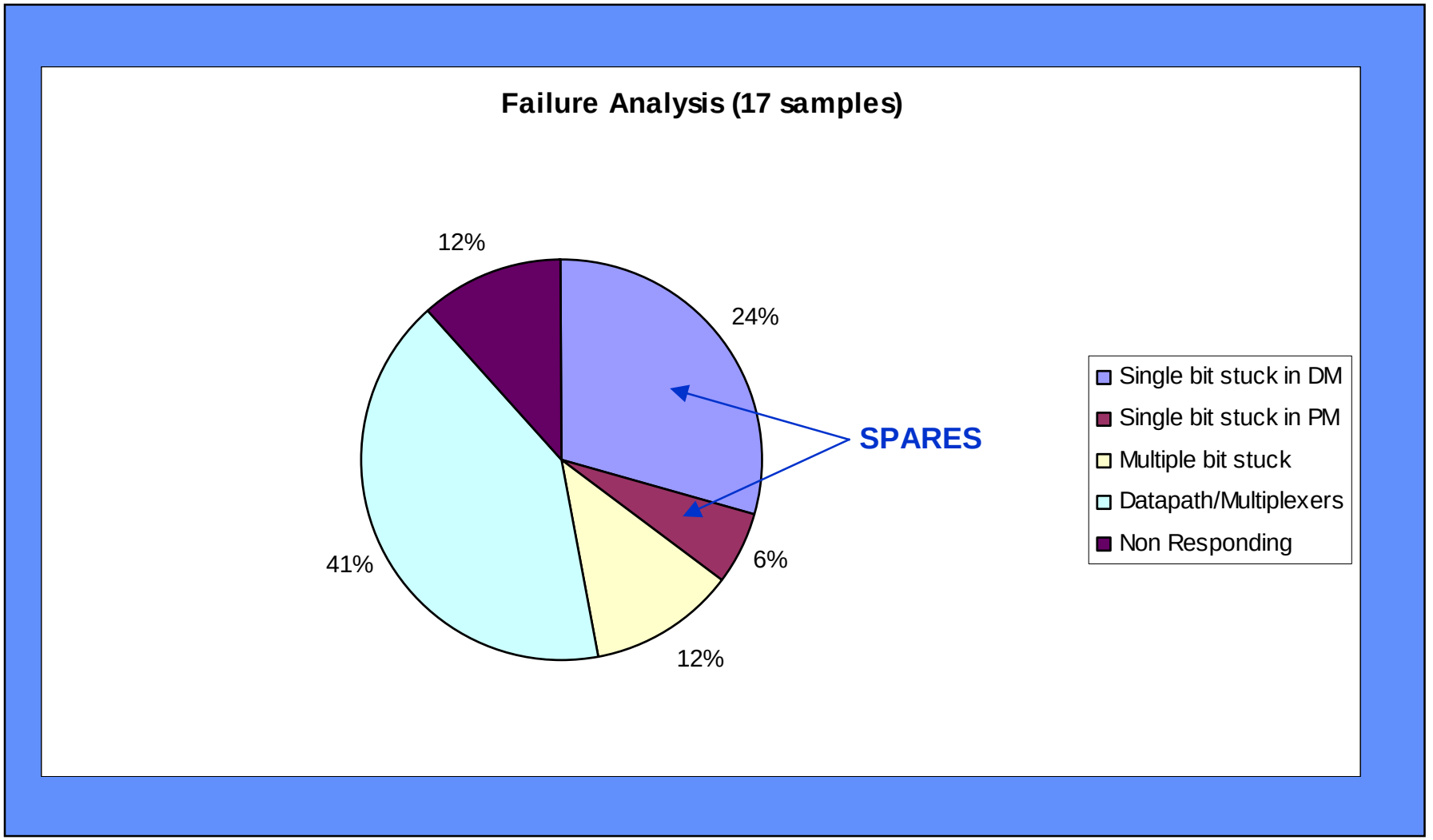
PRODUCTION YIELD (MPW)



Recoverable chips correspond to single and double bit stuck in the Memories

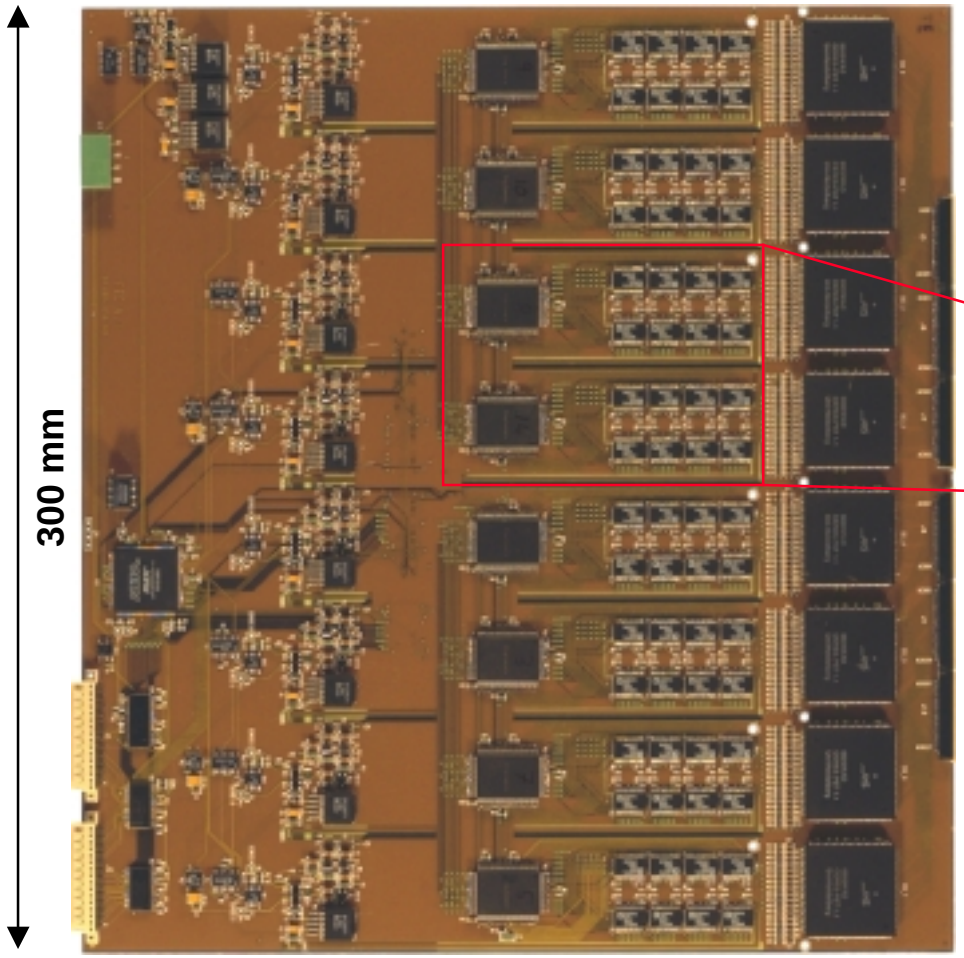
The specific location of single bit stuck can be known, and the error can be corrected while de-formatting the data packet.

PRODUCTION YIELD (MPW)

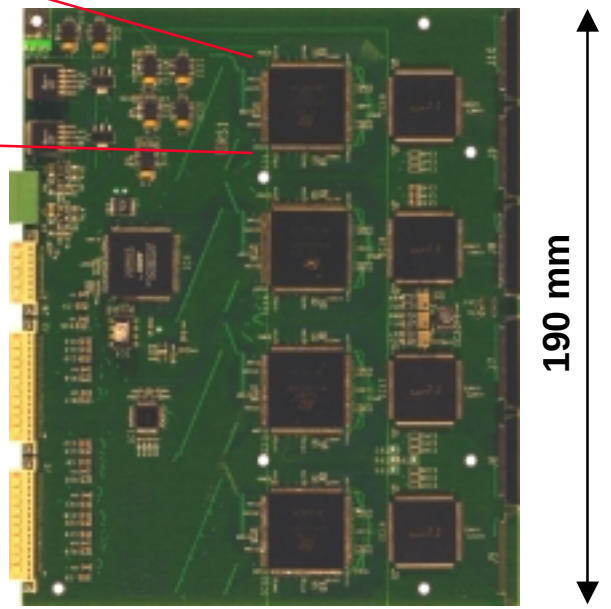


FRONT END CARD

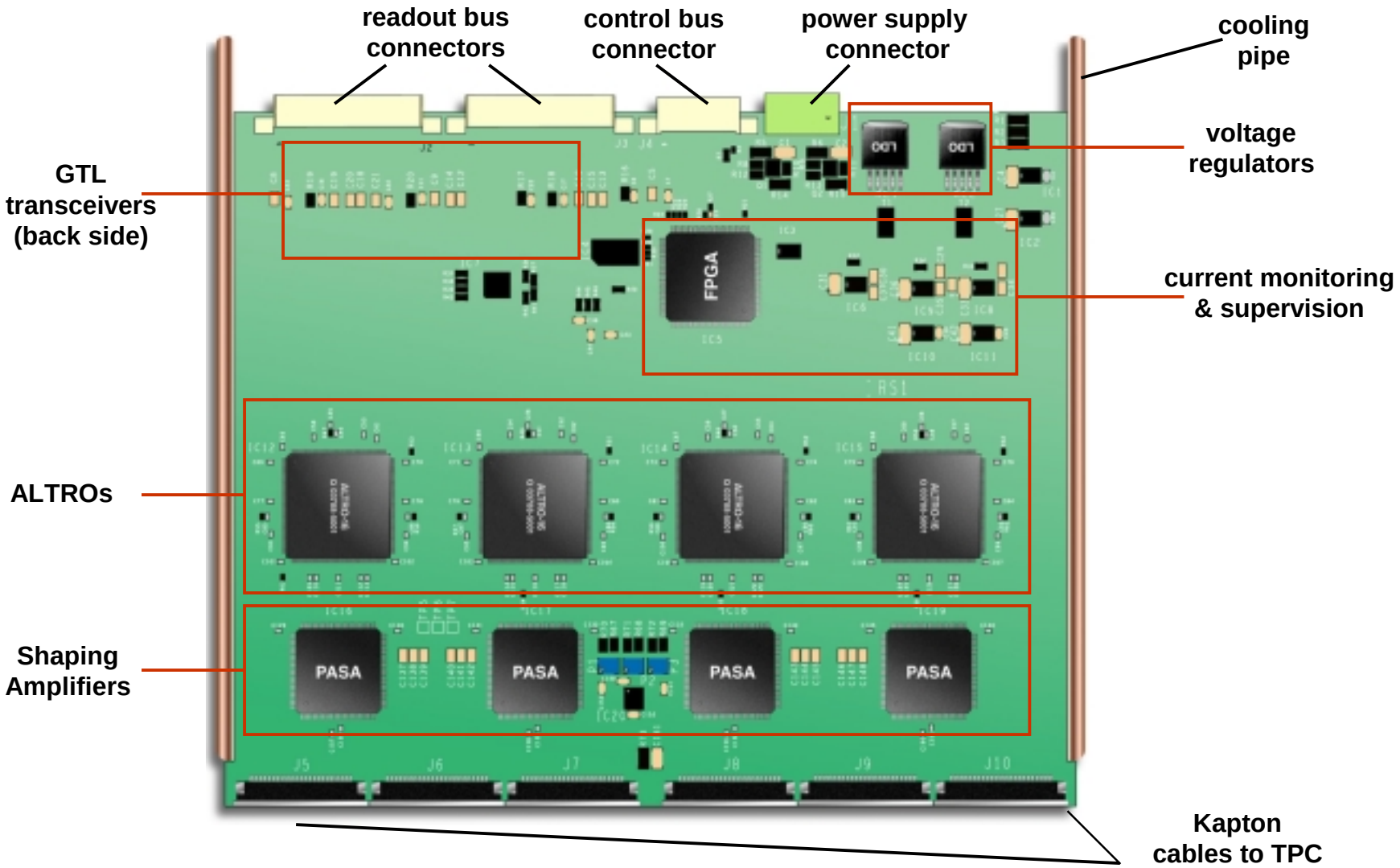
FIRST PROTOTYPE



NEW DESIGN

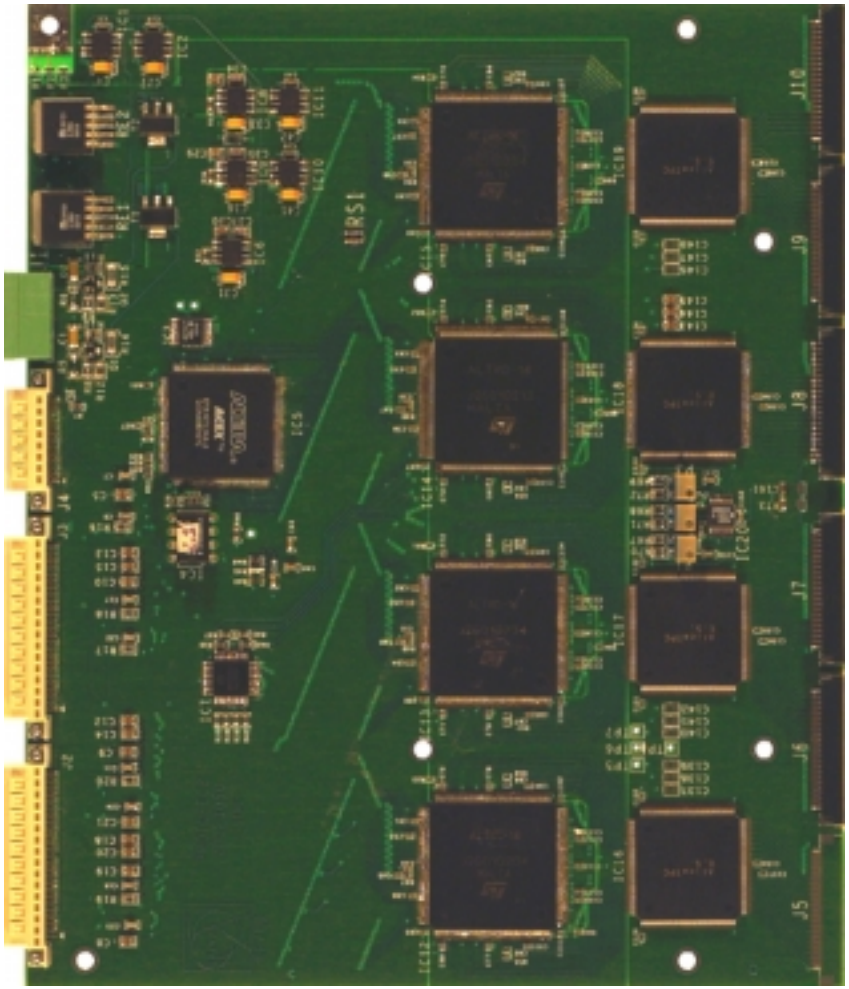


FRONT END CARD ARCHITECTURE
(128 CHANNELS)

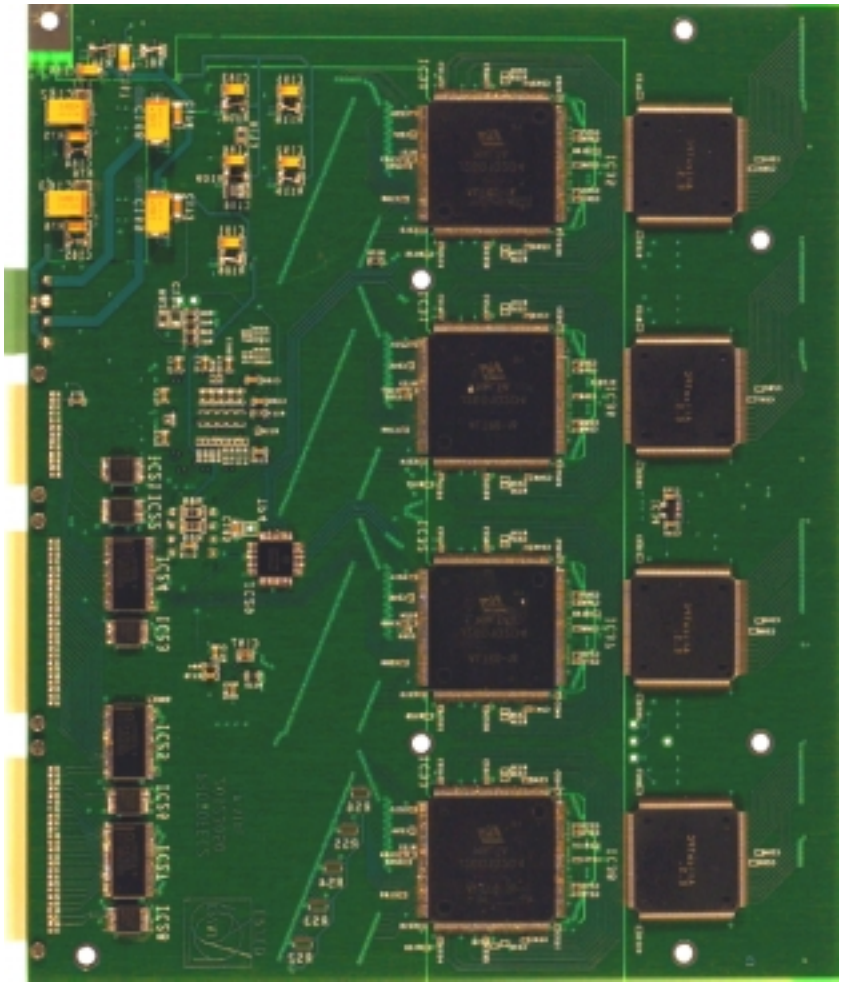


FRONT END CARD LAYOUT

TOP SIDE

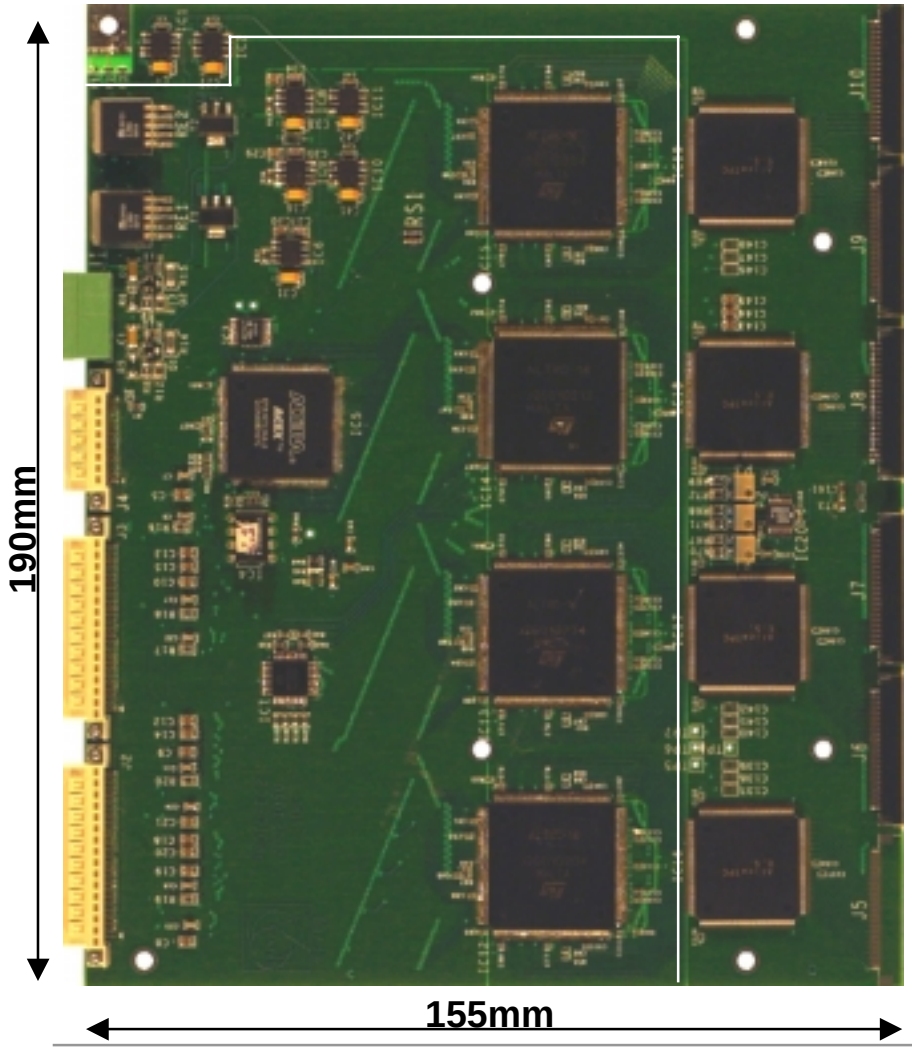


BOTTOM SIDE

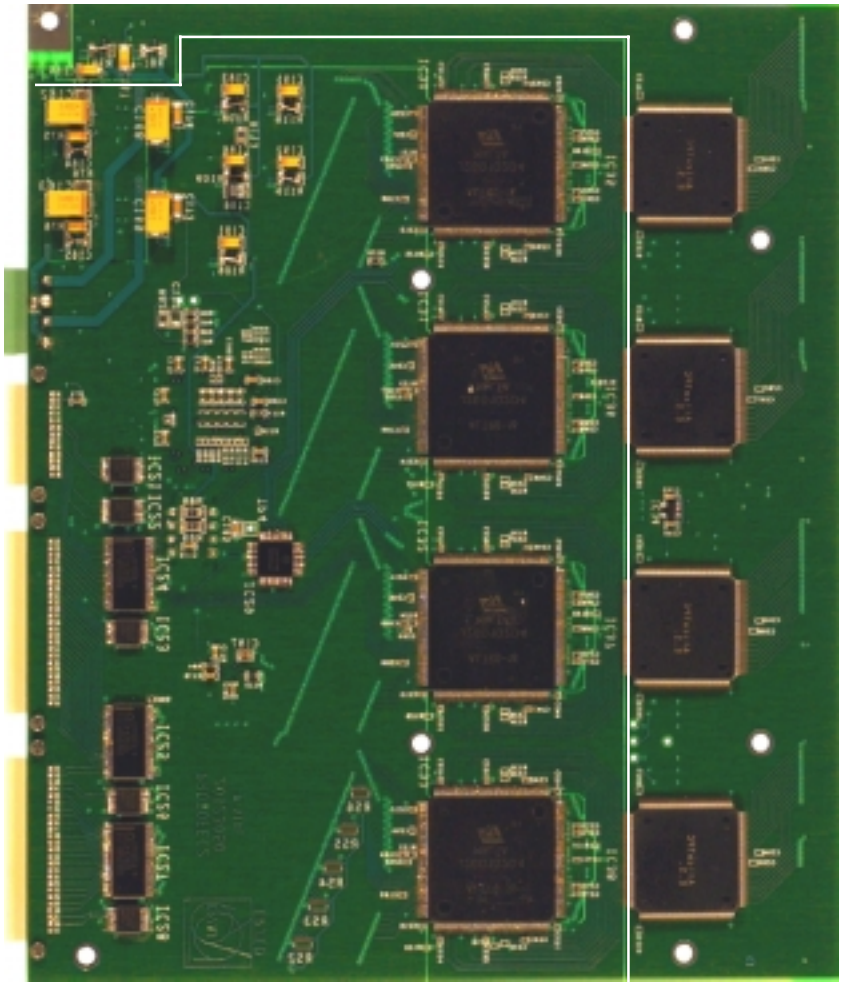


FRONT END CARD LAYOUT

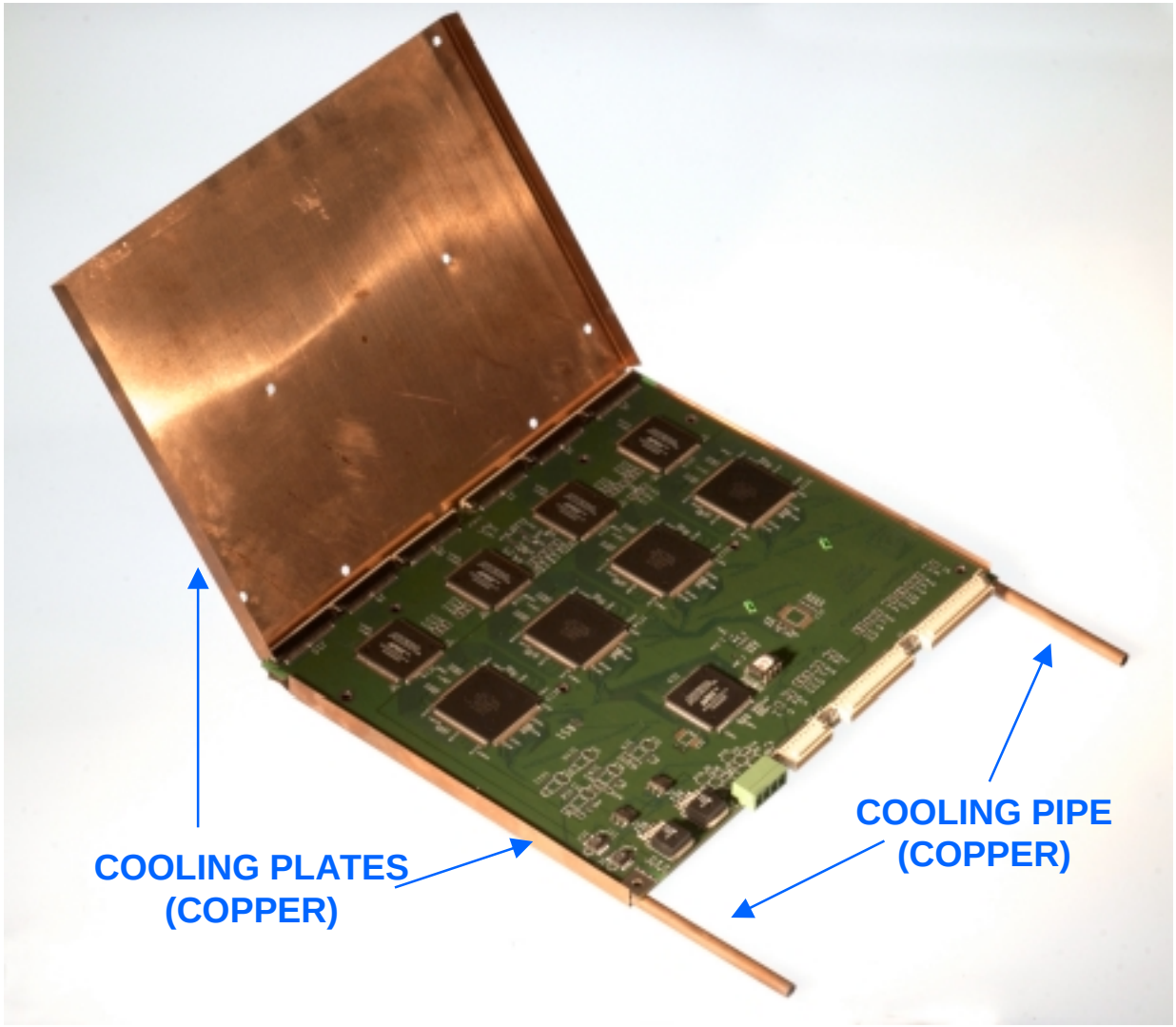
TOP SIDE



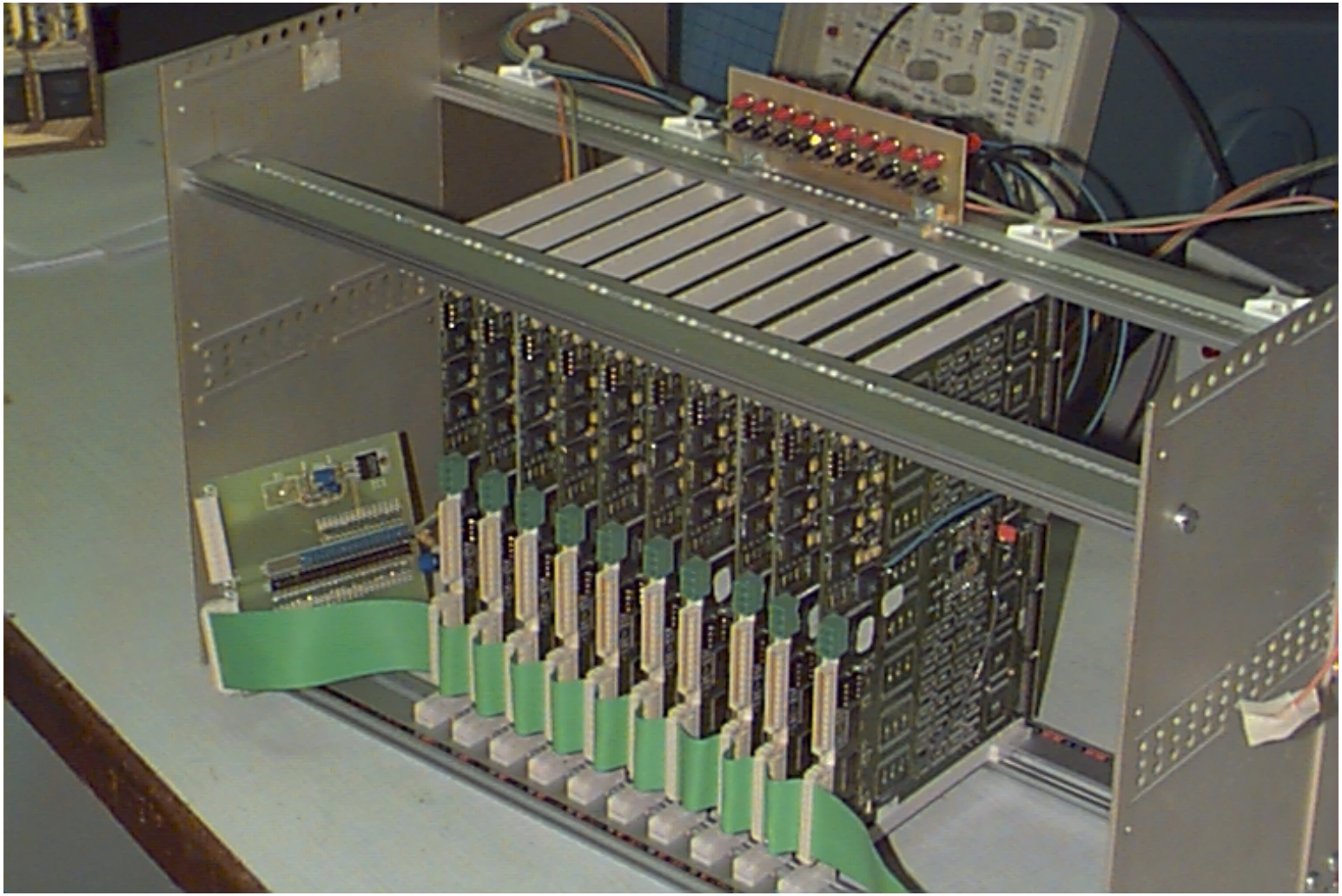
BOTTOM SIDE



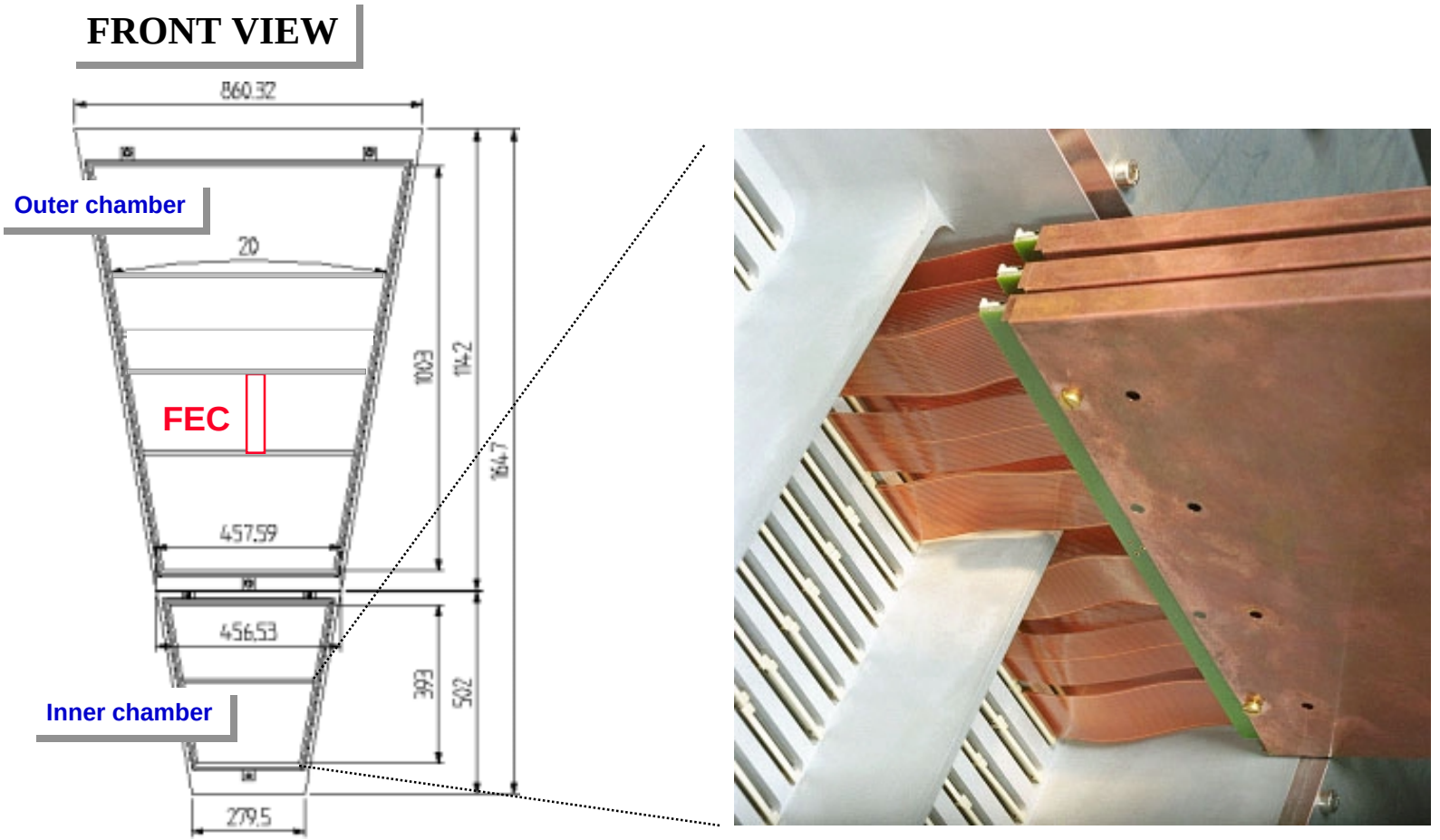
FRONT END CARD COOLING



FEC READOUT BUS



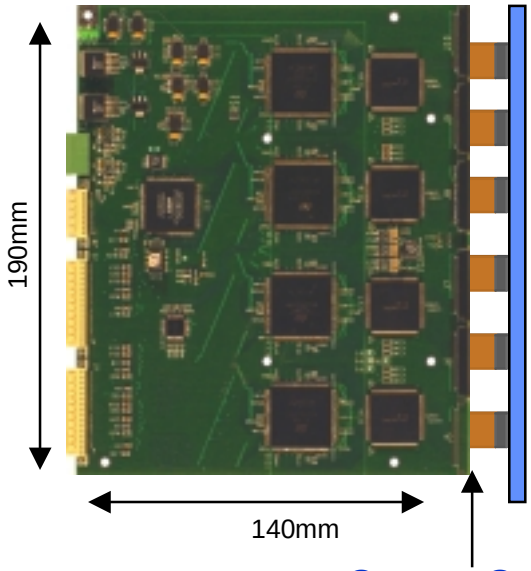
INTEGRATION IN THE READOUT CHAMBER



MOUNTING

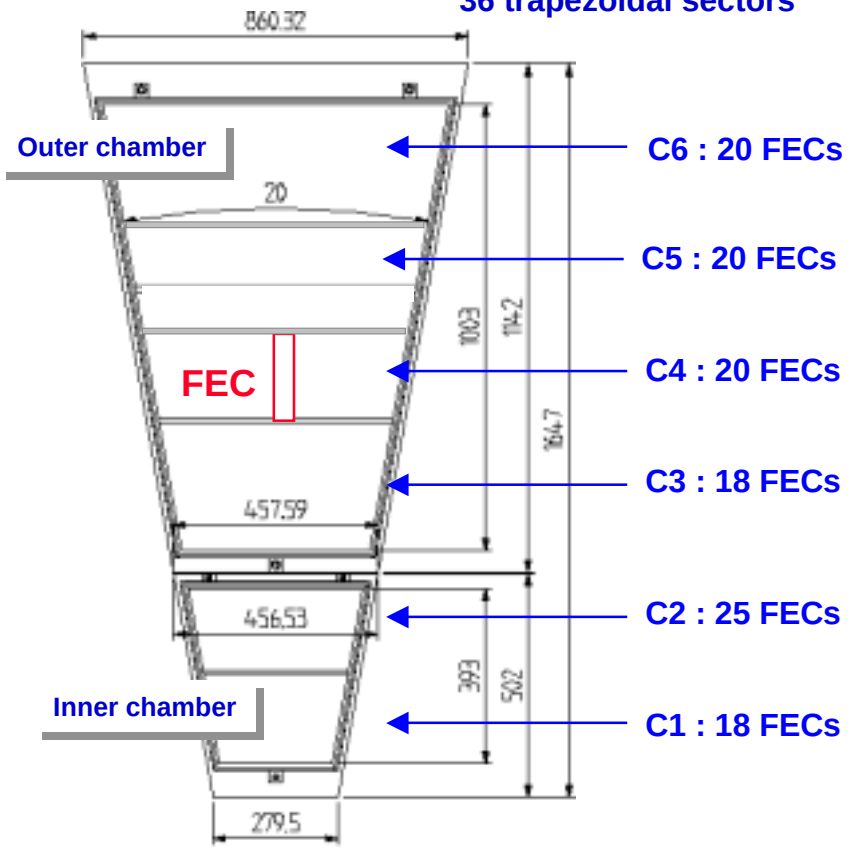
SIDE VIEW

128 channels
Front End Card (FEC)



FRONT VIEW

36 trapezoidal sectors



FEE POWER:

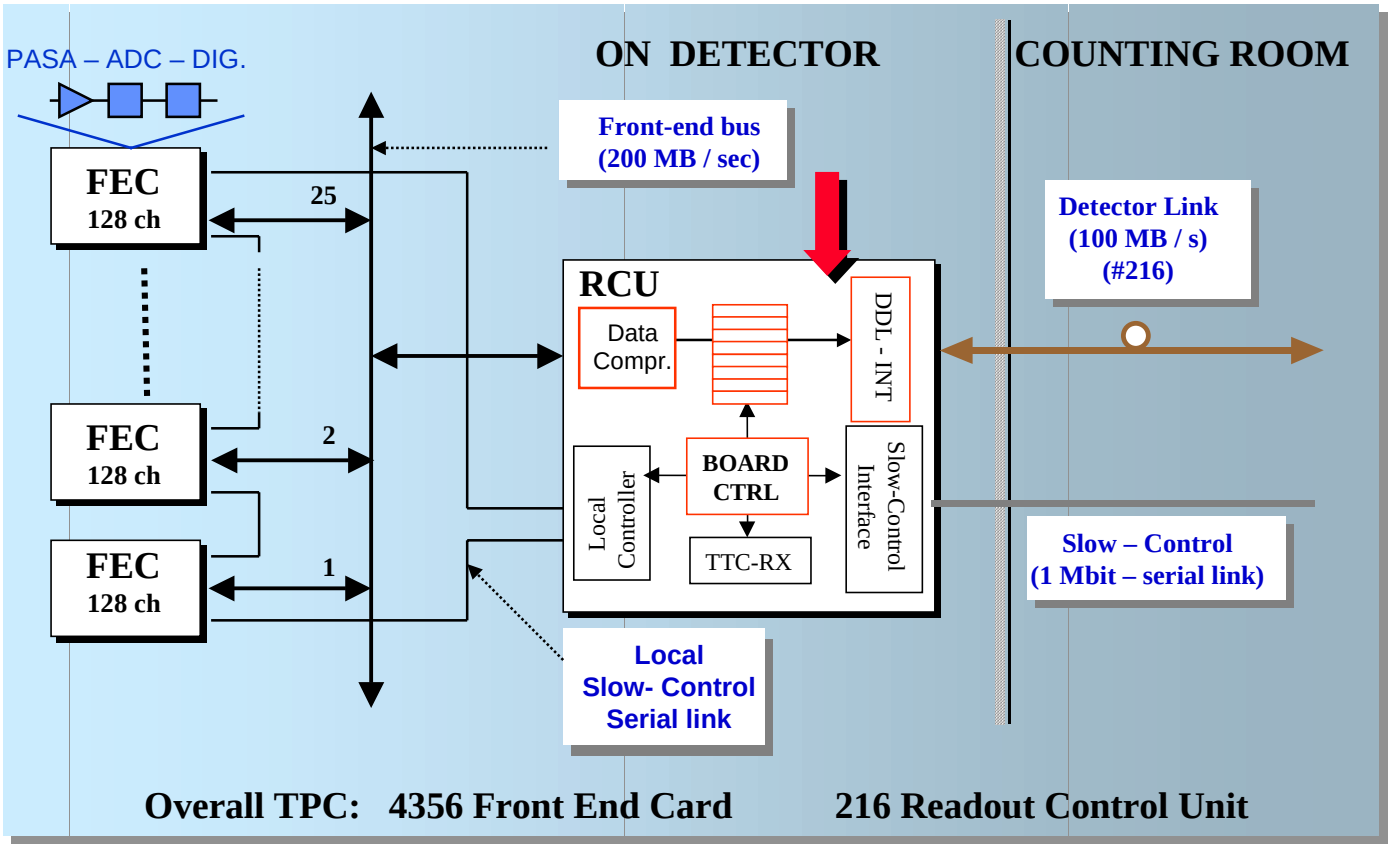
- **CHANNEL:** 40 mW
- **BOARD:** 6.9 W
- **SECTOR:** 832 W
- **TOTAL:** 30.2 KW

FRONT END CARD MILESTONES

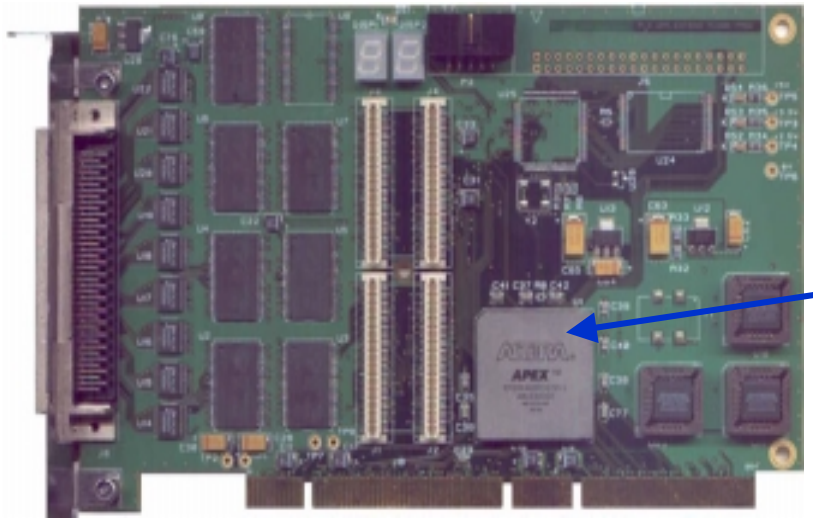
- Pre-series production of 30 FEC (60% of one IROC) started
- Market survey for mass production concluded in June ‘02
- Radiation test of FEC Sept 02
- Start of mass production Jan 03
- End of production test Jan 04

GLOBAL ARCHITECTURE

Each TPC Sector is served by 6 Readout Subsystems



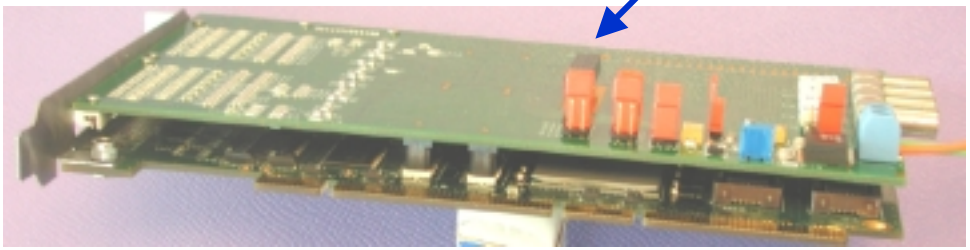
READOUT CONTROL UNIT
FIRST PROTOTYPE

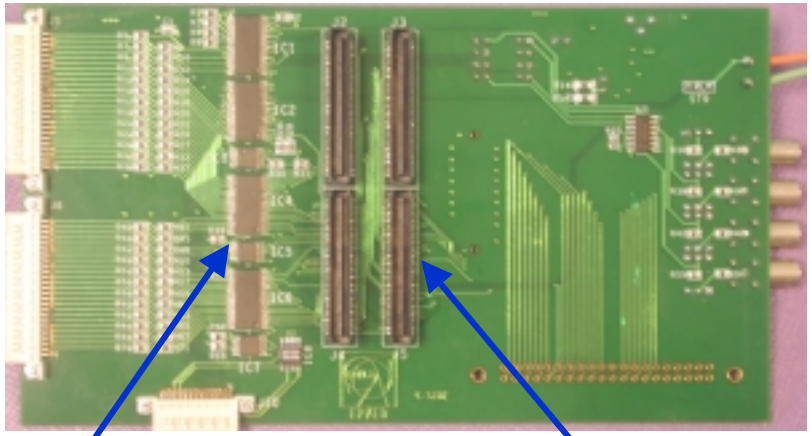


PCI CARD (PLDa)

FPGA with PCI-core

DDL-SIU CONNECTOR





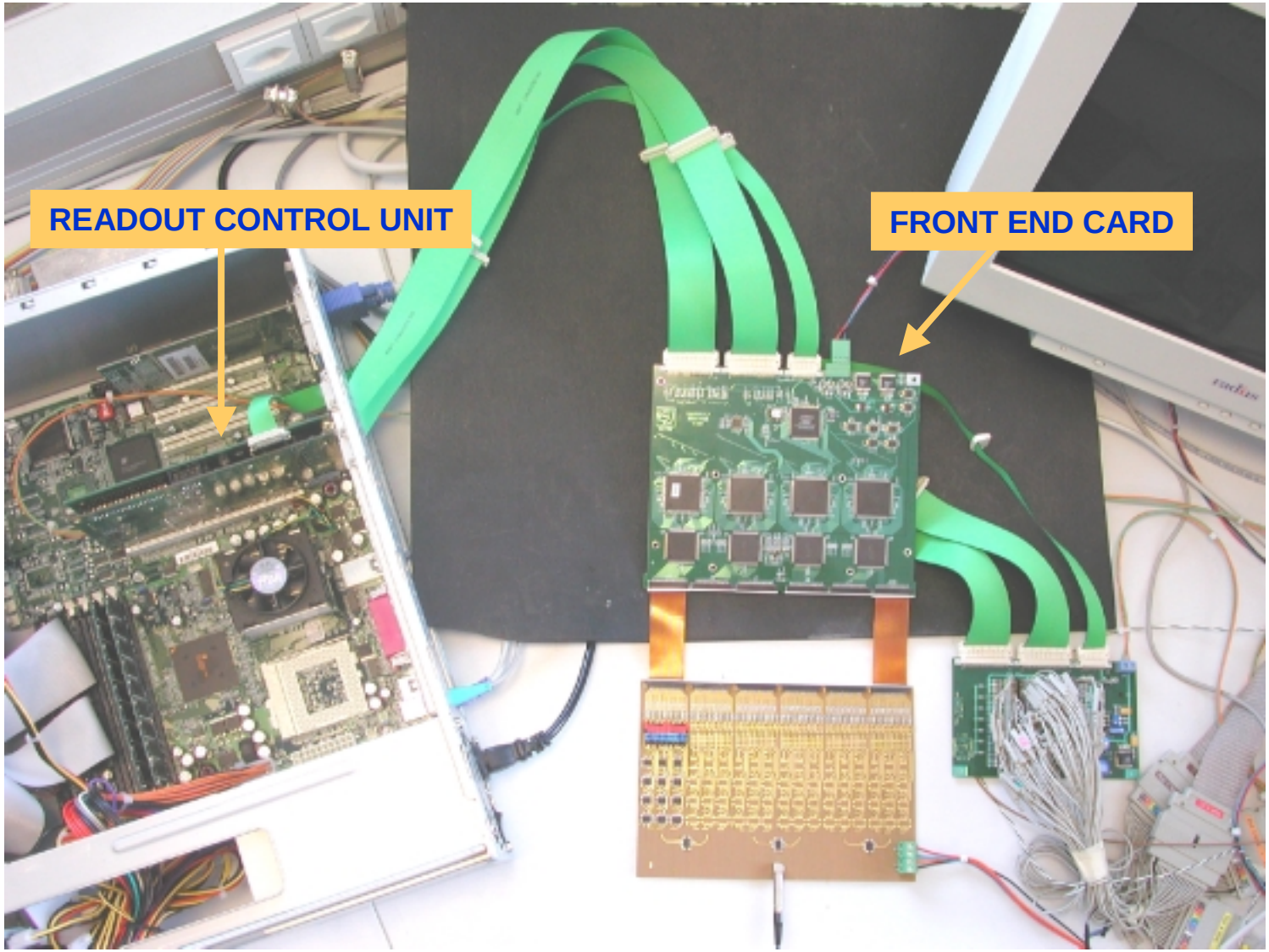
LEMO CONNECTOR
(L1, L2, RDOCLK, ADCCLK)

PMC CARD

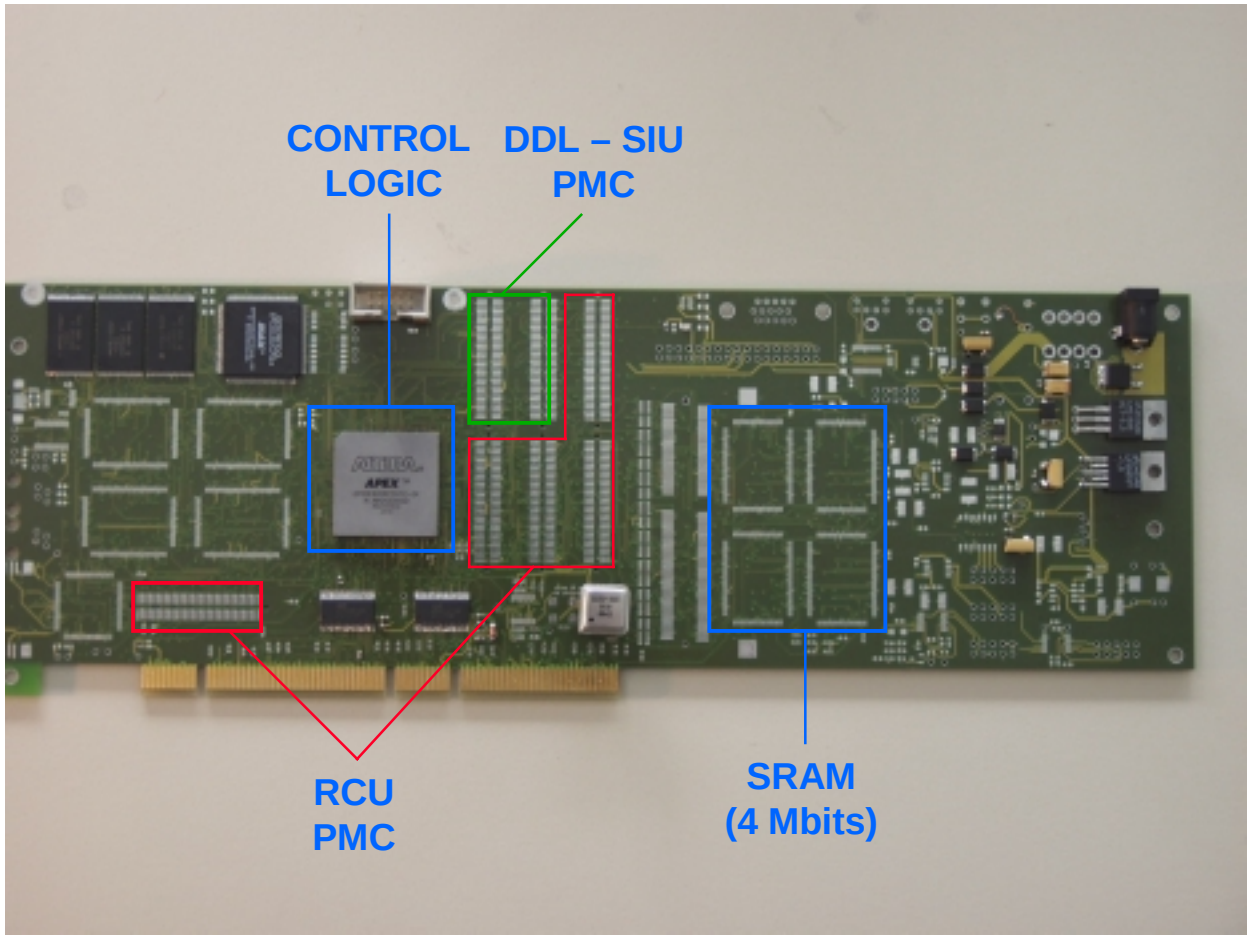
GTL Transceivers

PMC connectors

FRONT END CARD + READOUT CONTROL UNIT



READOUT CONTROL UNIT
SECOND PROTOTYPE



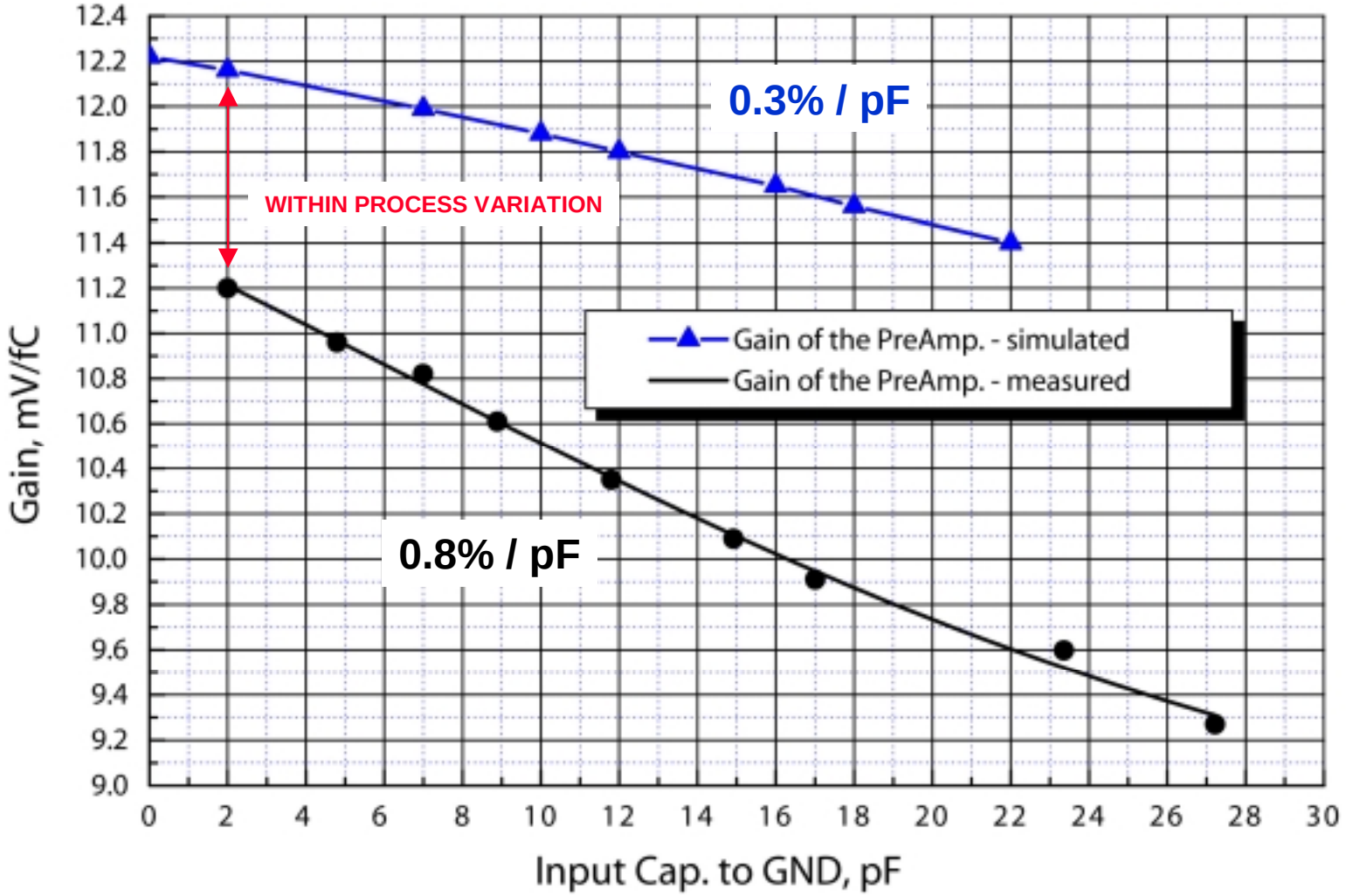
SUMMARY

- **The TPC FEE consists of 4 basic components:**
  - PASA (40 000 chips)
  - ALTRO (40 000 chips)
  - FEC (4500 boards)
  - RCU (220 boards)

- **Production:**
  - ALTRO: Apr ‘02
  - PASA: Nov ’02
  - FEC: Jan ’03

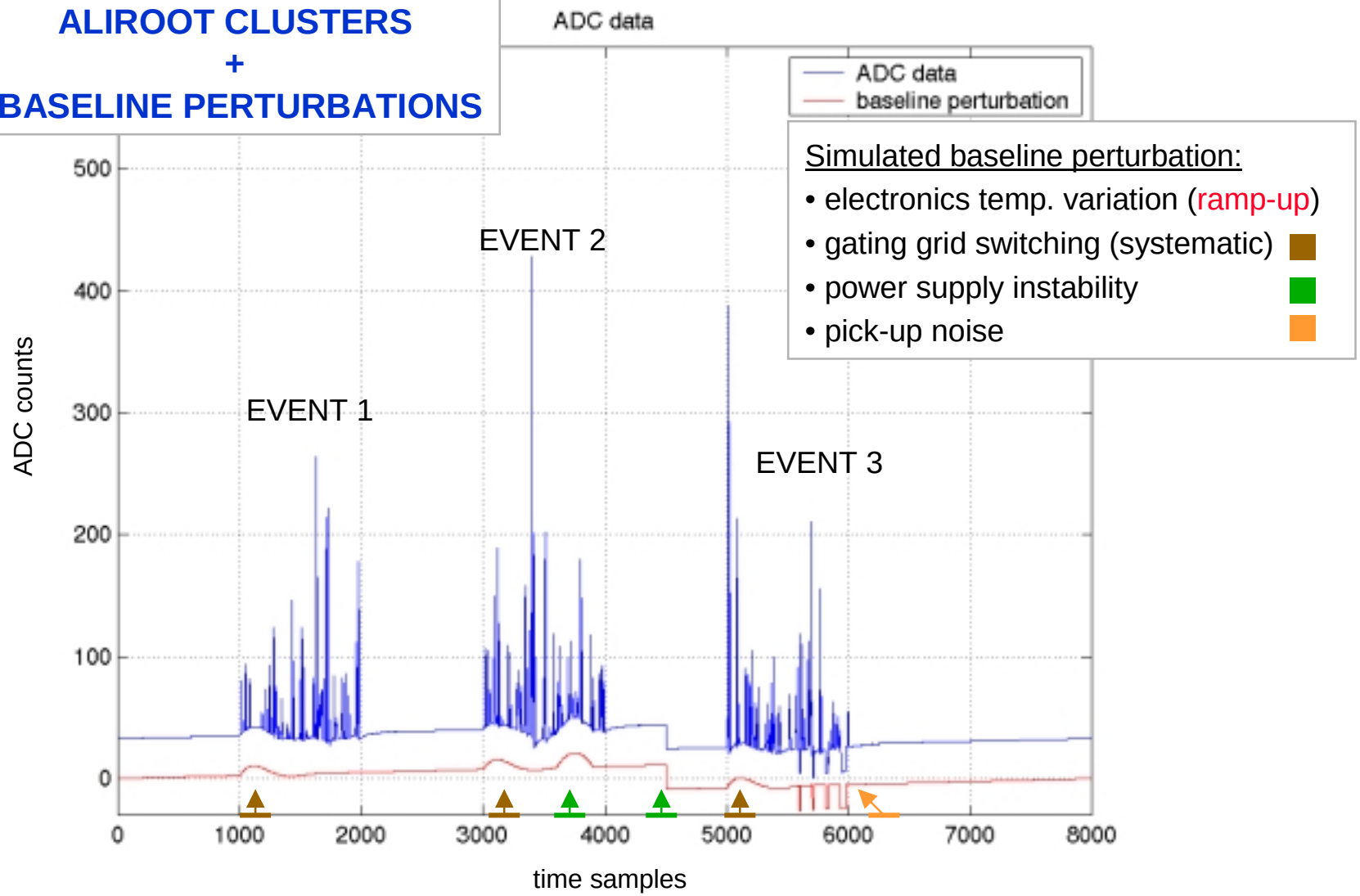
- **A significant fraction of the complete electronics (5.000 channels) connected to the IROC will be tested during Summer ‘02**

CONVERSION GAIN



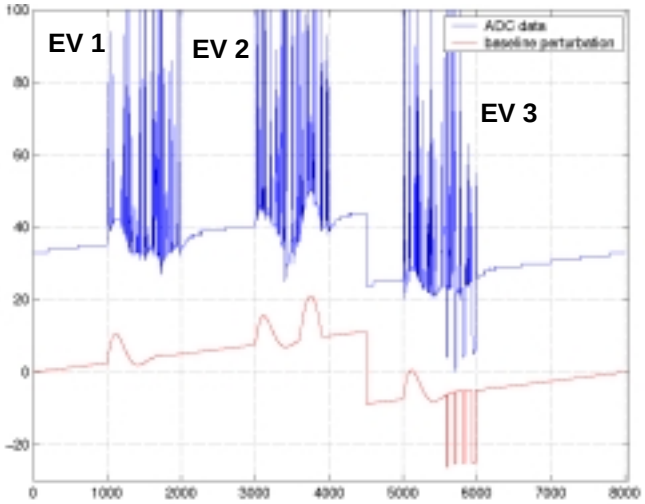
FRONT-END SIGNAL PROCESSING

ALIROOT CLUSTERS
+
BASELINE PERTURBATIONS

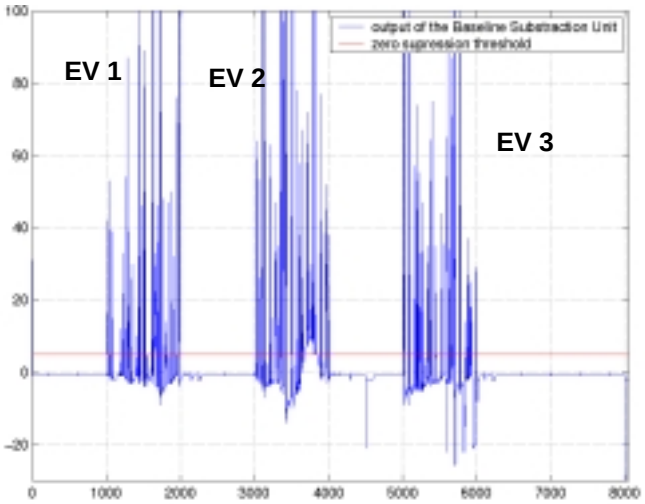


FRONT-END SIGNAL PROCESSING

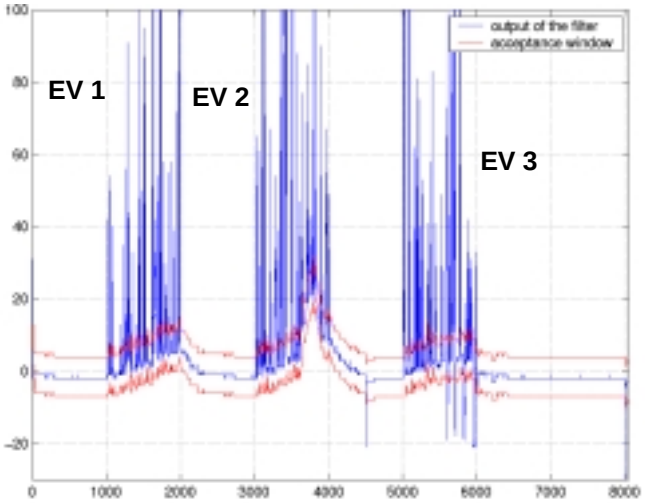
INPUT SIGNAL



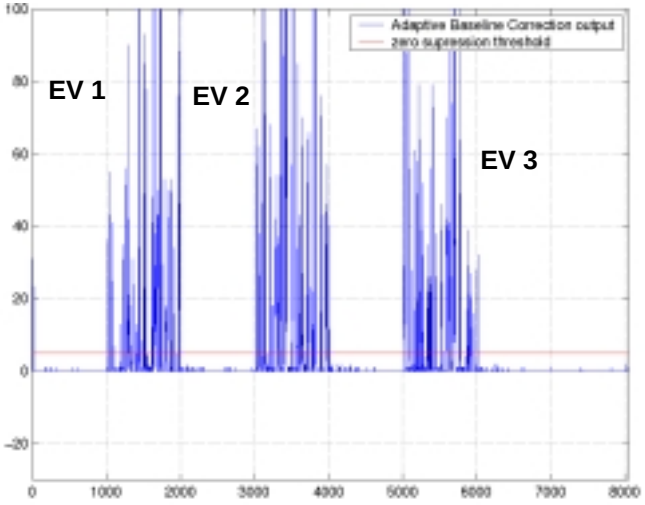
AFTER 1st BASELINE CORRECTION



AFTER TAIL CANCELLATION

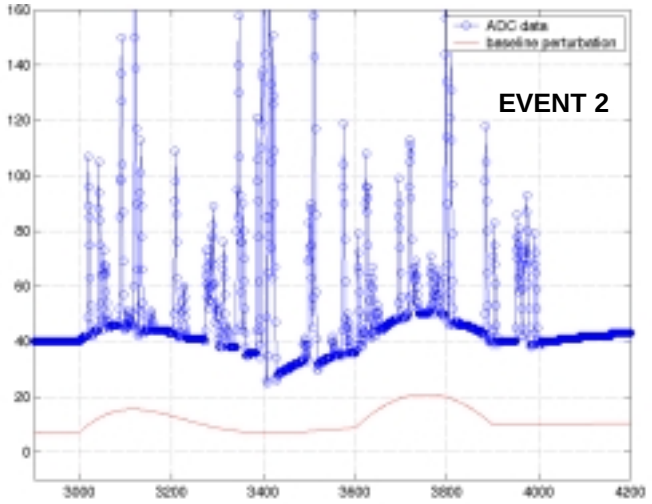


AFTER 2nd BASELINE CORRECTION

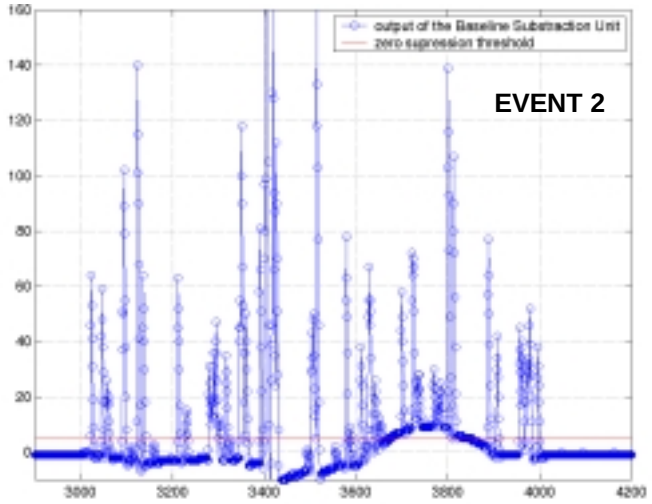


FRONT-END SIGNAL PROCESSING

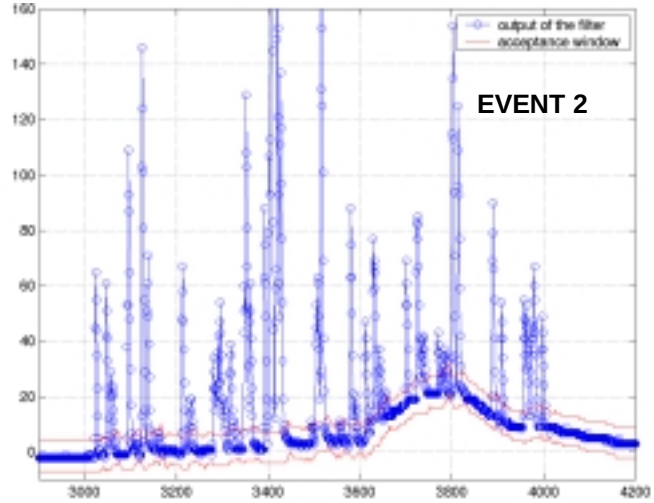
INPUT SIGNAL



AFTER 1st BASELINE CORRECTION



AFTER TAIL CANCELLATION



AFTER 2nd BASELINE CORRECTION