RCU Characterization

Bergen, 7th April 2005

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- New hardware prototype
- Generation of the Sampling Clock
- DCS Interface
- Clock Signals
- SIU Interface
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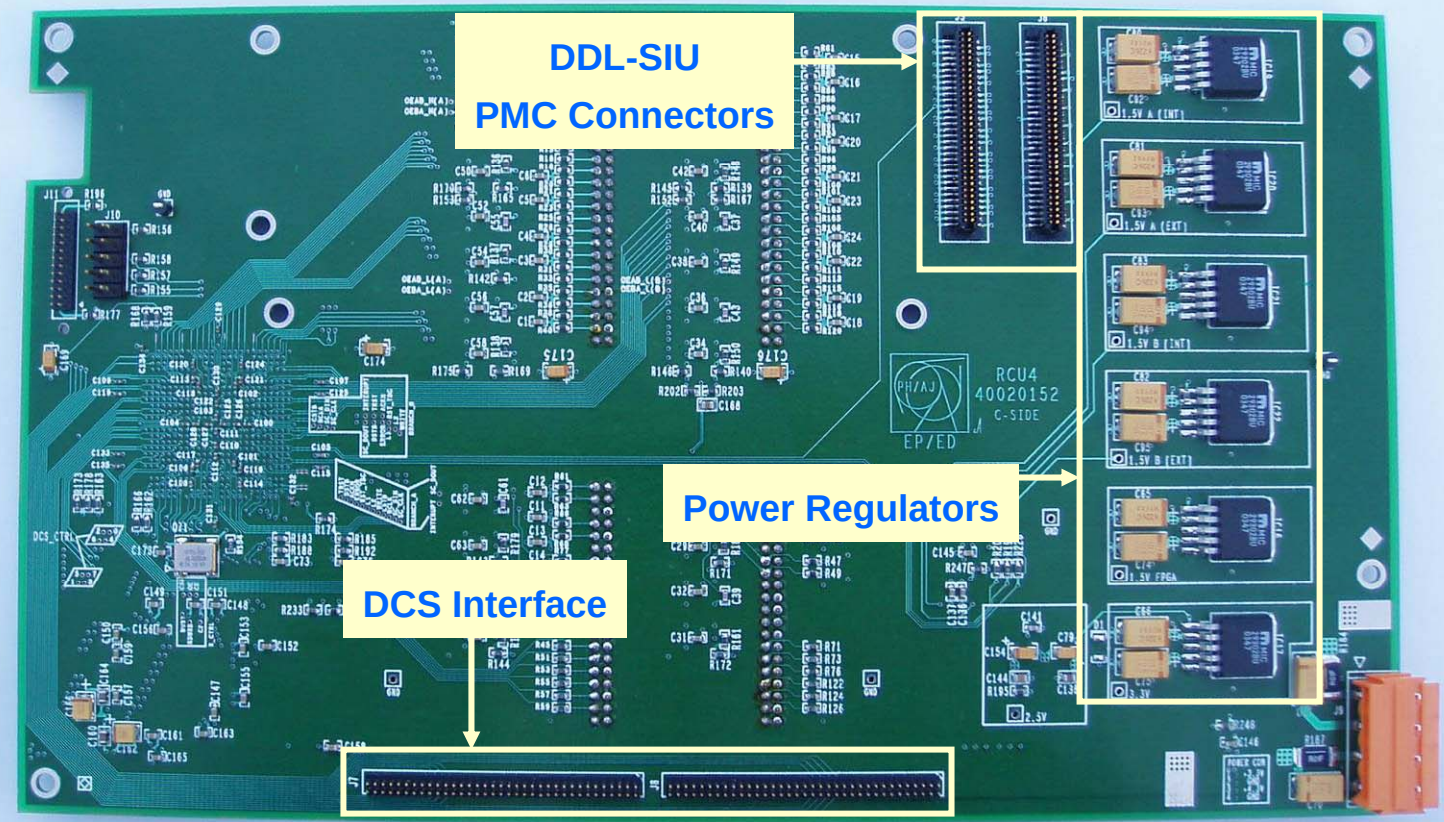
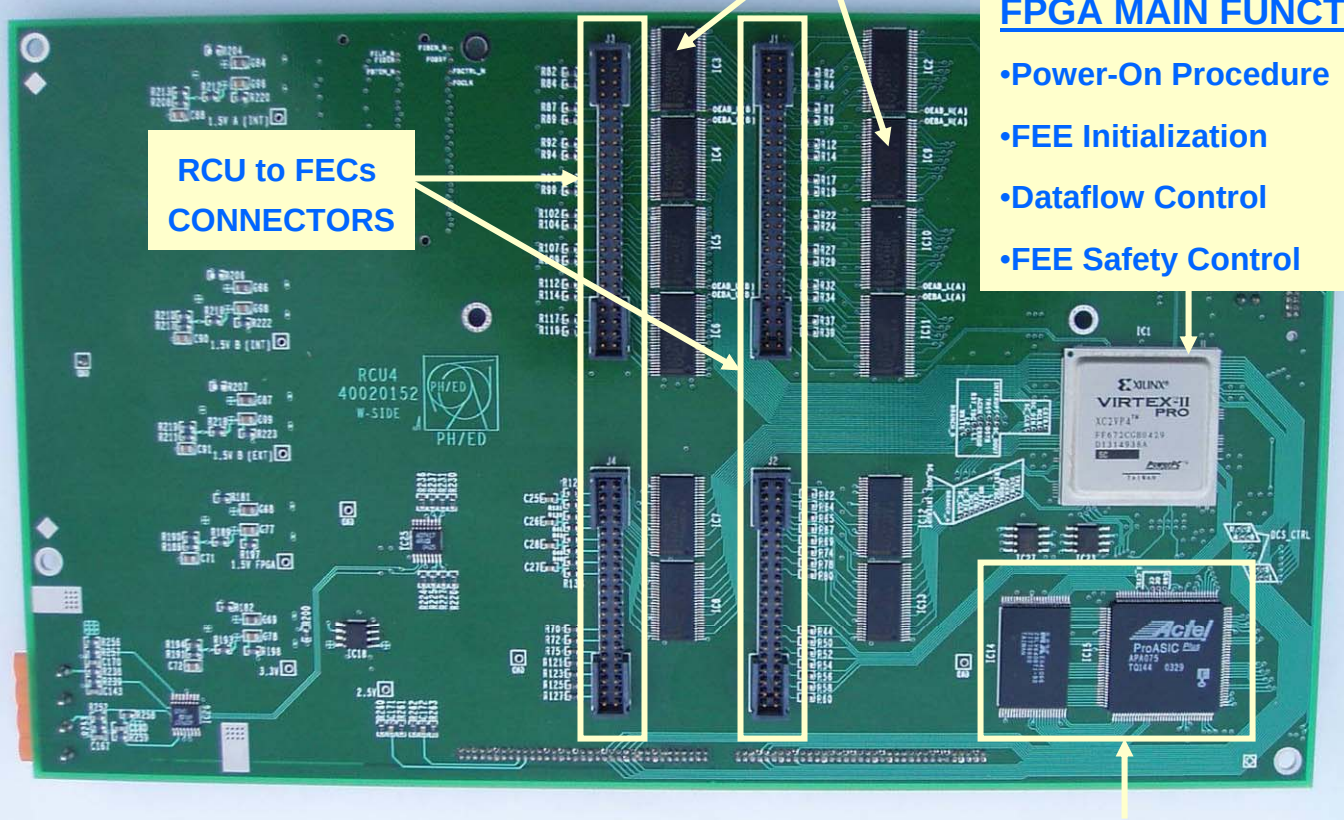
New Hardware Prototype

TOP SIDE

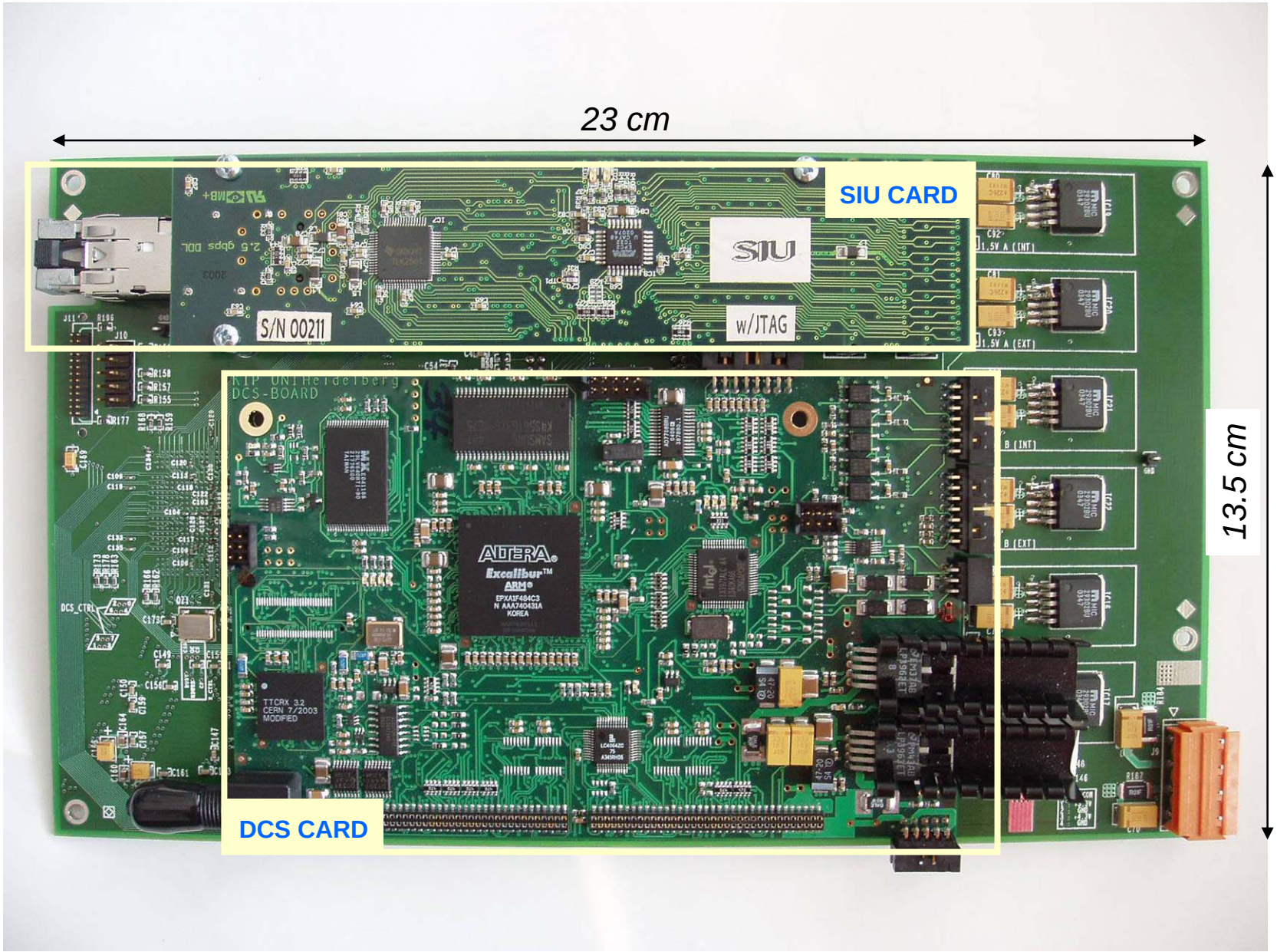


New Hardware Prototype

BOTTOM SIDE



New Hardware Prototype



Generation of the Sampling Clock

Problem: How to insure synchronism of SCLK on all 216 RCUs? (At the level of 1 TTC clock cycle)

- By PLL in RCU FPGA using as input the TTC clock?

<< … It is as I suspected. there is no elegant way of insuring phase synchronism … Most likely, you will end up building a conventional divider on each Board, using flip-flops … >>

Peter Alfke, Senior Designer @ Xilinx Corp.

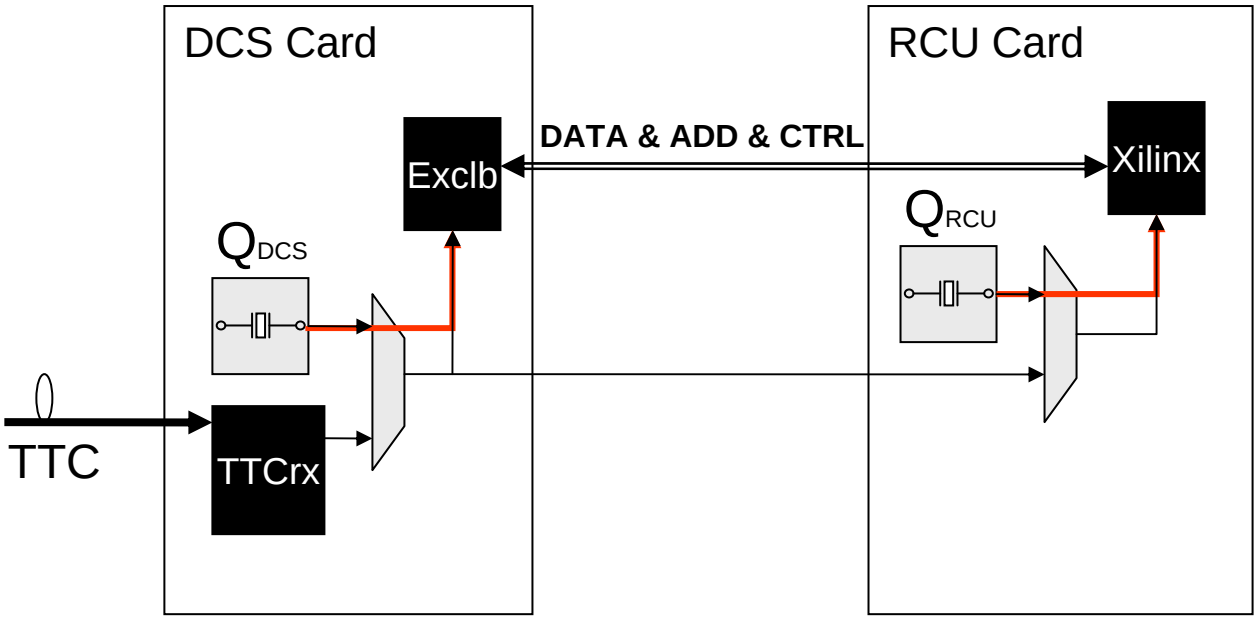
Due to indetermination in the “time to lock” of the PLL

=> Divider with global reset could be solution

DCS Interface

- Measurements @ DCS connector

Clocking scheme between RCU and DCS



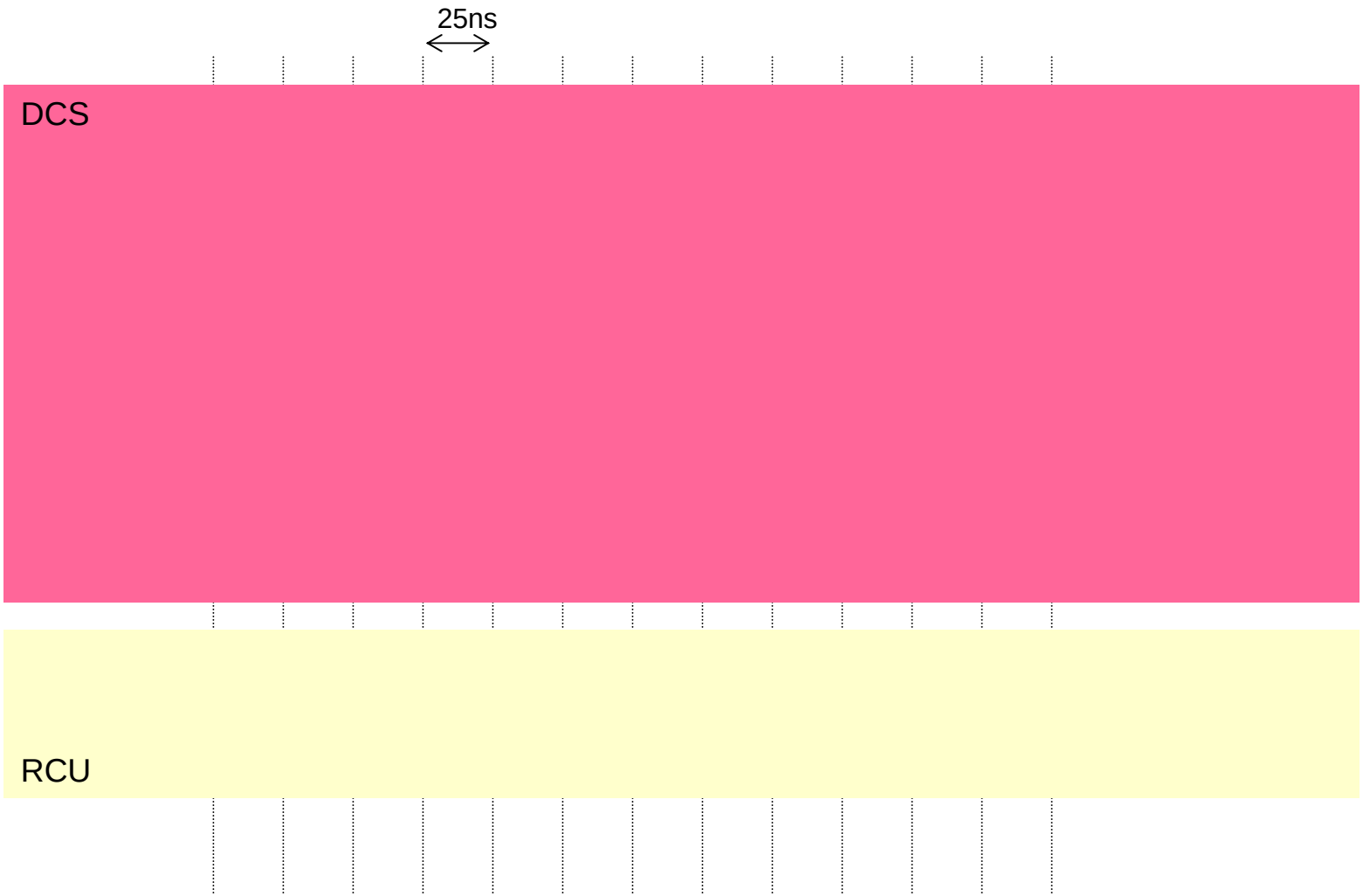
Clock scheme used in measurements

Asynchronous protocol with two different clock domains

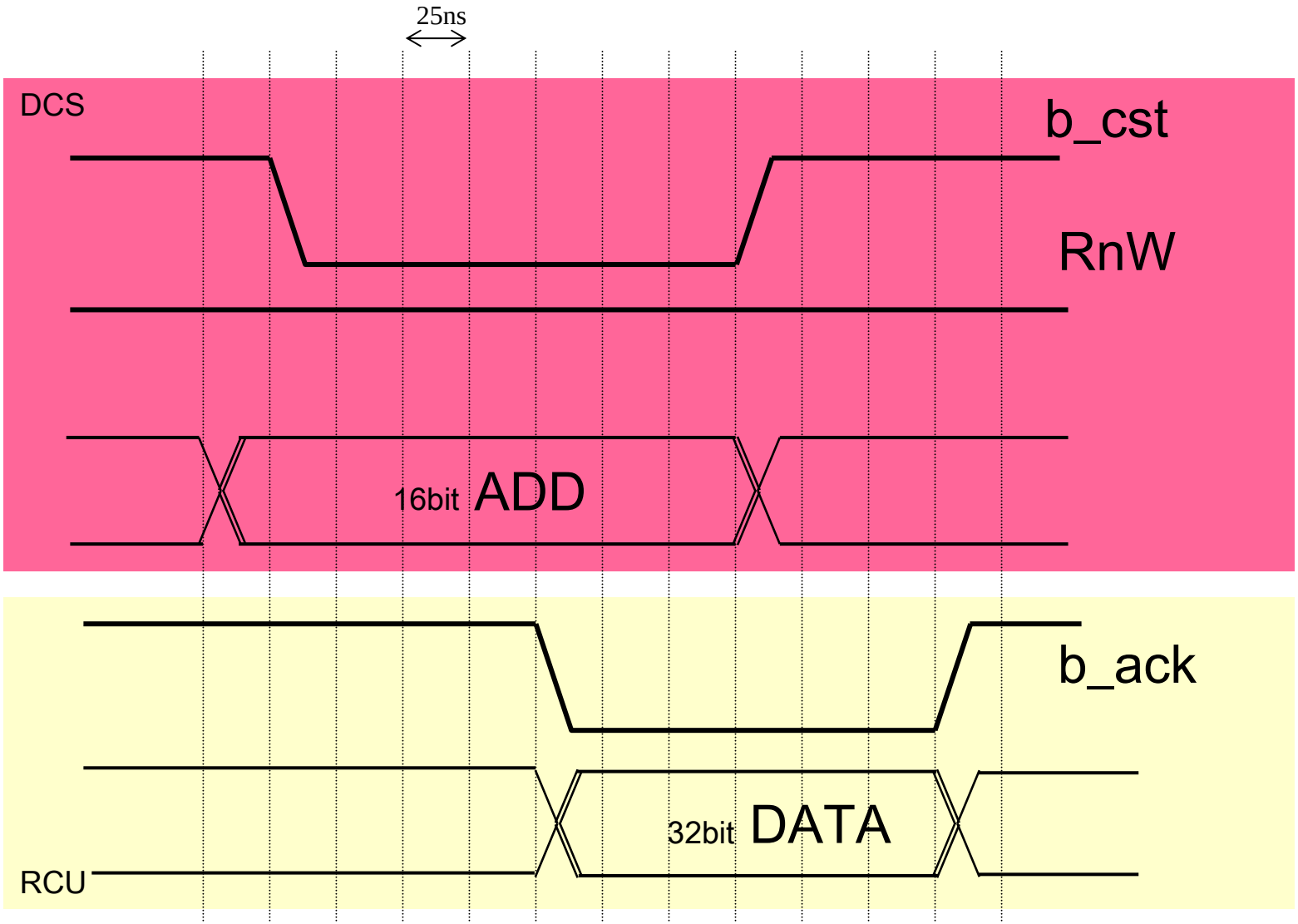
Requirements:

- Be able to work with RCU as stand-alone boards
- Eventually avoid 2 different clock domain when no TTC input is present?
- Automatic detection and selection of clock sources

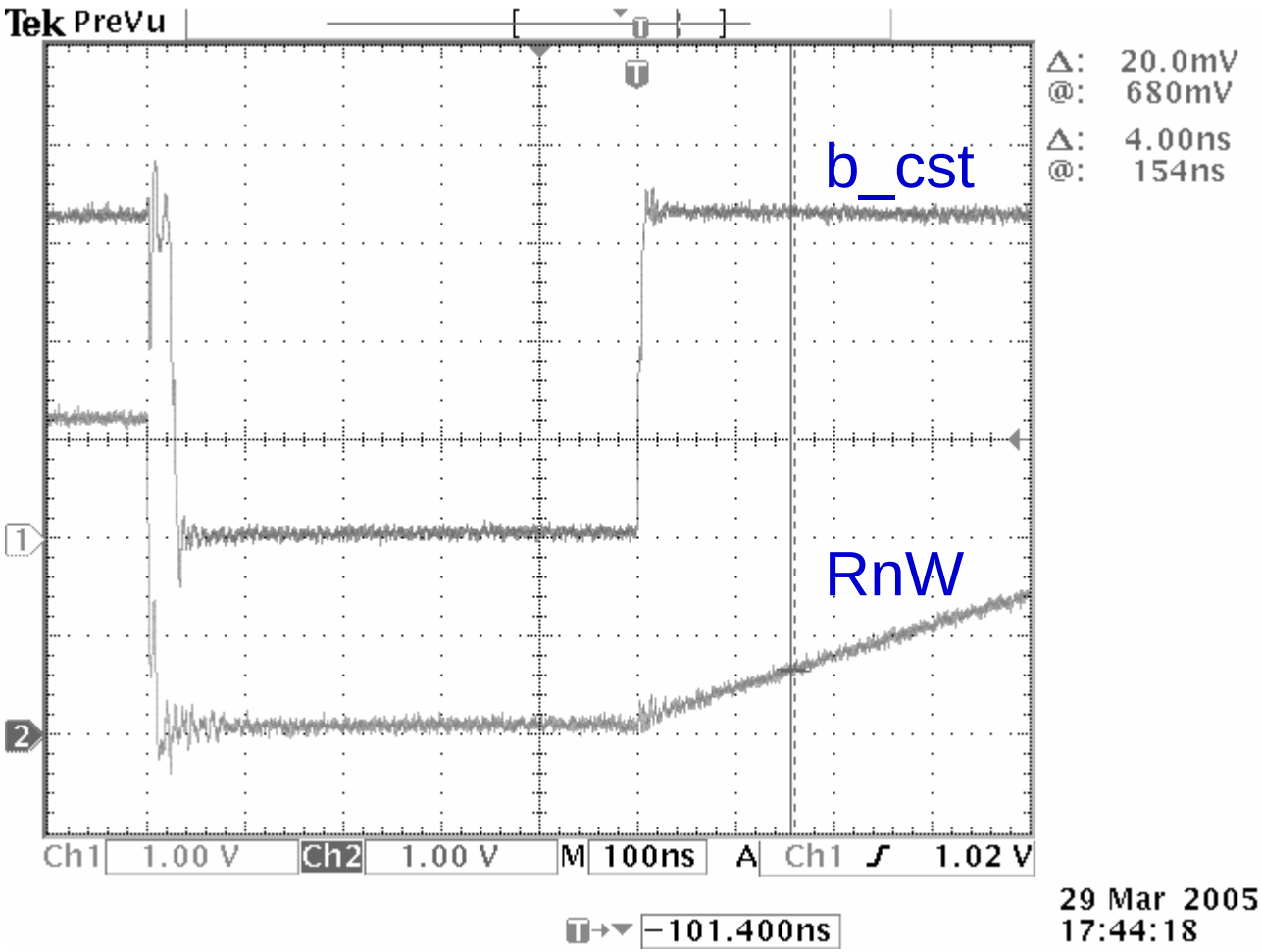
Current DCS-RCU interface protocol: Write cycle



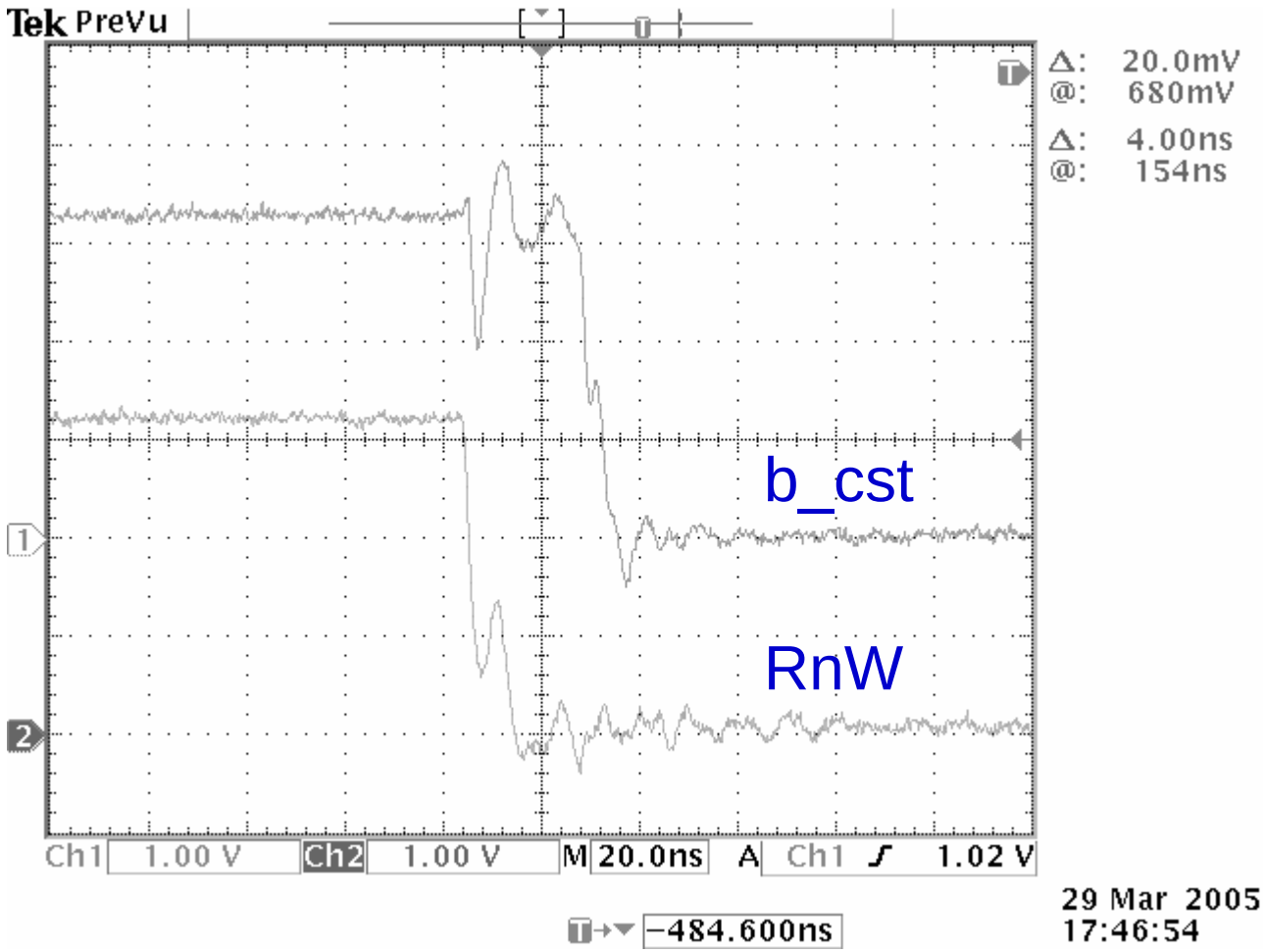
Current DCS-RCU interface protocol: Read cycle



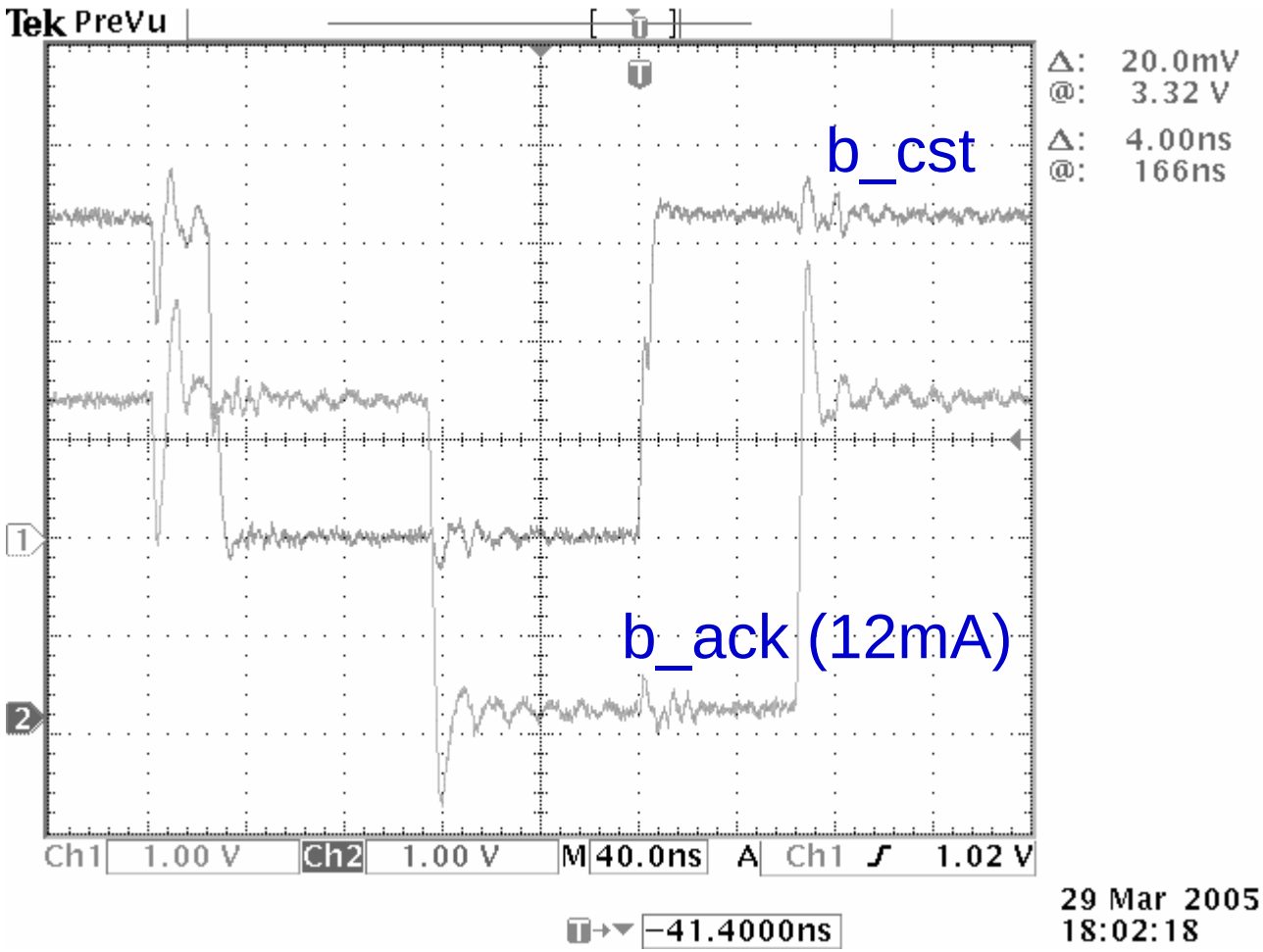
Control lines driven by the DCS card



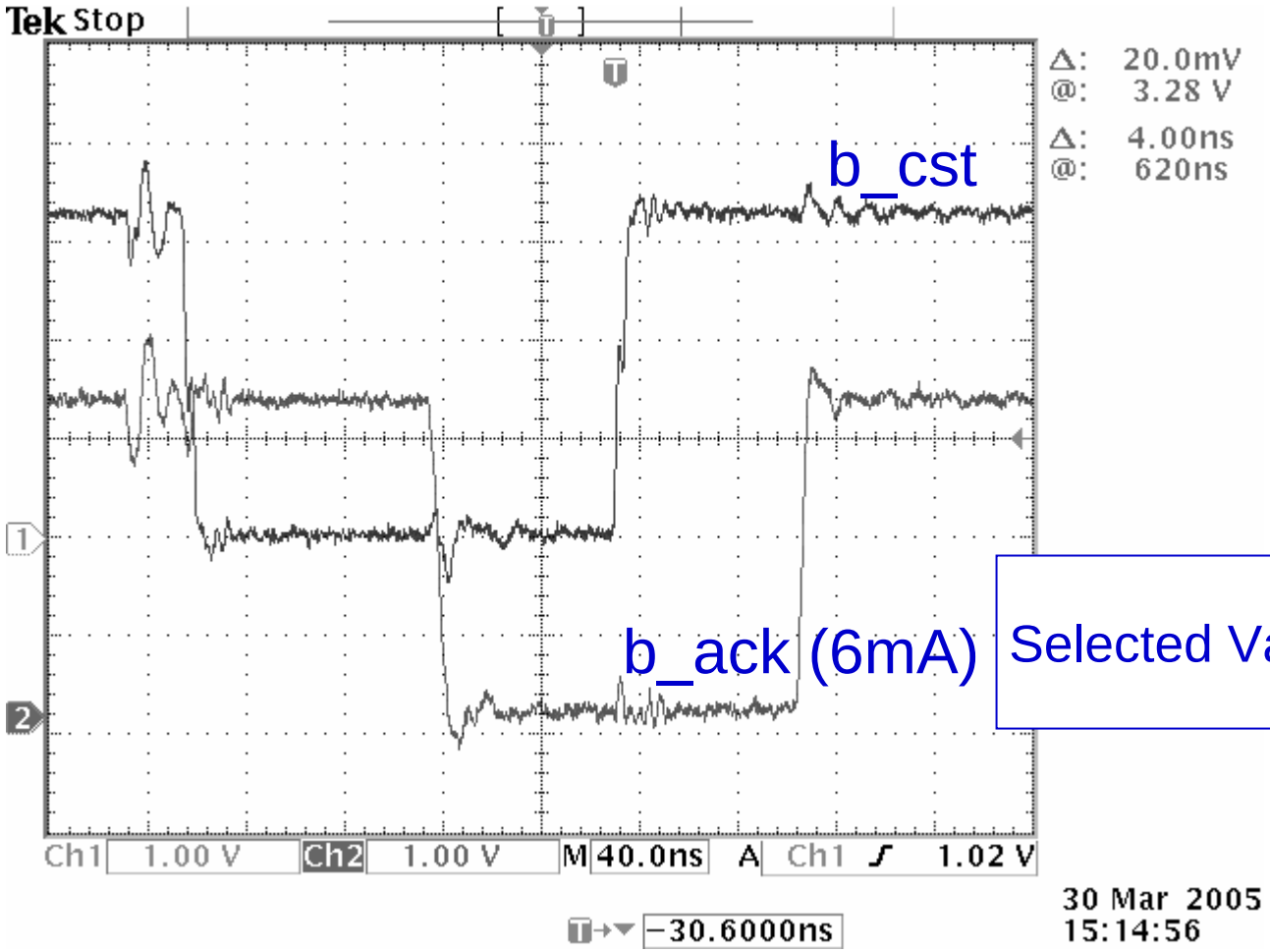
Control lines driven by the DCS card



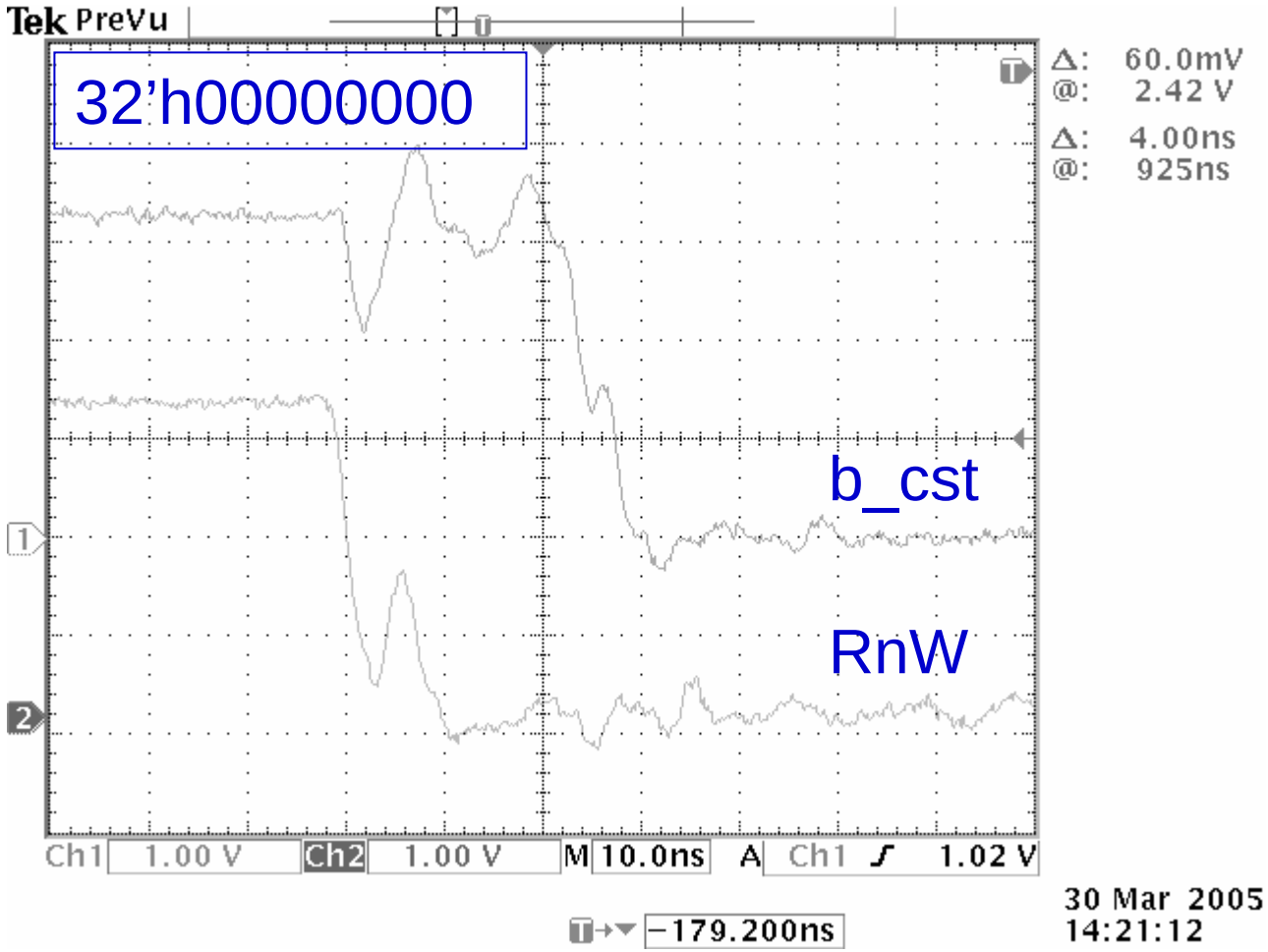
Control lines driven by the DCS card



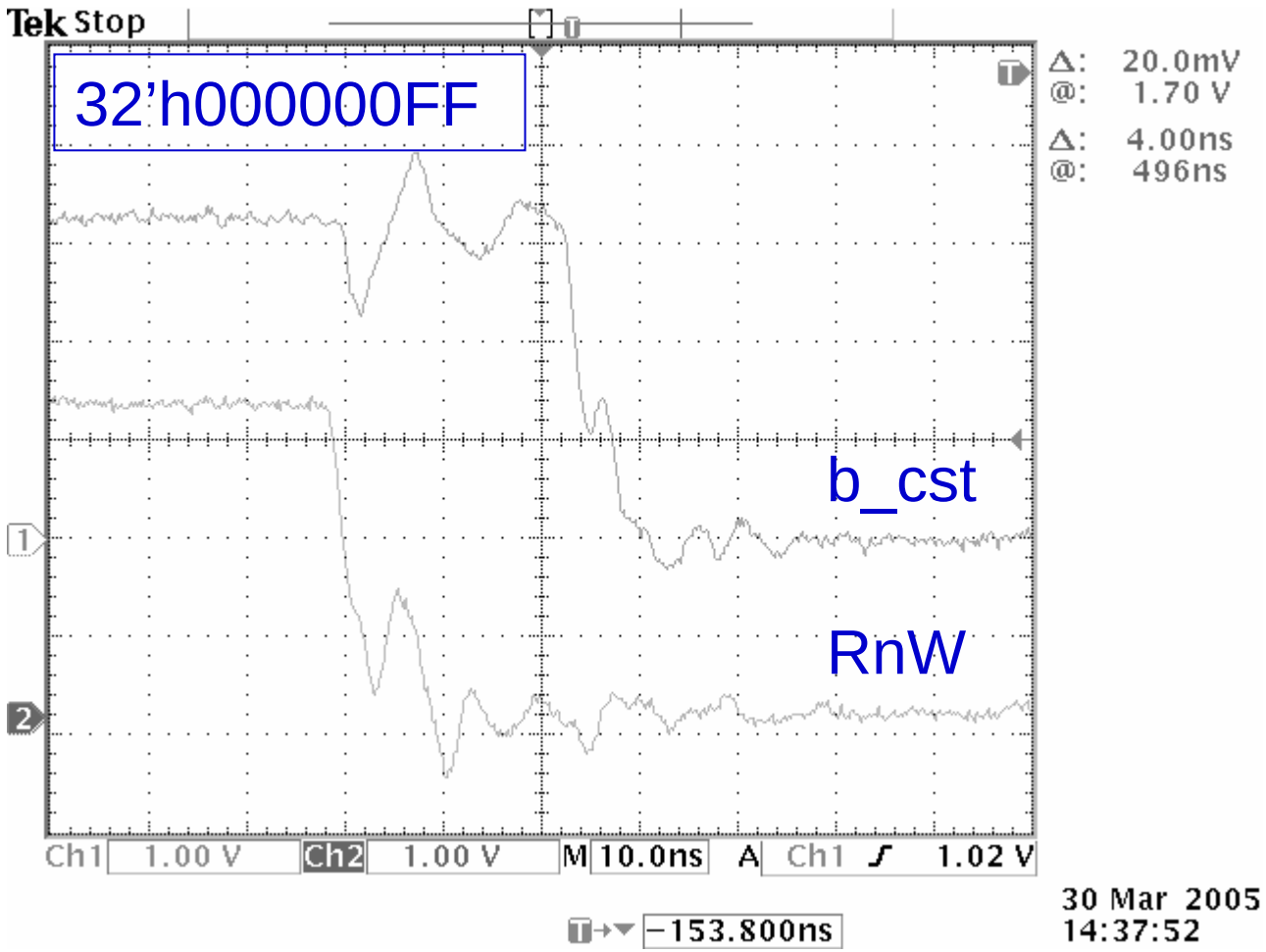
Control lines driven by the DCS and RCU cards



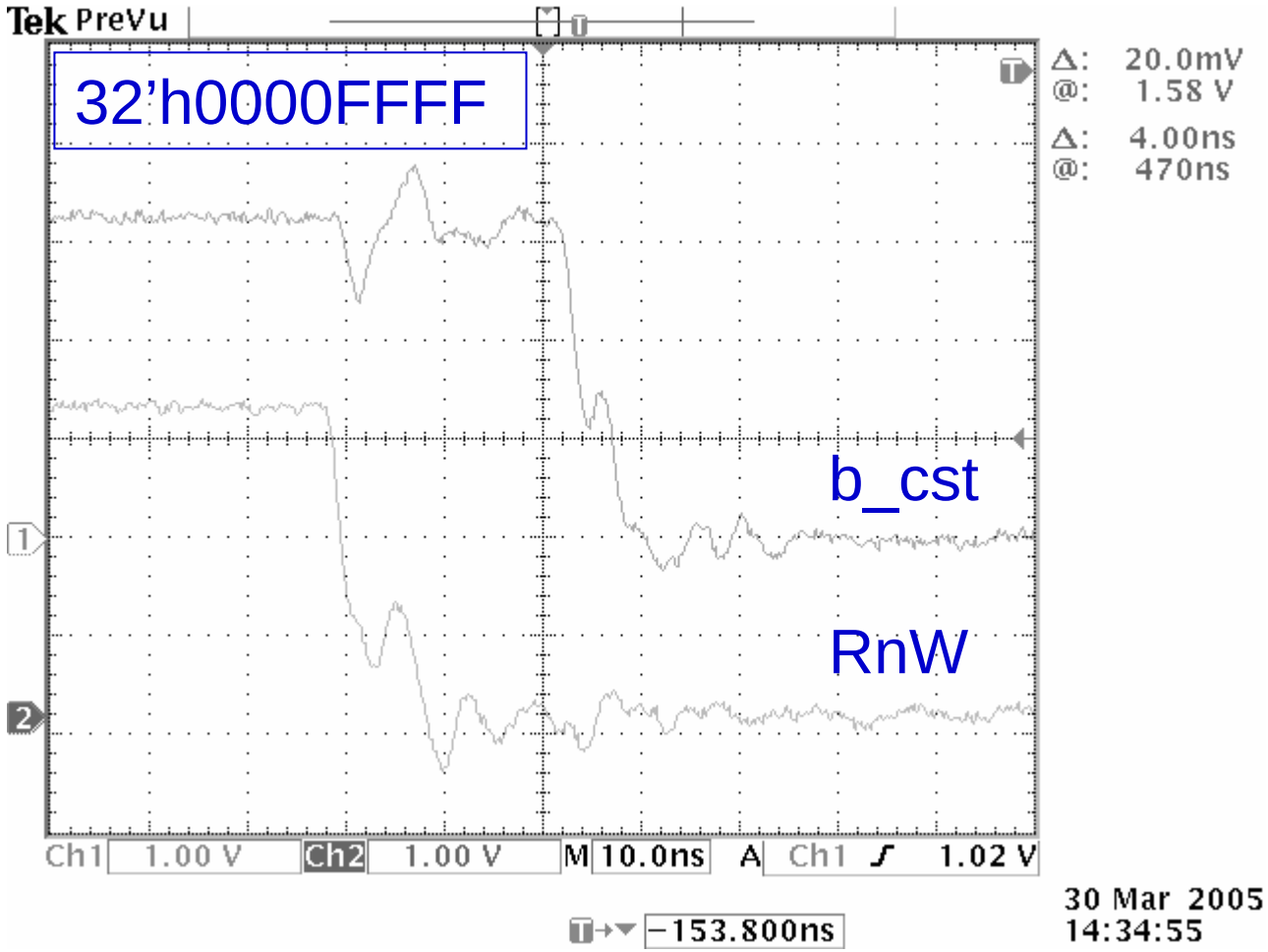
Signal integrity with respect with # switching lines



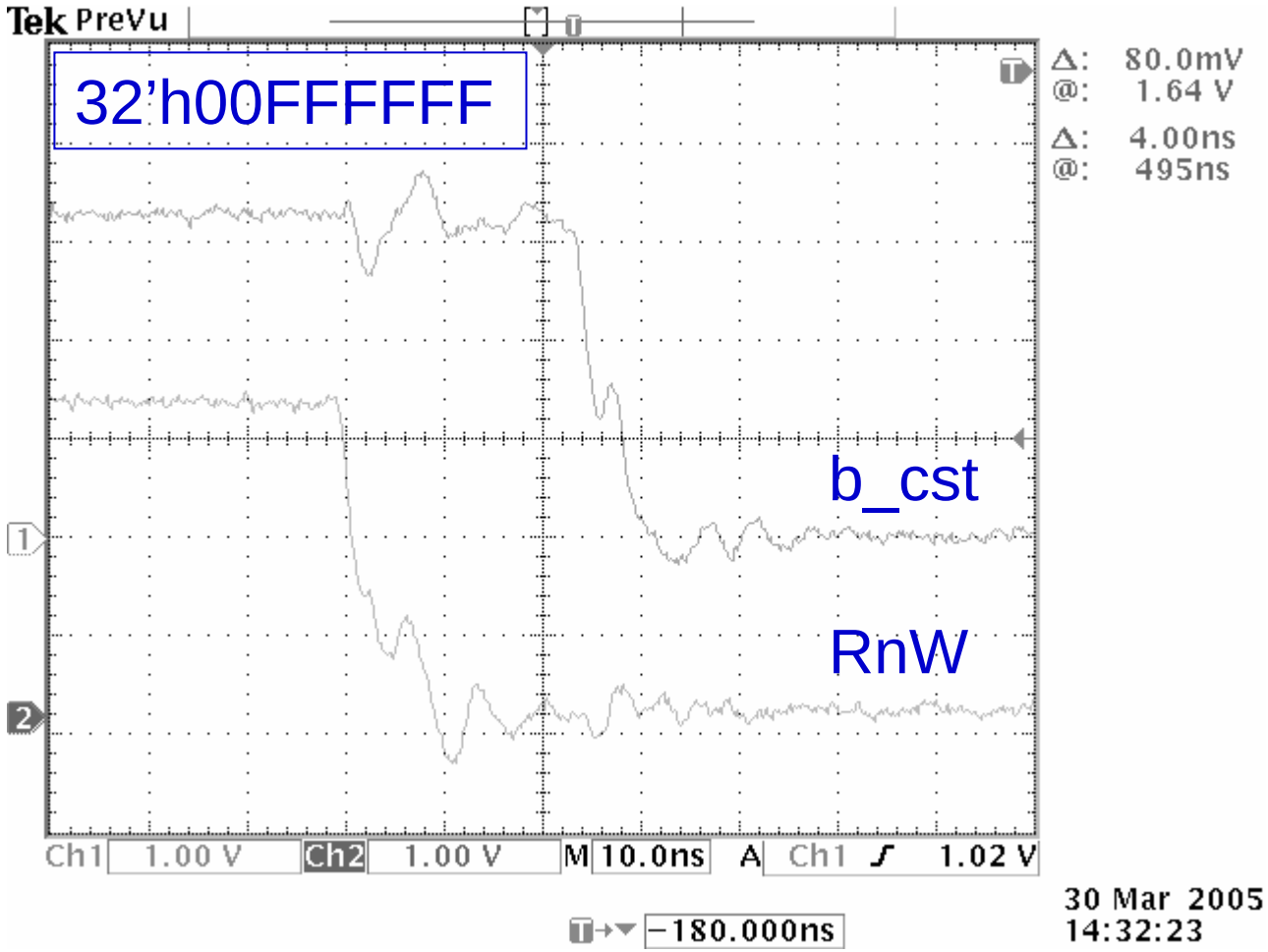
Signal integrity with respect with # switching lines



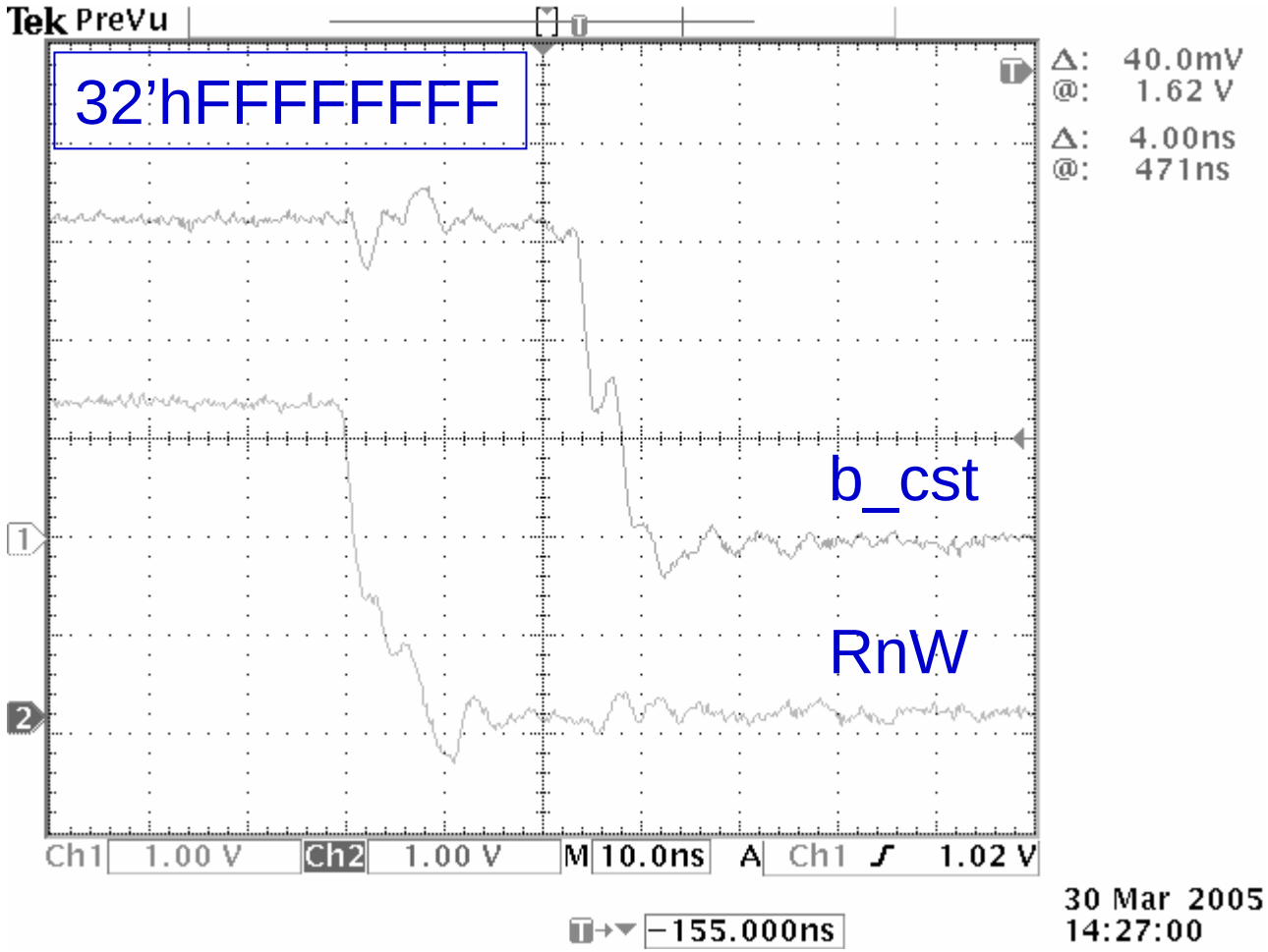
Signal integrity with respect with # switching lines



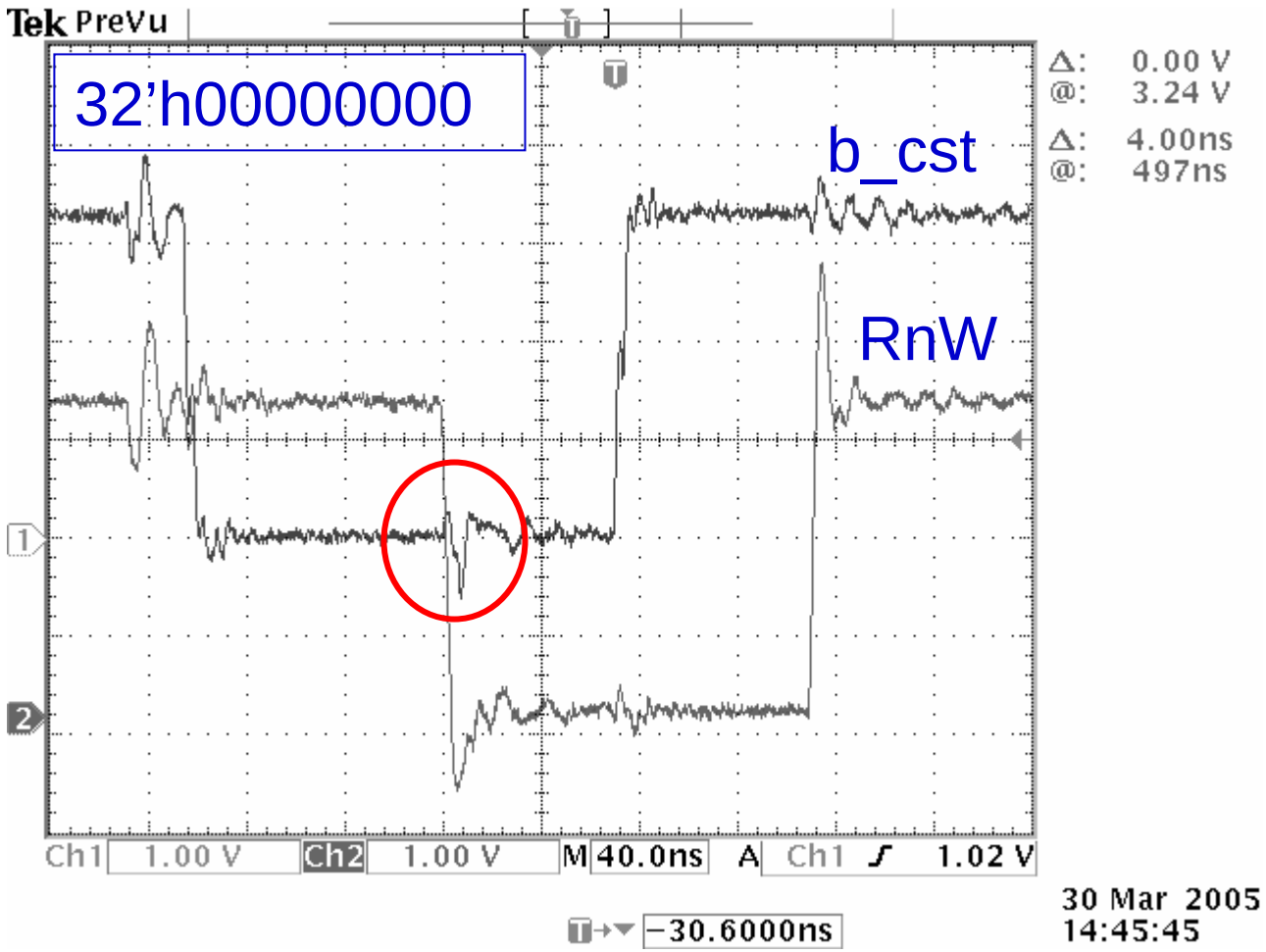
Signal integrity with respect with # switching lines



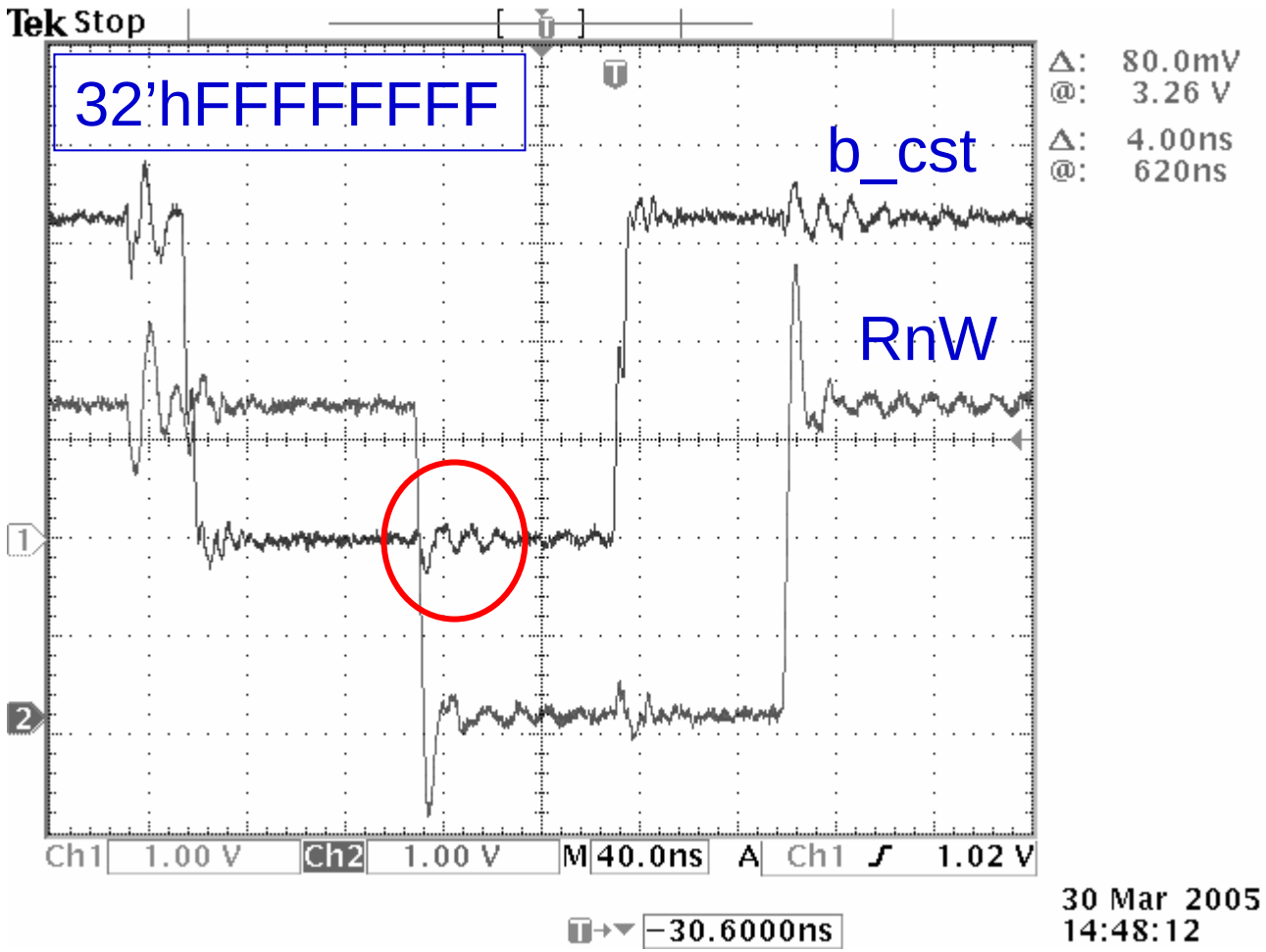
Signal integrity with respect with # switching lines



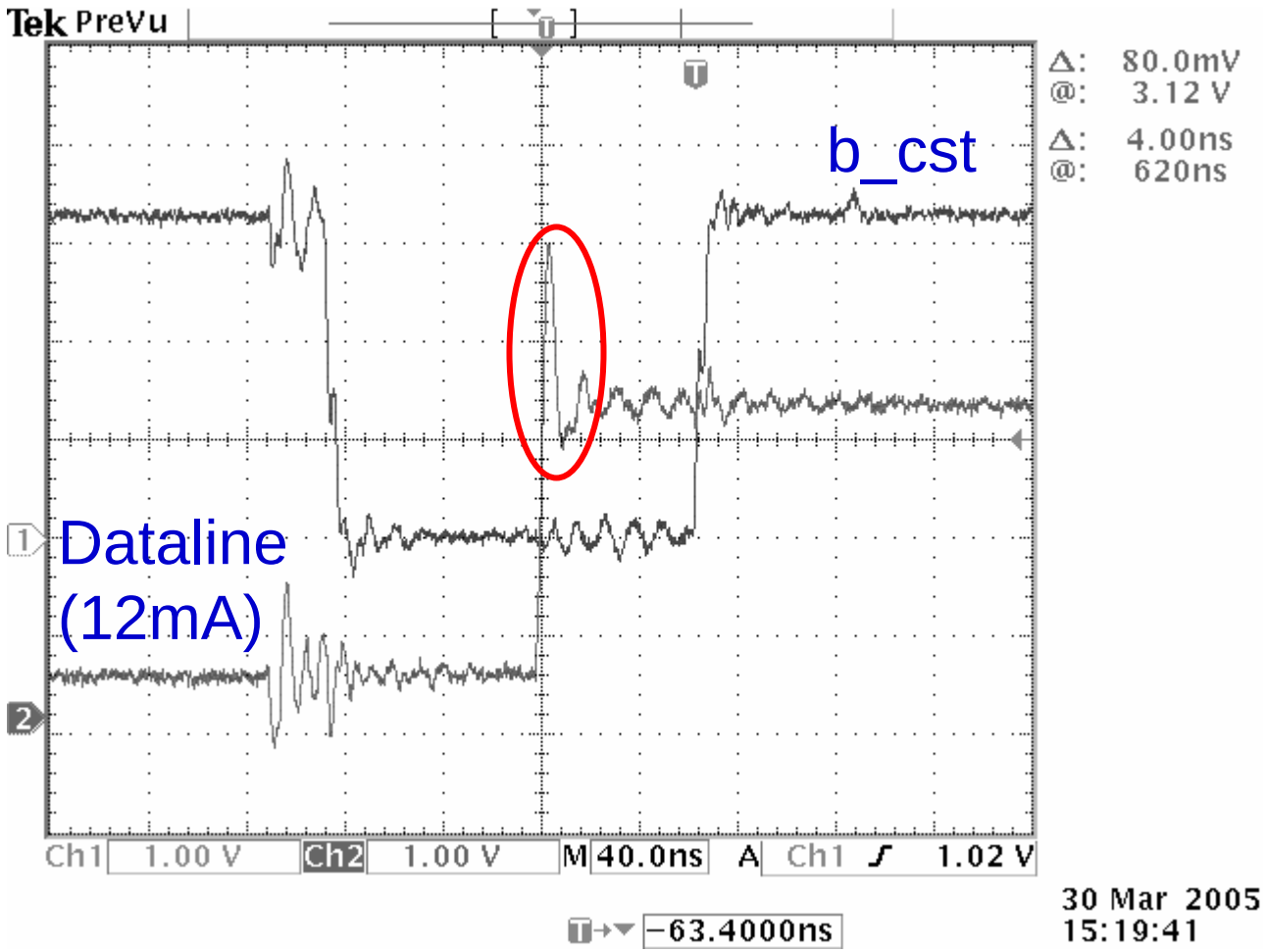
Signal integrity : READ instruction



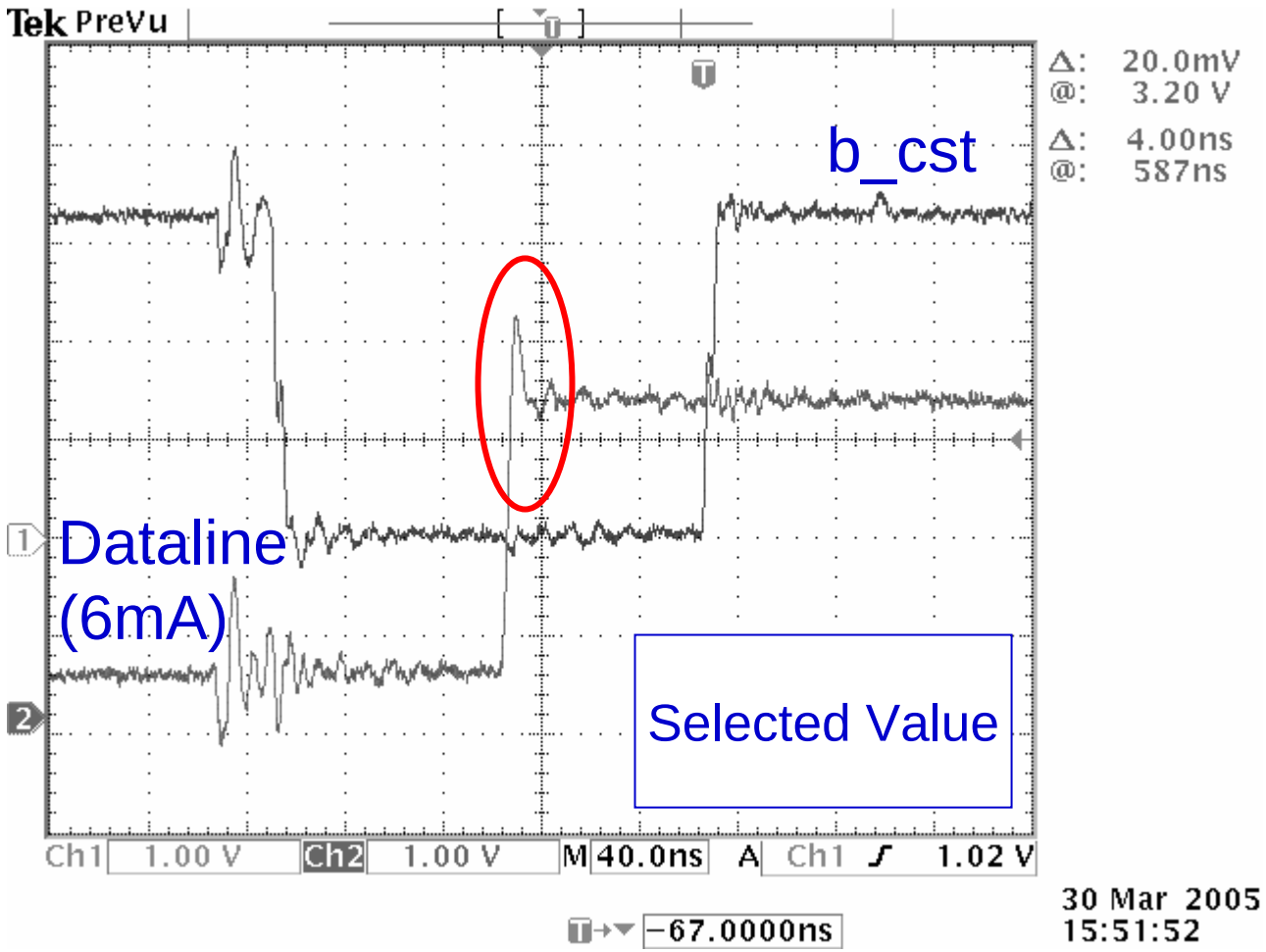
Signal integrity : READ instruction



Signal integrity : READ instruction



Signal integrity : READ instruction



To be addressed …

- What is the nature of the power bounces due to data line switching?
  - Excessive driving strength of the Excalibur FPGA?

  => Modification of current settings in DCS FPGA?

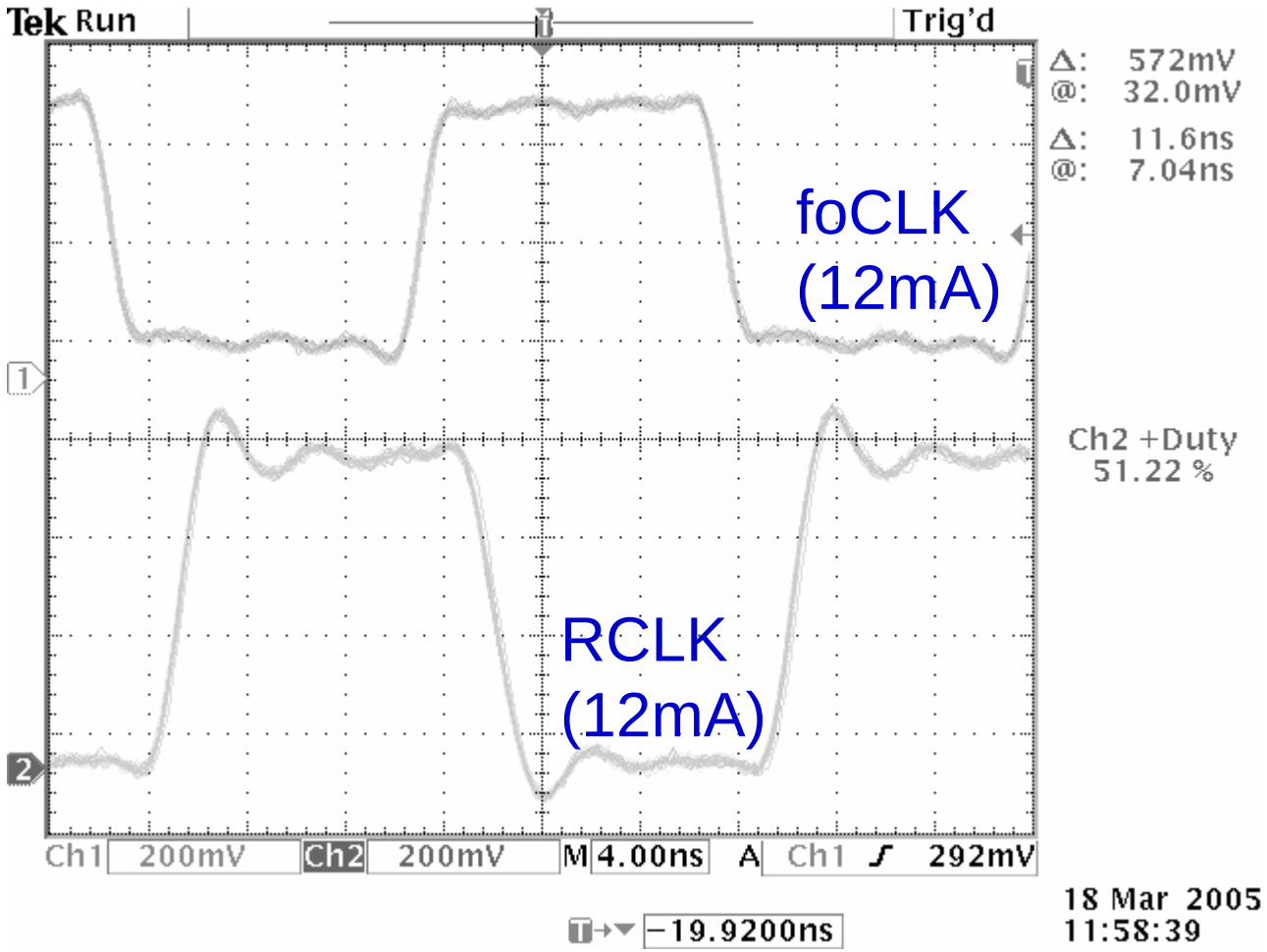
  => Addition of capacitors in the RCU board?

- Clocking Scheme for the DCS board?
  - RCU and DCS with 2 asynchronous clock domains?
  - Synchronous with automatic detection of clock in DCS/RCU cards?

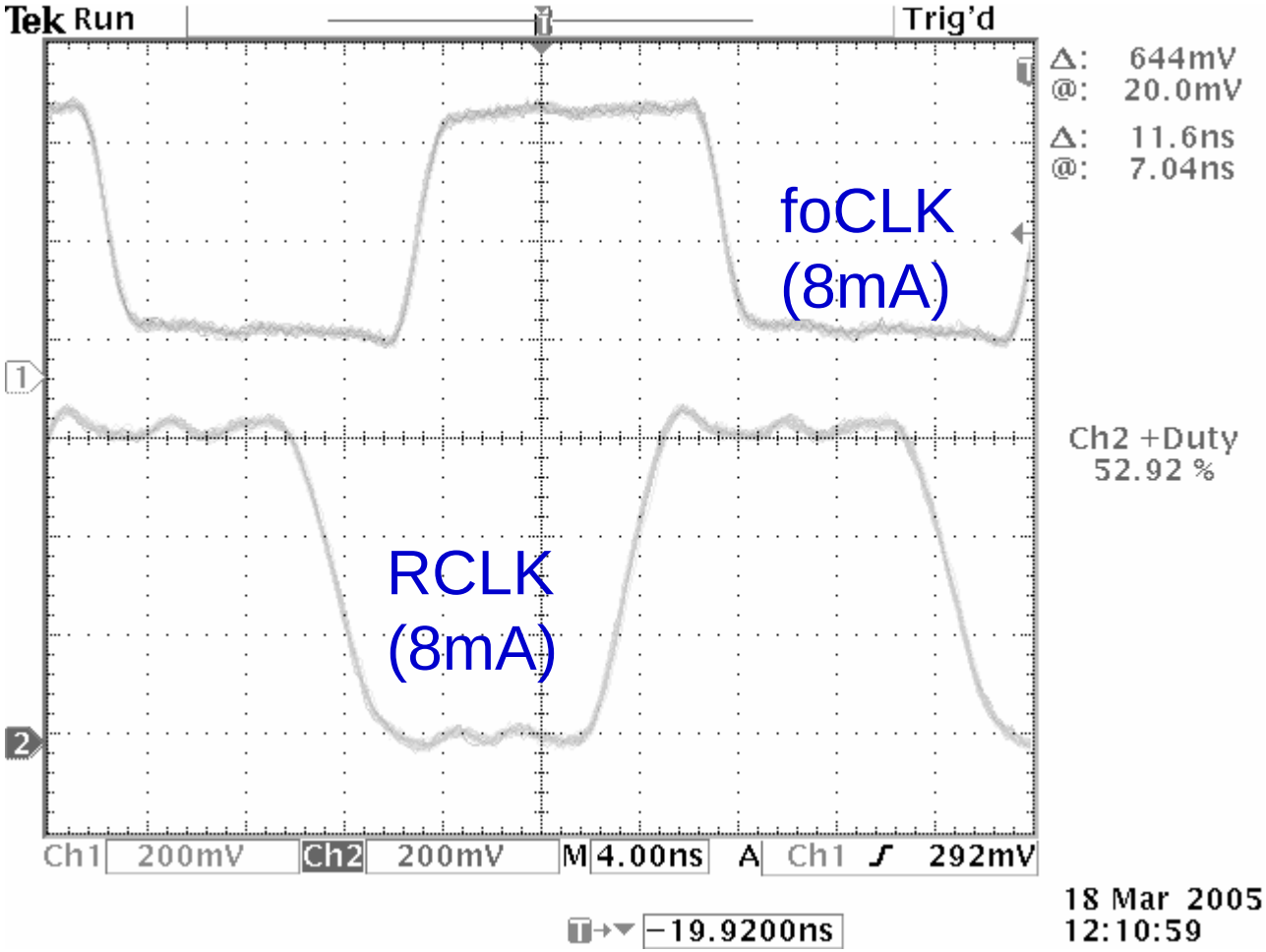
Clock Signals

- foCLK
  - Driven by Xilinx towards SIU card
  - Terminated with 50Ω resistor network on SIU card
  - Tunable in driving strength and phase
- RCLK
  - Driven by Xilinx towards GTL transceiver
  - Sent to both branches of FECs
  - Tunable in driving strength and phase

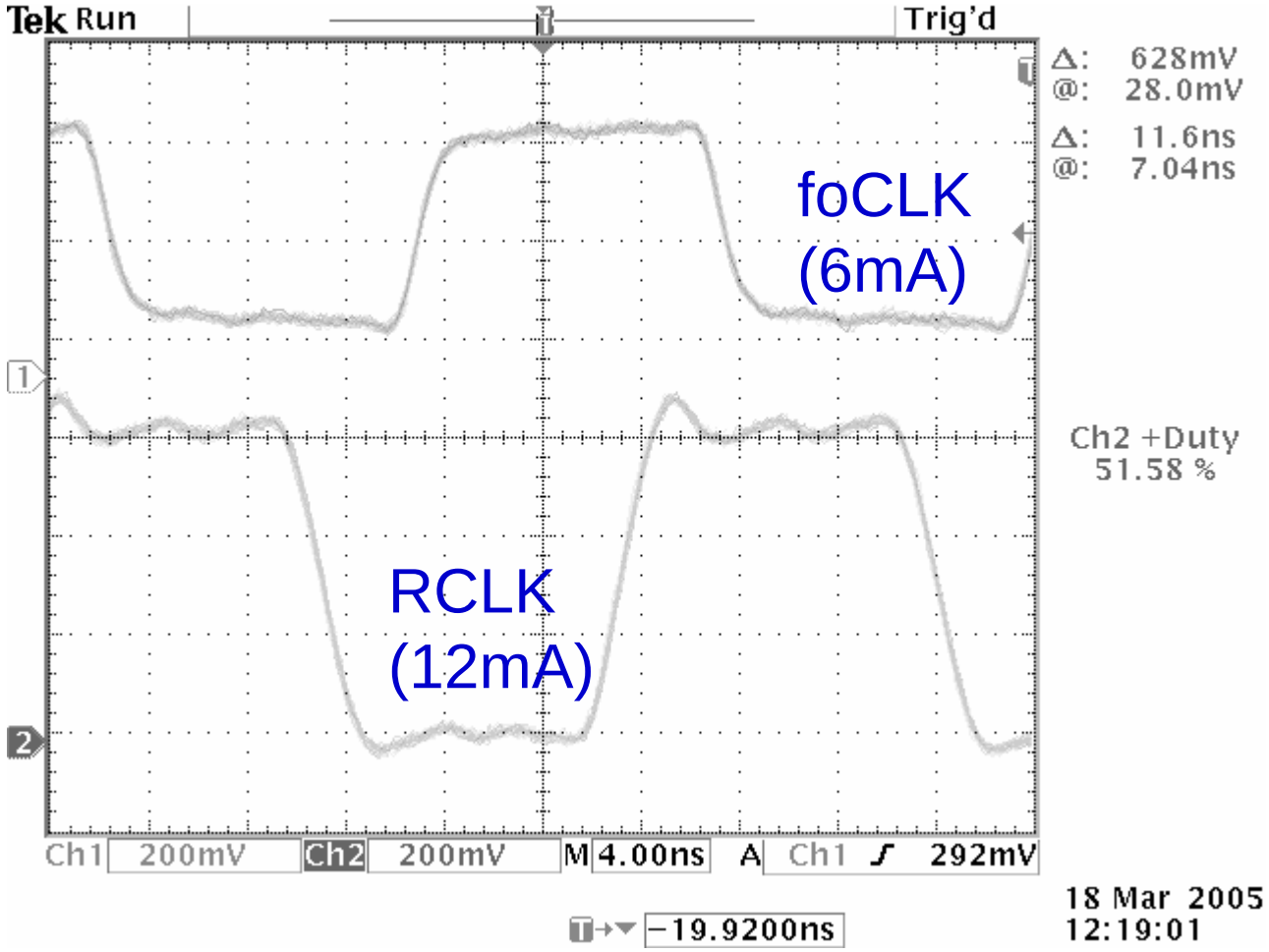
foCLK & RCLK


Tek Run
Trig'd
Δ: 572mV
@: 32.0mV
Δ: 11.6ns
@: 7.04ns
foCLK
(12mA)
RCLK
(12mA)
Ch2 +Duty
51.22 %
Ch1 200mV
Ch2 200mV
M 4.00ns
A Ch1 292mV
−19.9200ns
18 Mar 2005
11:58:39

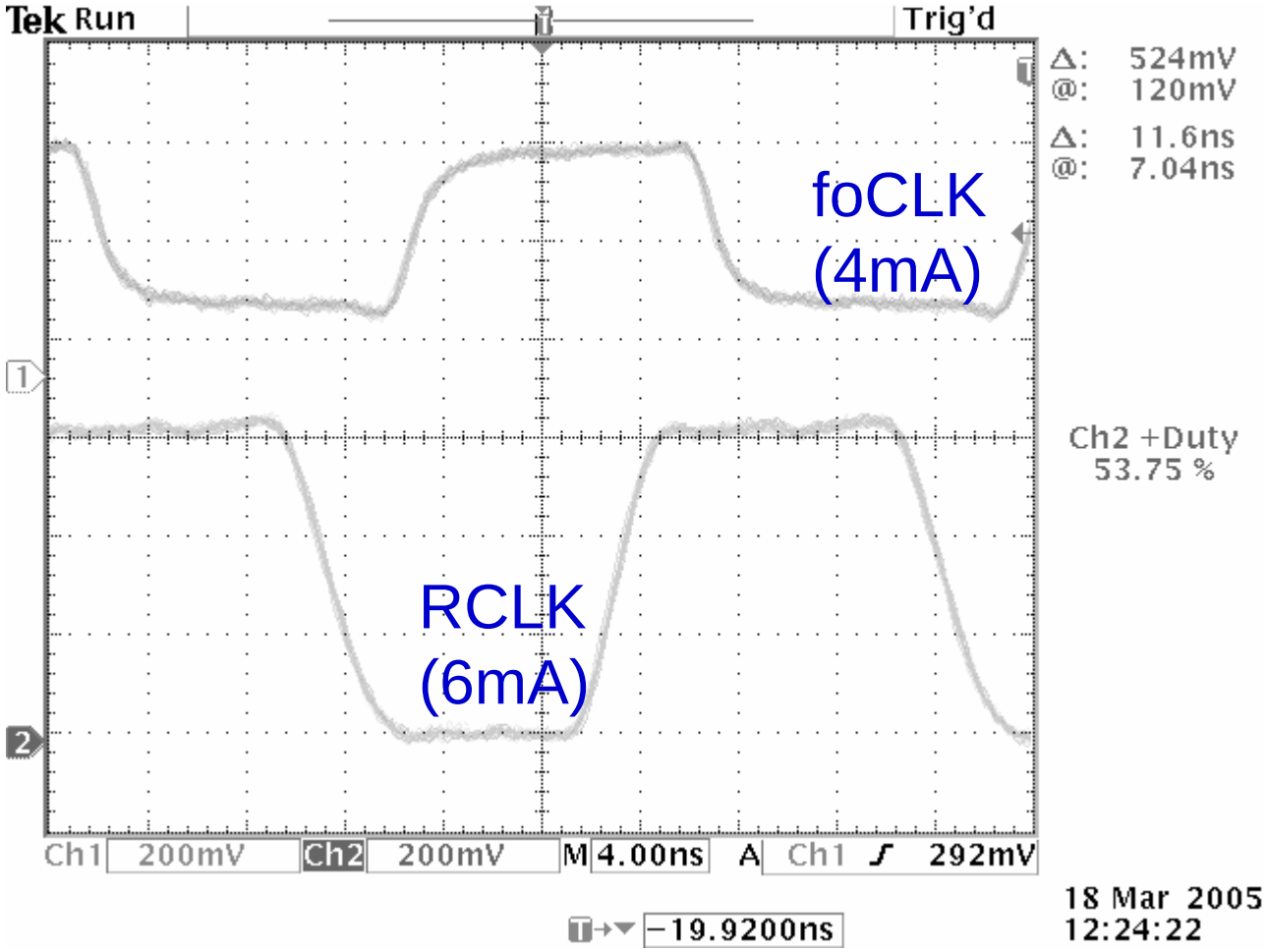
foCLK & RCLK


Tek Run
Trig'd
Δ: 644mV
@: 20.0mV
Δ: 11.6ns
@: 7.04ns
foCLK
(8mA)
RCLK
(8mA)
Ch2 +Duty
52.92 %
Ch1 200mV
Ch2 200mV
M 4.00ns
A Ch1 292mV
−19.9200ns
18 Mar 2005
12:10:59

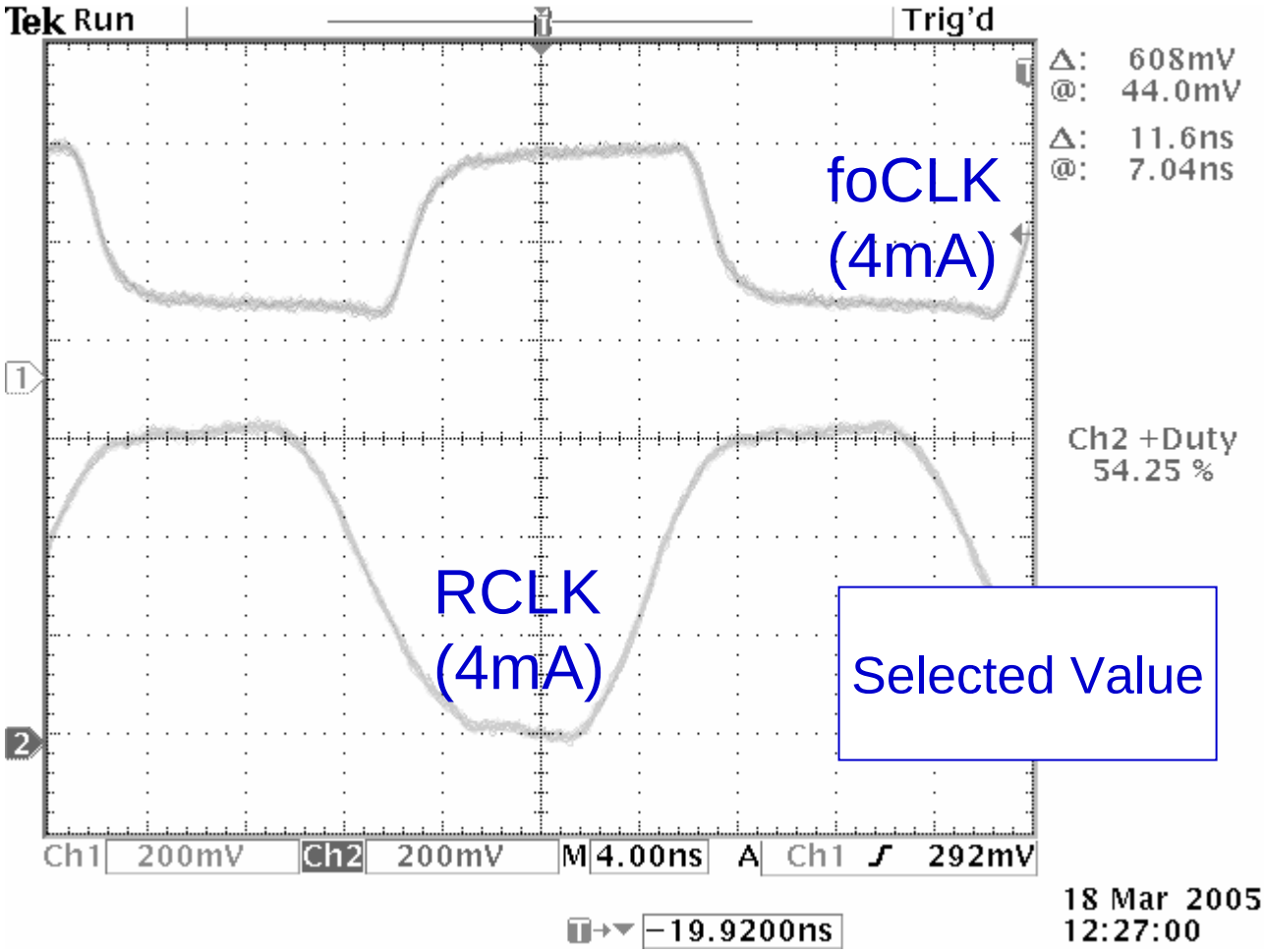
foCLK & RCLK


Tek Run
Trig'd
Δ: 628mV
@: 28.0mV
Δ: 11.6ns
@: 7.04ns
foCLK
(6mA)
RCLK
(12mA)
Ch2 +Duty
51.58 %
Ch1 200mV
Ch2 200mV
M 4.00ns
A Ch1 292mV
−19.9200ns
18 Mar 2005
12:19:01

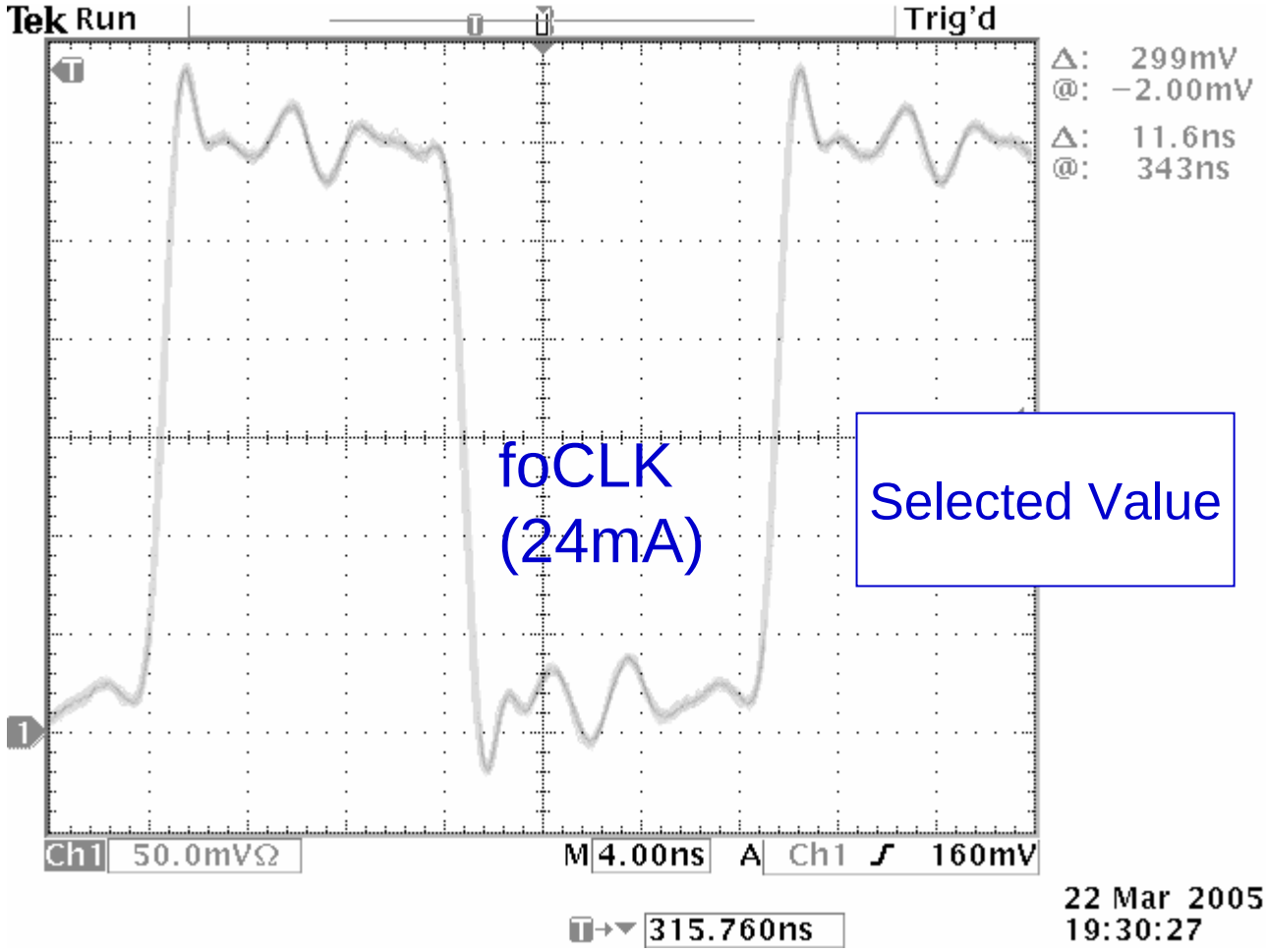
foCLK & RCLK


Tek Run
Trig'd
Δ: 524mV
@: 120mV
Δ: 11.6ns
@: 7.04ns
foCLK
(4mA)
RCLK
(6mA)
Ch2 +Duty
53.75 %
Ch1 200mV
Ch2 200mV
M 4.00ns
A Ch1 292mV
−19.9200ns
18 Mar 2005
12:24:22

foCLK & RCLK


Tek Run
Trig'd
Δ: 608mV
@: 44.0mV
Δ: 11.6ns
@: 7.04ns
foCLK
(4mA)
Ch2 +Duty
54.25 %
RCLK
(4mA)
Selected Value
Ch1 200mV
Ch2 200mV
M 4.00ns
A Ch1 292mV
−19.9200ns
18 Mar 2005
12:27:00

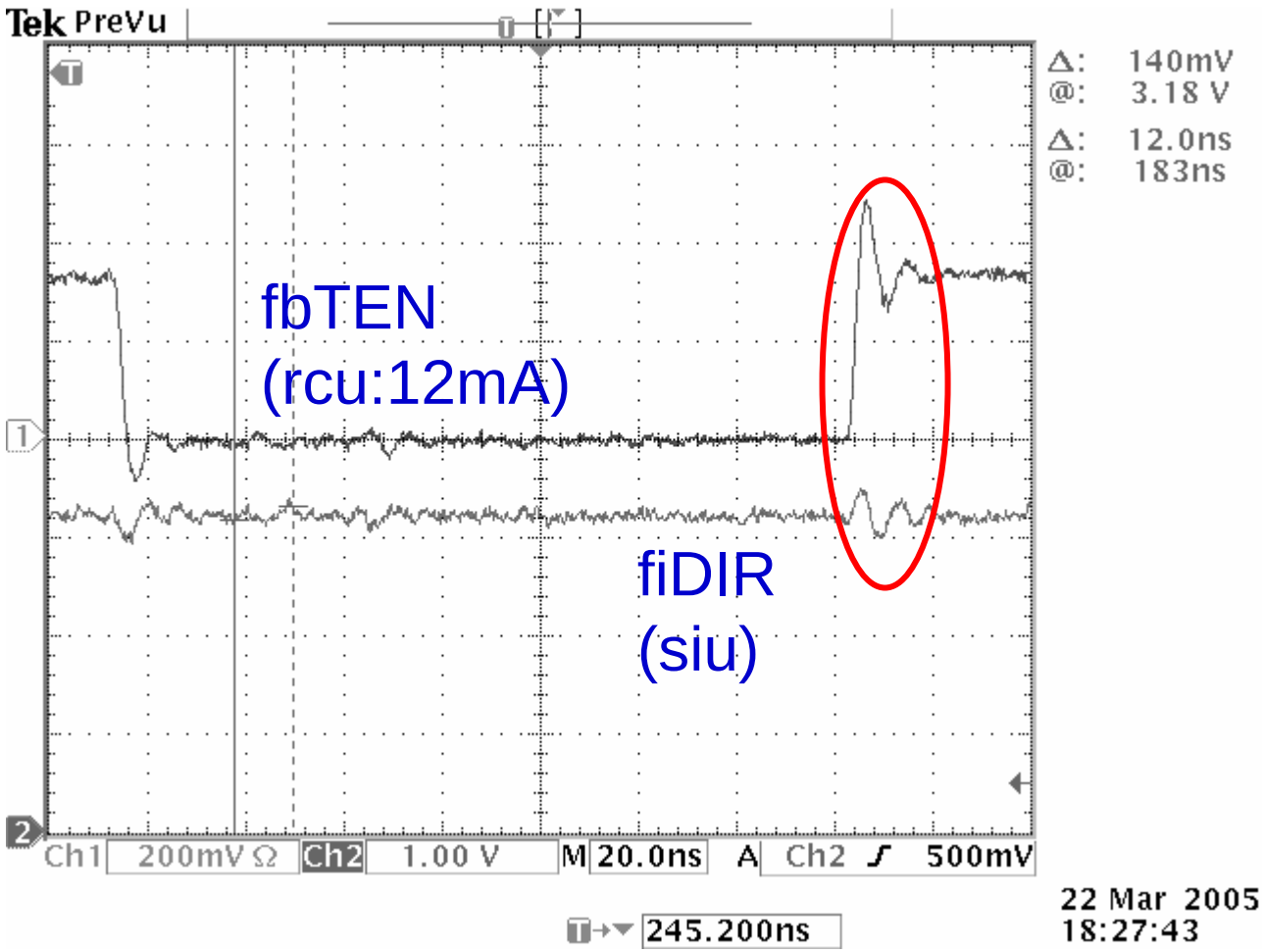
foCLK & RCLK


Tek Run
Trig'd
Δ: 299mV
@: −2.00mV
Δ: 11.6ns
@: 343ns
foCLK
(24mA)
Selected Value
Ch1 50.0mVΩ
M 4.00ns A Ch1 160mV
315.760ns
22 Mar 2005
19:30:27

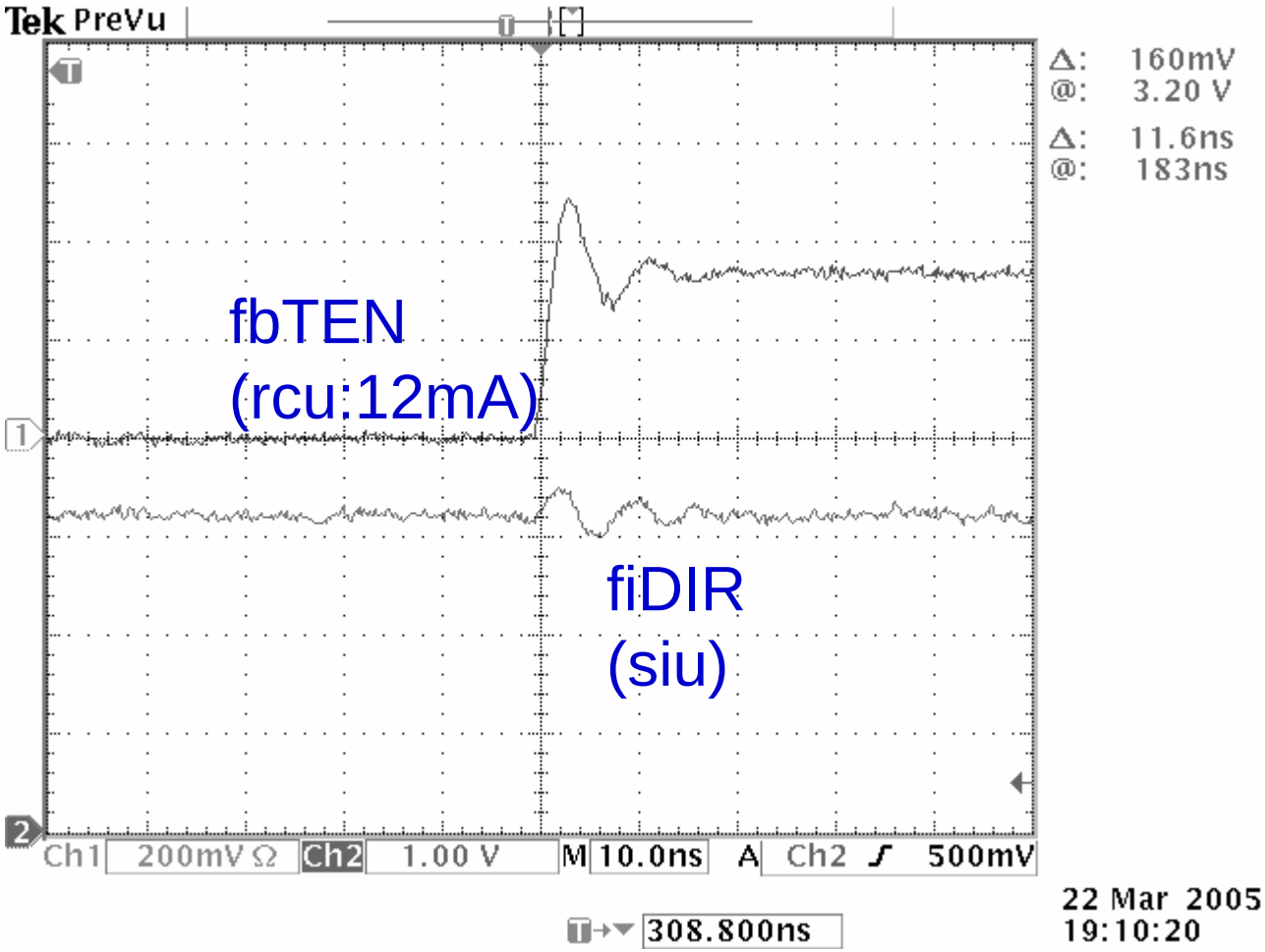
SIU Interface

- Measurements @ PCB traces -

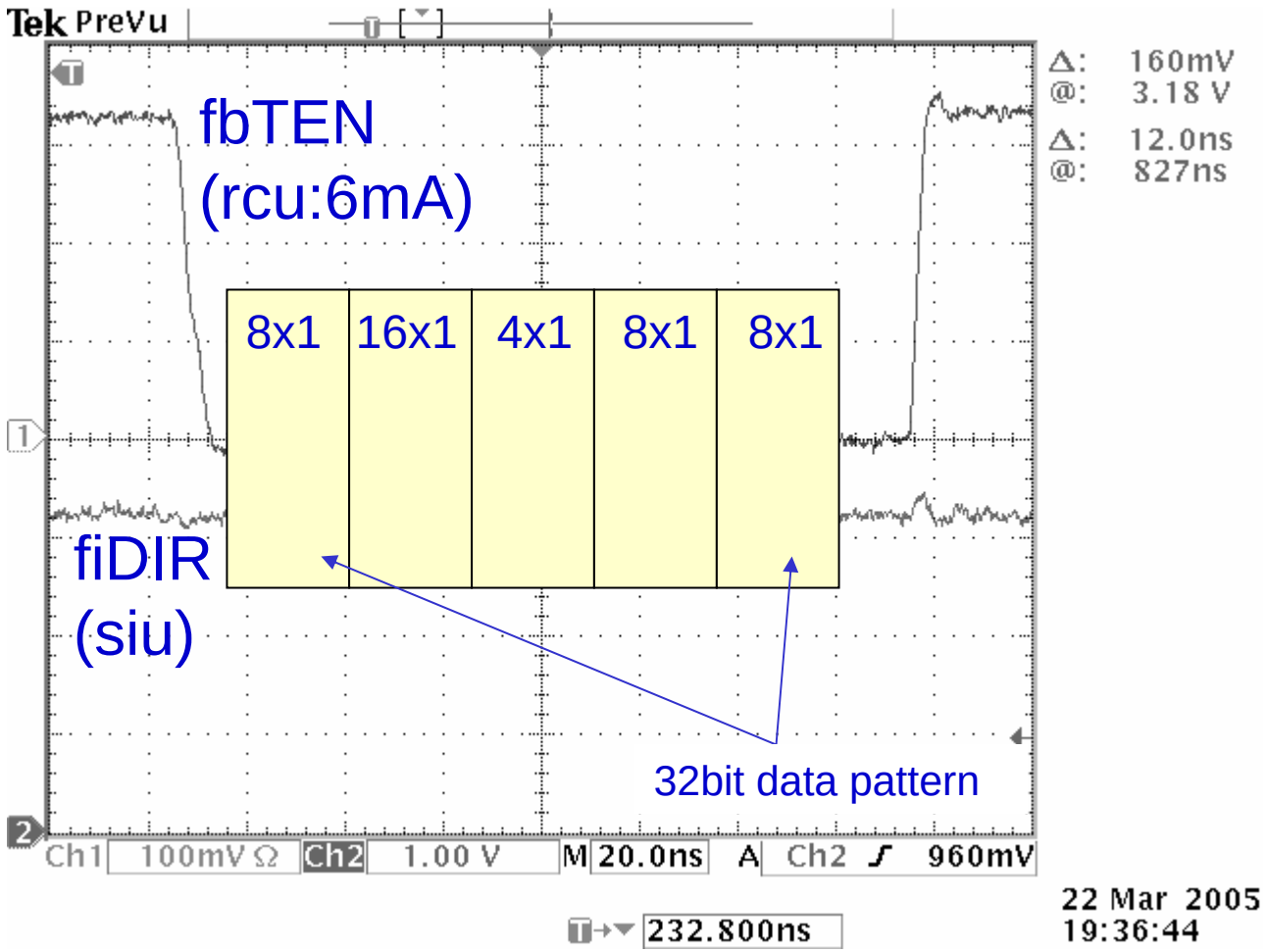
SIU control signals



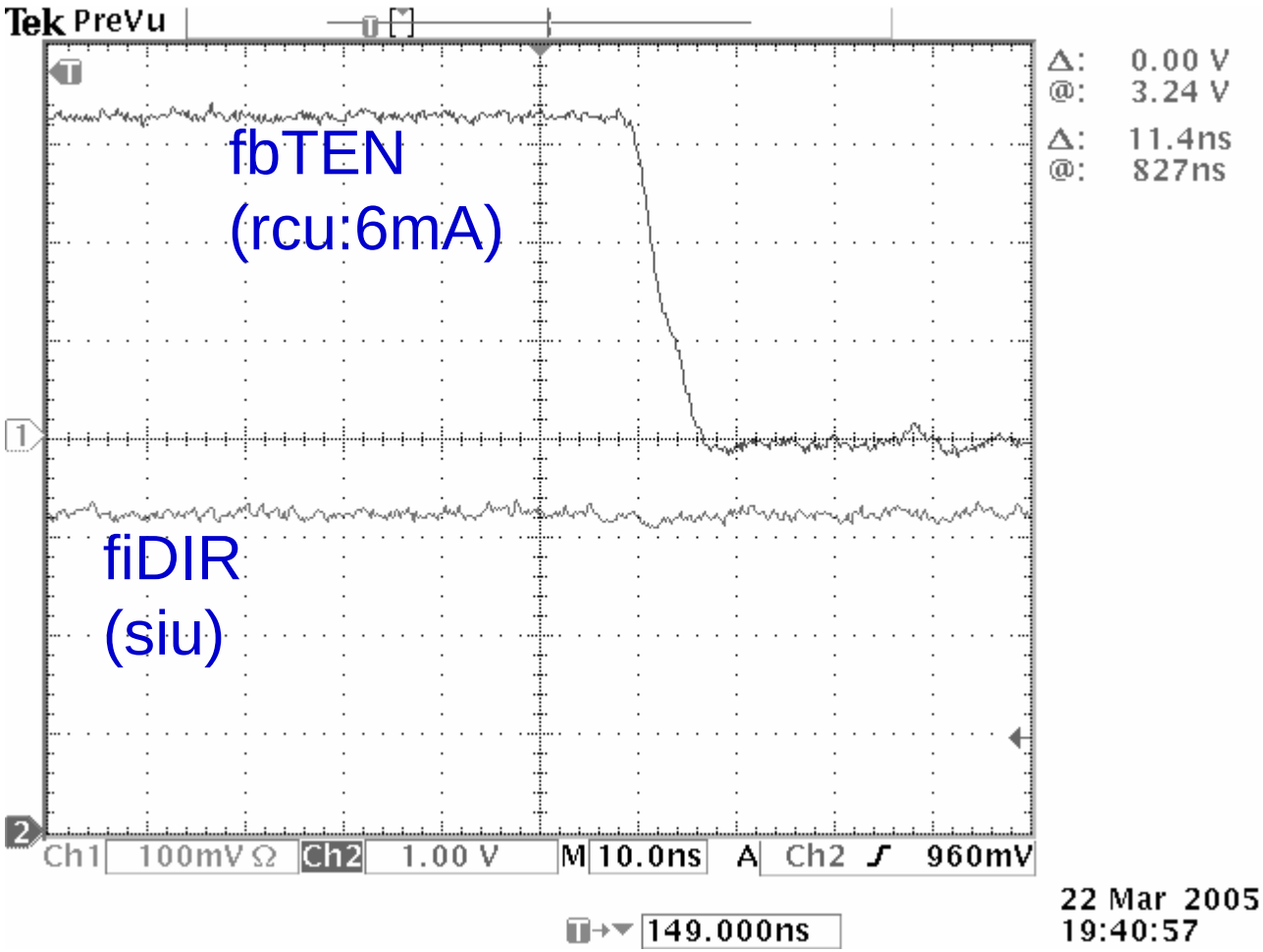
SIU control signals



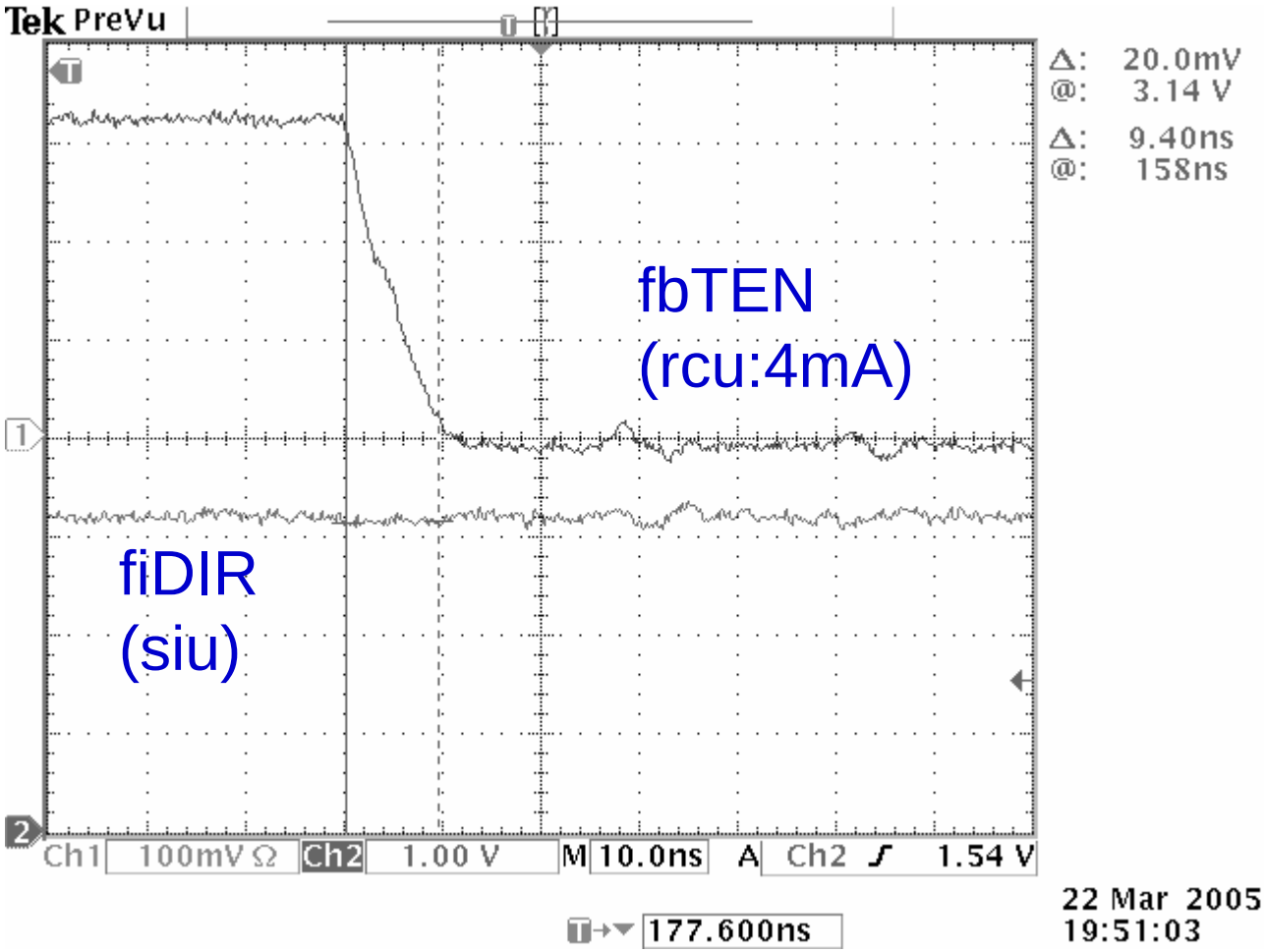
Signal integrity with respect with # switching lines



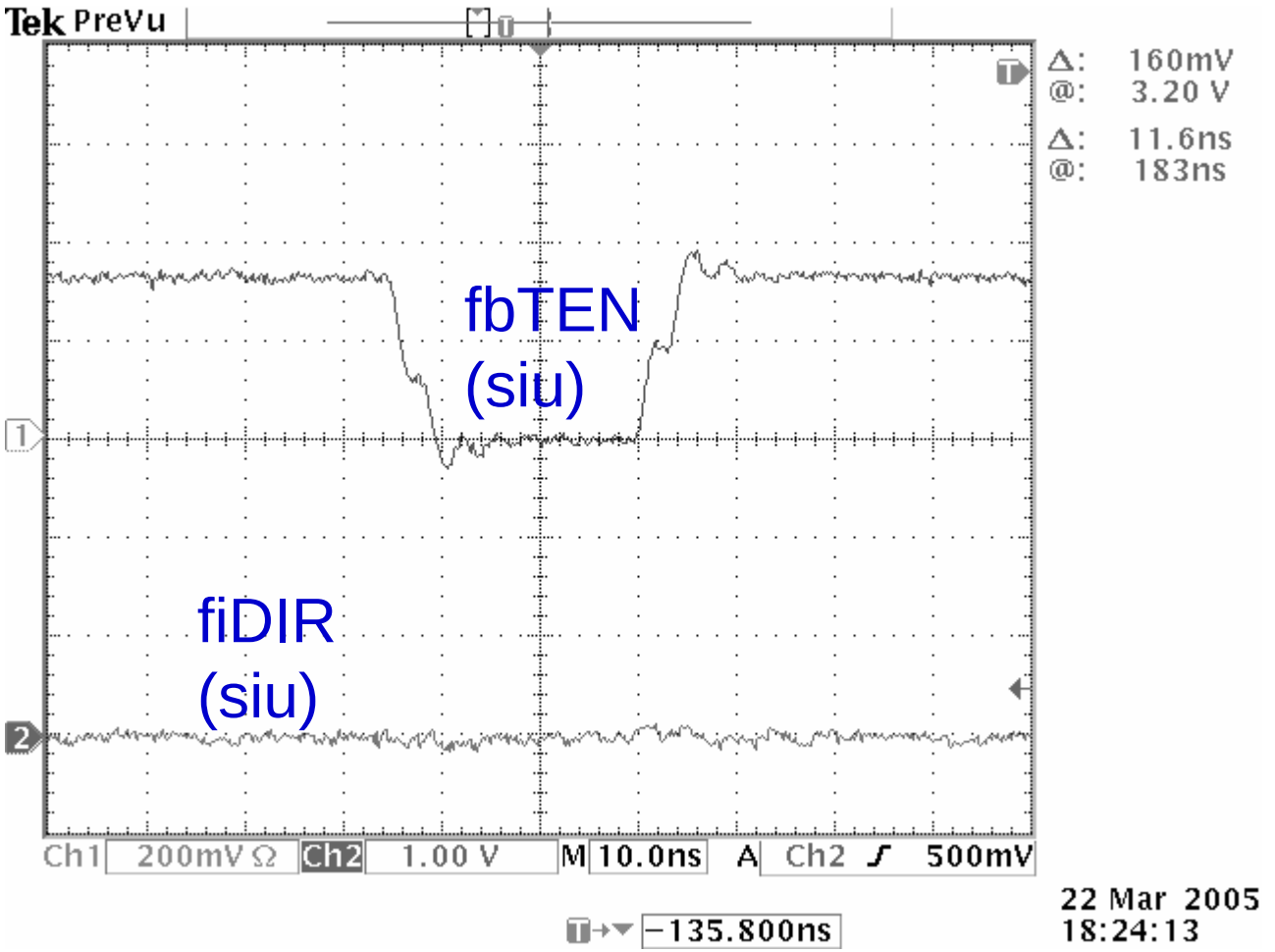
SIU control signals



SIU control signals



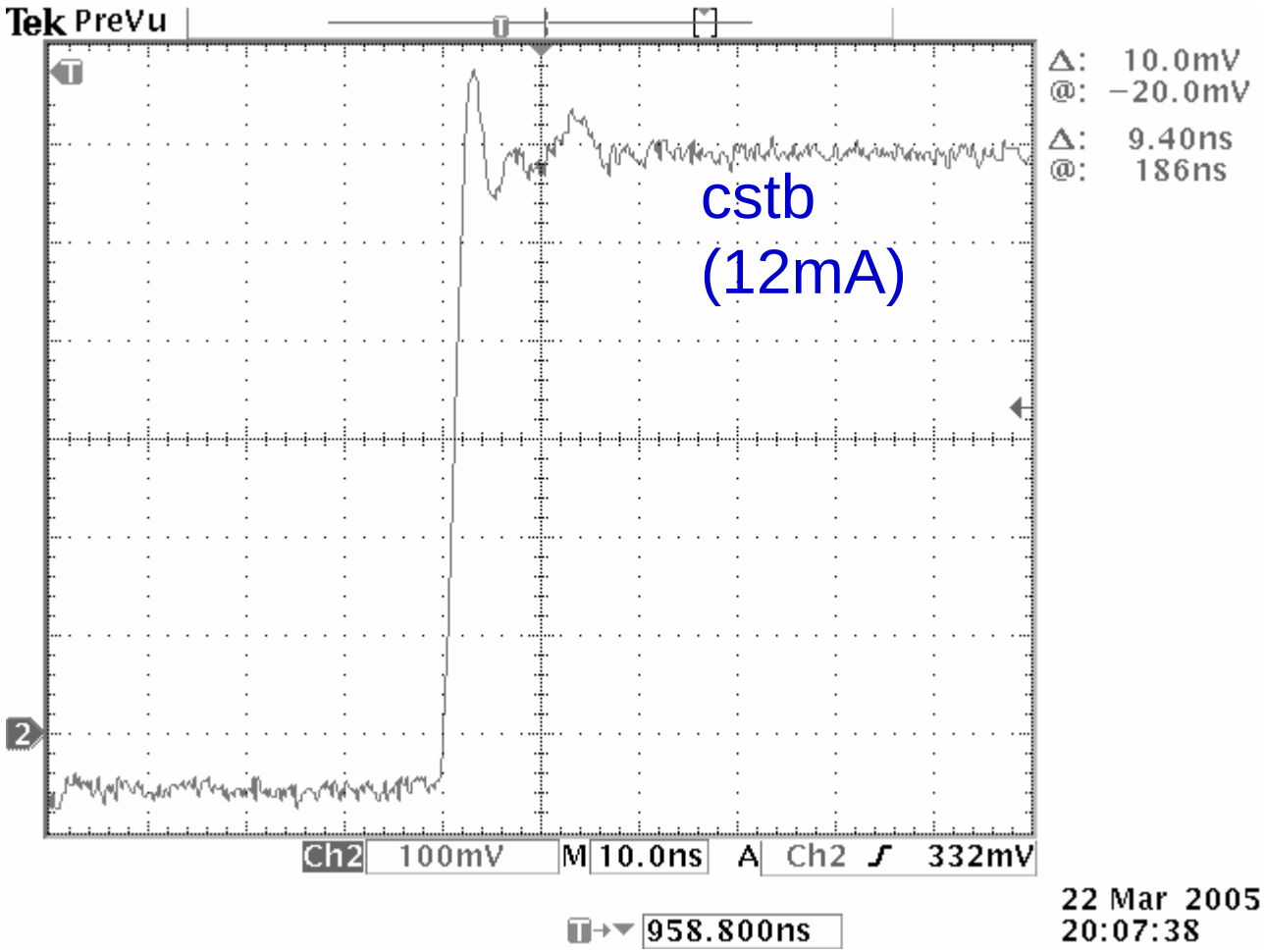
SIU control signals



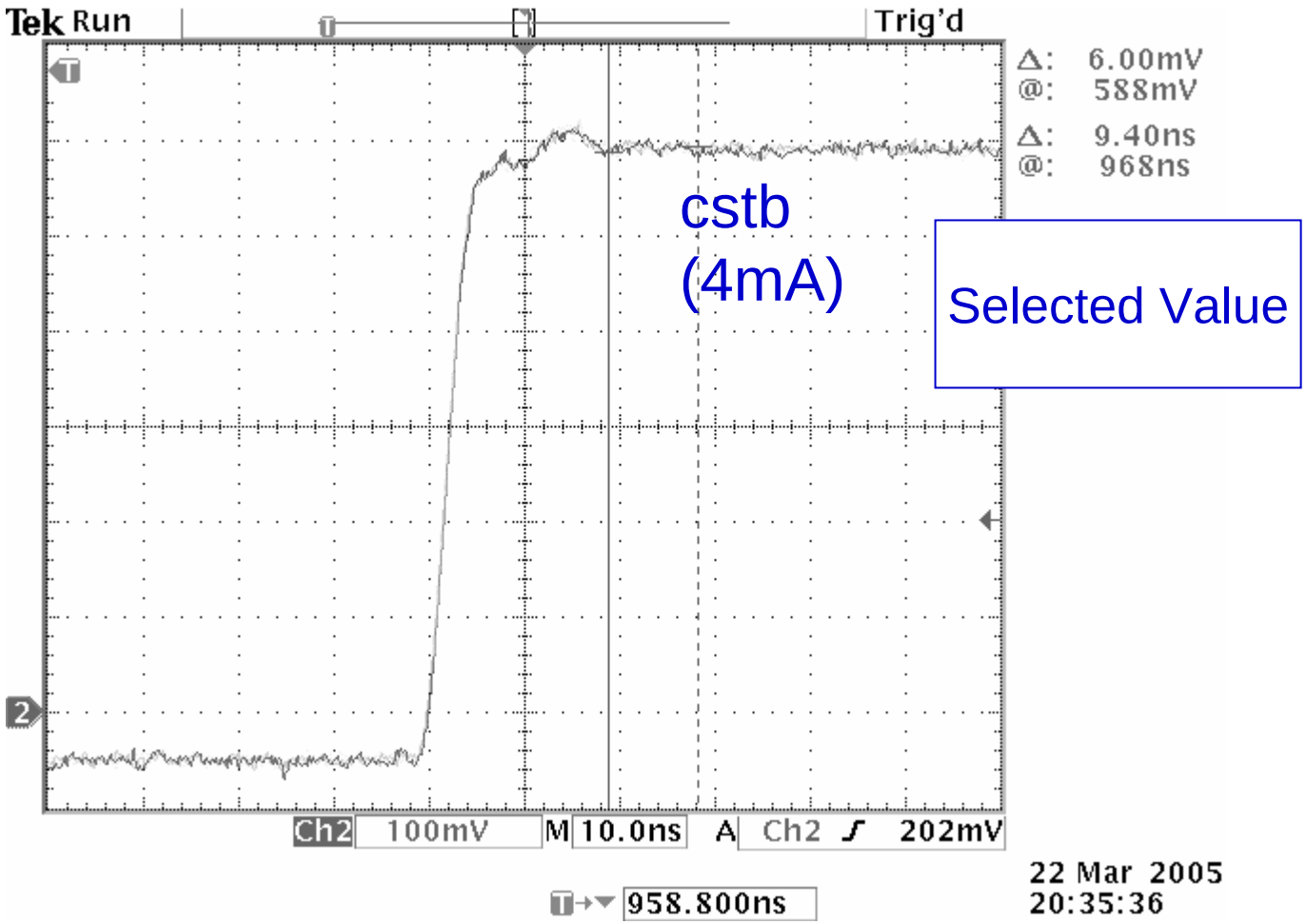
FEC Interface

- Measurements @ PCB traces -

FEC control signals



FEC control signals



Conclusions

- Driving strength of all signals at the output of Xilinx has been adjusted.
- Calibrate phase between [RCLK & foCLK] with the internal Xilinx clock.
- Sampling clock generation to be changed, avoiding PLL.
- Integrity of DCS issued signals to be better understood. (Power Bounces)