Configuring of Xilinx Virtex-II

- Proposed solution -

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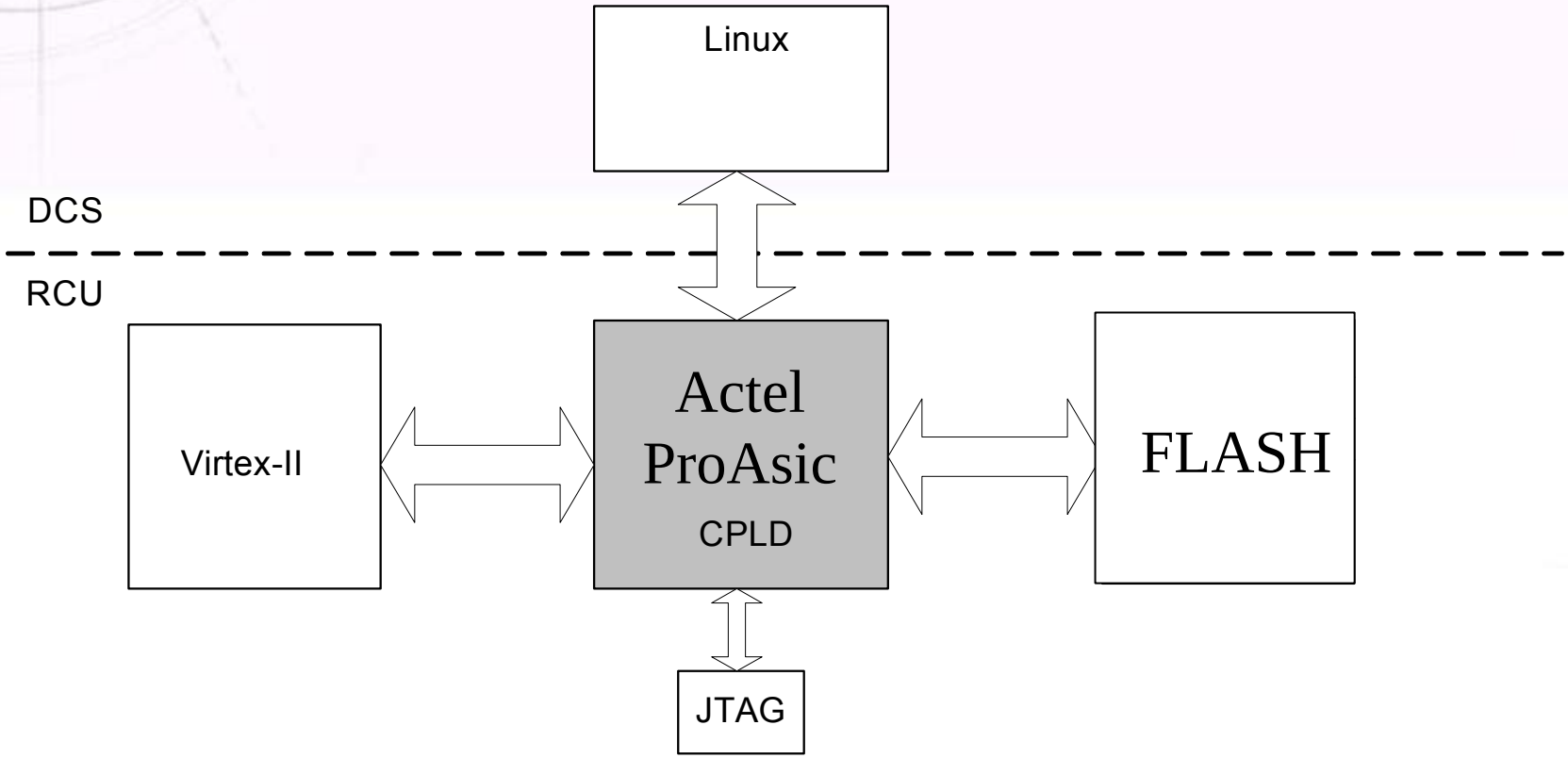
Overview

- Requirements
  - Uppsala
  - Final design
- Xilinx Virtex-II configuration
- Status and ongoing work

System modules



Configuration requirements

- *Uppsala irradiation test*
  - Full configuration on power-up
  - Scrubbing from Flash
  - Readback and verify (DCS controlled ?)
- *Additional functionality for final design*
  - Configure Virtex-II from DCS-card
  - Readback and verification against stored files in Flash (CPLD/DCS?)
- *FLASH content*
  - Full initial bit stream
  - Individual frame data (Frame by frame readback and refresh)
  - Full partial bit stream (Scrubbing mode only)
  - Max file size < 400kB (FLASH – 8 MB)

Configuring modes for Virtex-II

- 5 built-in modes
  - ***JTAG***
  - Master/Slave Serial
  - Master/***Slave SelectMap***

- JTAG and Slave SelectMap is chosen for RCU.
- 3 mode pins (M2, M1, M0) are used for setting the mode.

JTAG

- JTAG is the default mode.
  - JTAG always work whenever connected, no matter what mode is selected.
- Benefits:
  - Well known interface that is easy to use and is supported by all companies.
  - Possibility to do a readback
  - No extra firmware/software required except what is delivered by Xilinx.

Slave SelectMap

- 8 bit wide databus
- 7 control/status lines
- External clock is used for configuring.
- Mode pins should be set to 110 (M2, M1, M0)
  - Note: If connected to a 3.3V network, these inputs must have a 100Ω serial resistor attached

- Benefits:
  - Parallel data transport => fast interface.
  - Possibility to do readback of configuration memory.

Active Partial Reconfiguration

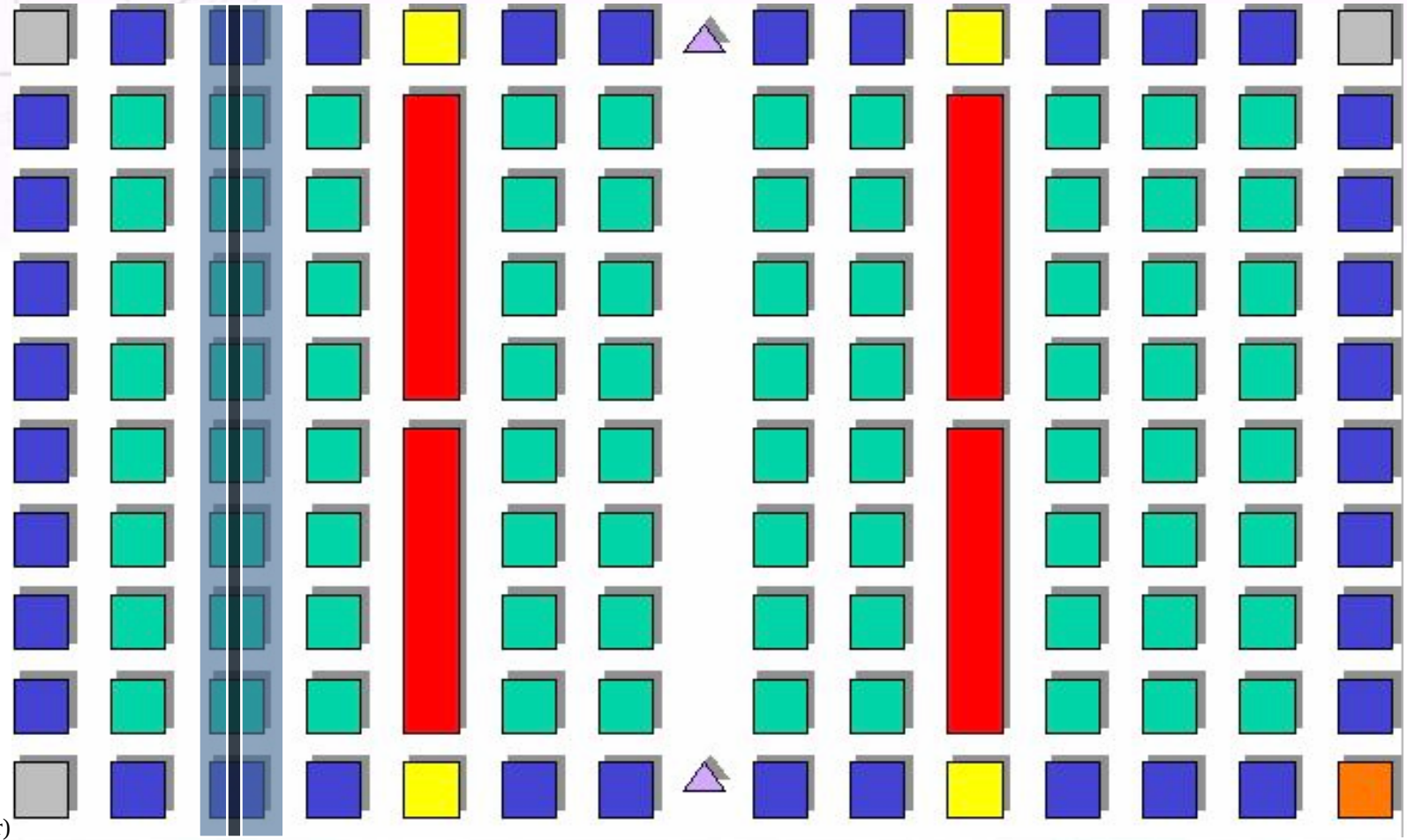
- How does it work?

- Configuration Space divided into units, “frames” in Xilinx terminology
- ‘Partial’: frames are individually reconfigurable
- ‘Active’: without interrupting the device,

  glitch-free: no change → no signal flanks
- Configuration is ‘atomic operation’ (no bit shifting)

(Gerd Tröger)

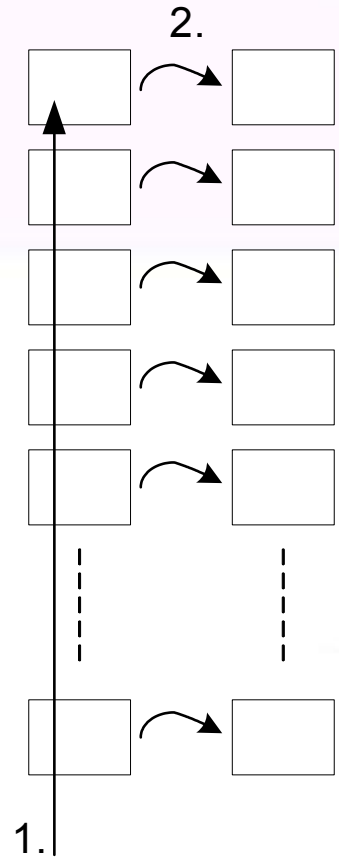
Configuration Frames



(Gerd Tröger)

What is Scrubbing?

- Scrubbing is when the FPGA has been reconfigured without first deleting existing configuration.
- This is possible because there is a shadow register column for the configuration register columns.
- A scrubbing cycle should always be preceded and followed by an abort-command, according to documentation.



Operation of system

1. Initial configuration
2. Read back frame by frame and store in FLASH (Or produce frame data from software)
3. Scrubbing (continuously or/and on demand ?)

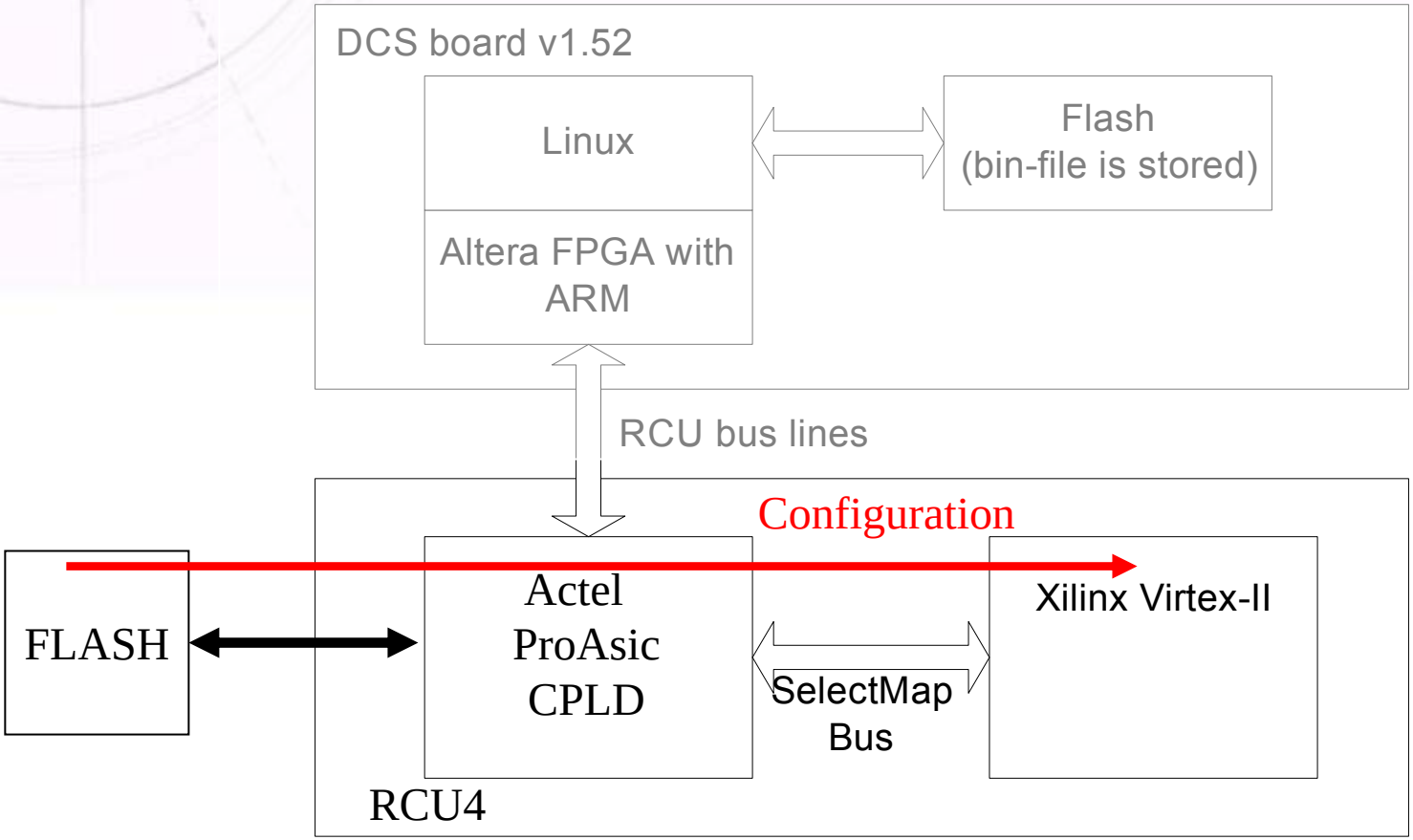
   (a) Full partial scrubbing only

   (b) Readback, verify and scrub (frame by frame)

Status (from last meeting)

- Changed the DCS messagebuffer-design so that Linux (ARM processor) have complete control of the RCU bus lines (data, address & ctrl)
- Wrote a device driver in C that configures the design using controlled clock scheme. (Virtexdriver.c)
- Made a simple design in the Altera CPLD that maps the selectMap bus to the RCU bus.
- This means we have a ”tunnel” going from linux directly to the SelectMap bus.

Sketch of test design



Progress & ongoing work

- Initial configuration of Virtex-II from flash memory
  - Improved configuration speed
  - 40 ms vs 600 ms from DCS software
- Small change needed in order to implement scrubbing functionality
- Porting of CPLD firmware on RCU4 (ProAsic) and further integration with DCS firmware/software
- Add functionality from DCS card
  - Configuration and scrubbing
  - Readback of configuration memory
  - Programming of flash memory

Status

- **Uppsala**
  - Looks good
  - Small changes to implement scrubbing
  - A bit more work on integrating CPLD firmware with DCS card. Feasible within preparation time period
- **Final design**
  - Readback and verification functionality in CPLD
    => Requires increased firmware complexity
  - In software – already implemented by Gerd Tröger, in principle only hardware adjustments are needed.
  - Software solution dependent on DCS workload

More information

http://www.xilinx.com

- Ug012.pdf
  - **Virtex-II Pro and Virtex-II Pro FPGA User Guide**
- Ds083.pdf
  - **Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Complete Data Sheet**
- Xapp216.pdf
  - **Correcting Single-Event Upsets Through Virtex Partial Configuration**
- Xapp138.pdf
  - **Virtex FPGA Series Configuration and Readback**