Radiation Tolerant DDL SIU Status Report

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Preamble

Prototype DDL cards

- FPGA: Altera APEX-E (EP20K60E, 160 kgates - 0.18 μm)
- Amongst all consequences of radiation, one is really problematic: the loss (or corruption) of the device configuration (= configuration cell changes its state due to high-energy particle interacting with the device)
- Radiation tests have shown that we should expect 1 loss of configuration in 1 of the 400 DDL SIUs every hour

New DDL card

- 3 different solutions have been discussed (Altera Cyclon, Xilinx Virtex, Actel ProASIC+)
- The one based on **Actel ProASIC+** has been selected
  - 0.22 μm flash-based CMOS process

Actel ProASIC+

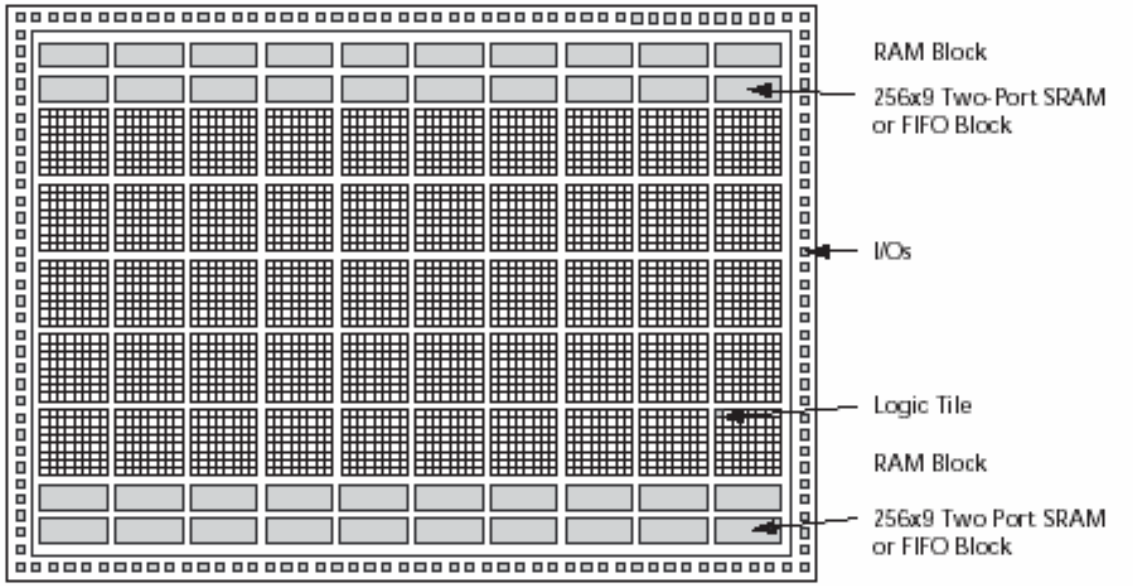
Bright side

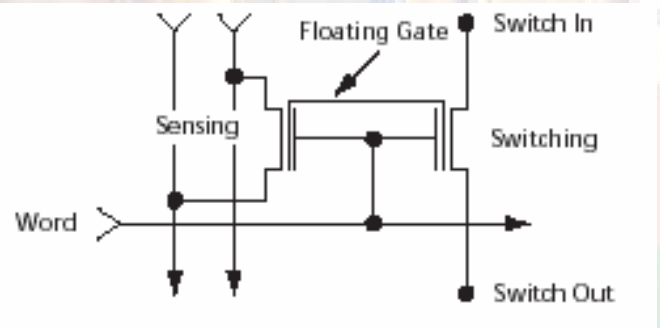
- Irradiation tests are encouraging
- Capacity: no problem to fit the DDL SIU in. (PQFP 208 pins 75k to 1Mgates)
- Lower power consumption
- Instant-on device (no configuration at power-on)
- No external device needed for storing the configuration

Not so bright…

- Different architecture
  - Learn the peculiarities of the ACTEL software tools
  - Timing-critical modules to be re-engineered (framing/de-framing @ 110 MHz)
  - Less internal resources (e.g. high-speed global network)
  - Less complex logic elements
- Special voltage (+16 V and -13.8 V) required to reload configuration
  - remote configuration is not supported

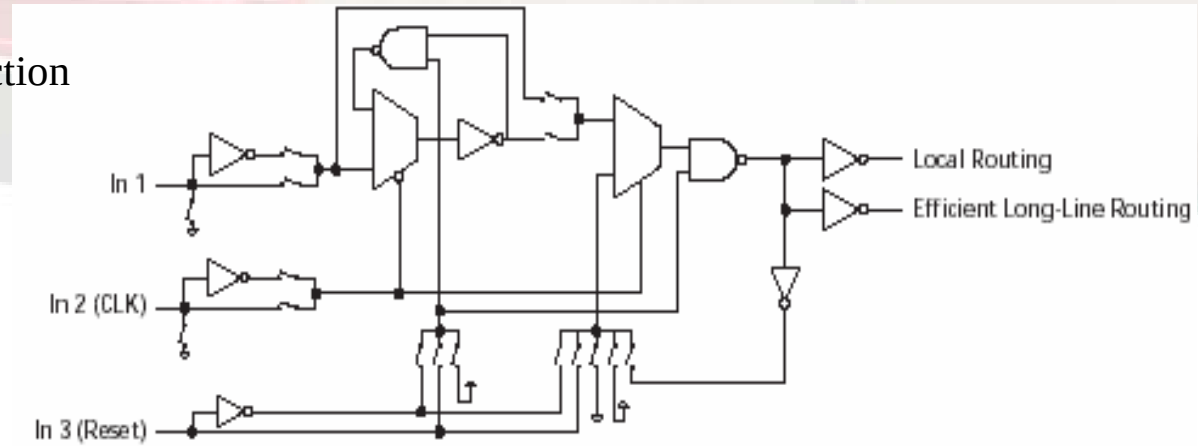
ProASIC+ Architecture





- Smaller die size = less power consumption
- Intrinsically hard switches (flash vs. SRAM)

- Any 3-input, 1-output logic function (expect 3-input XOR)
- Register/Latch with clear or set (enable requires additional cell)



The Future

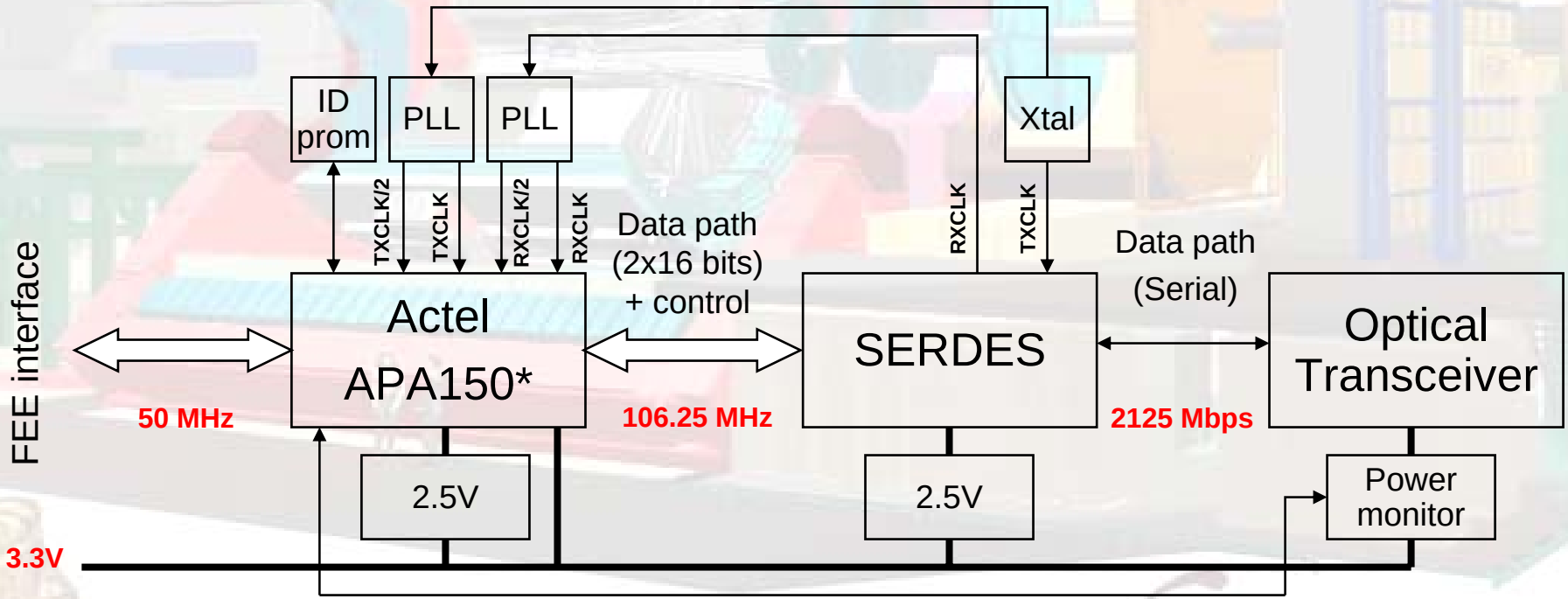
Actel ProASIC3 (3rd generation)

- 0.13 μm Flash-based CMOS process
- Higher performance, lower power consumption
- Improved global network supporting up to 18 global signals
- Six clock conditioning circuits, one of them with PLL
- High-speed I/Os supporting different standards with registers in the I/O cell
- On-chip Flash ROM (good for identification)
- Pin compatible with existing ProASIC+ devices

Not available yet

☹

Hardware

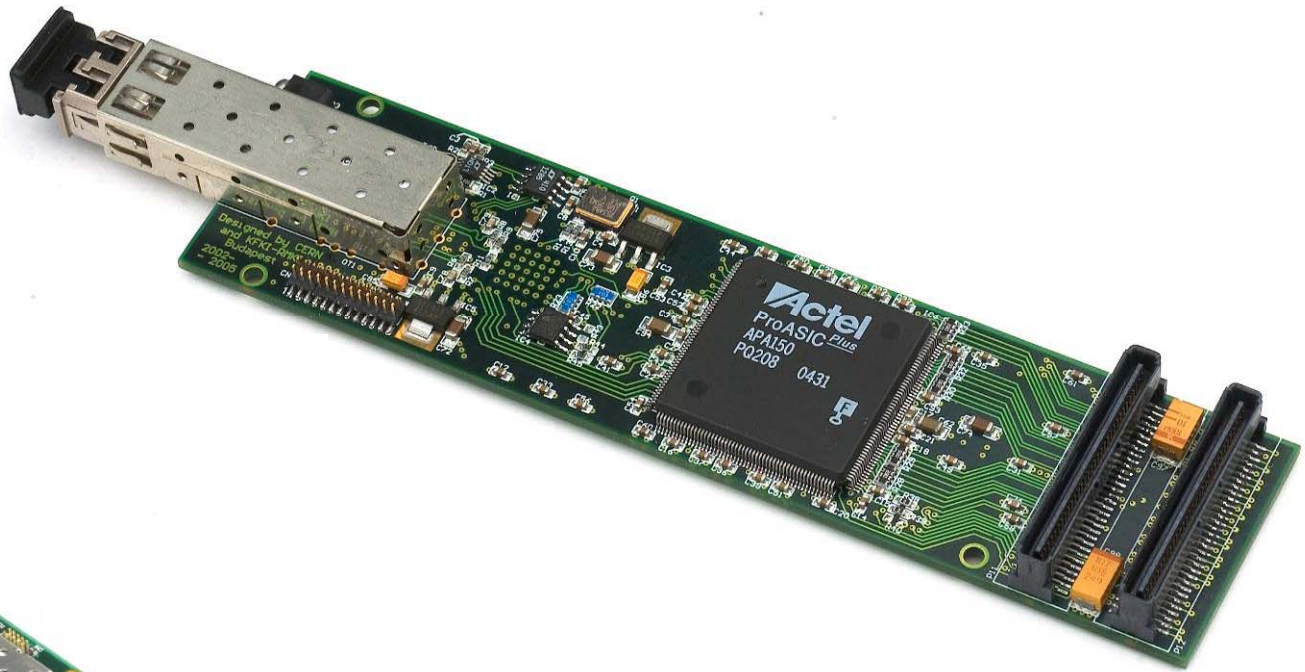


* Possible migration to A3P250

Hardware

100 % backward compatible with the existing DDL cards

- same pin-out, voltage levels and mechanical size



Firmware (1/2)

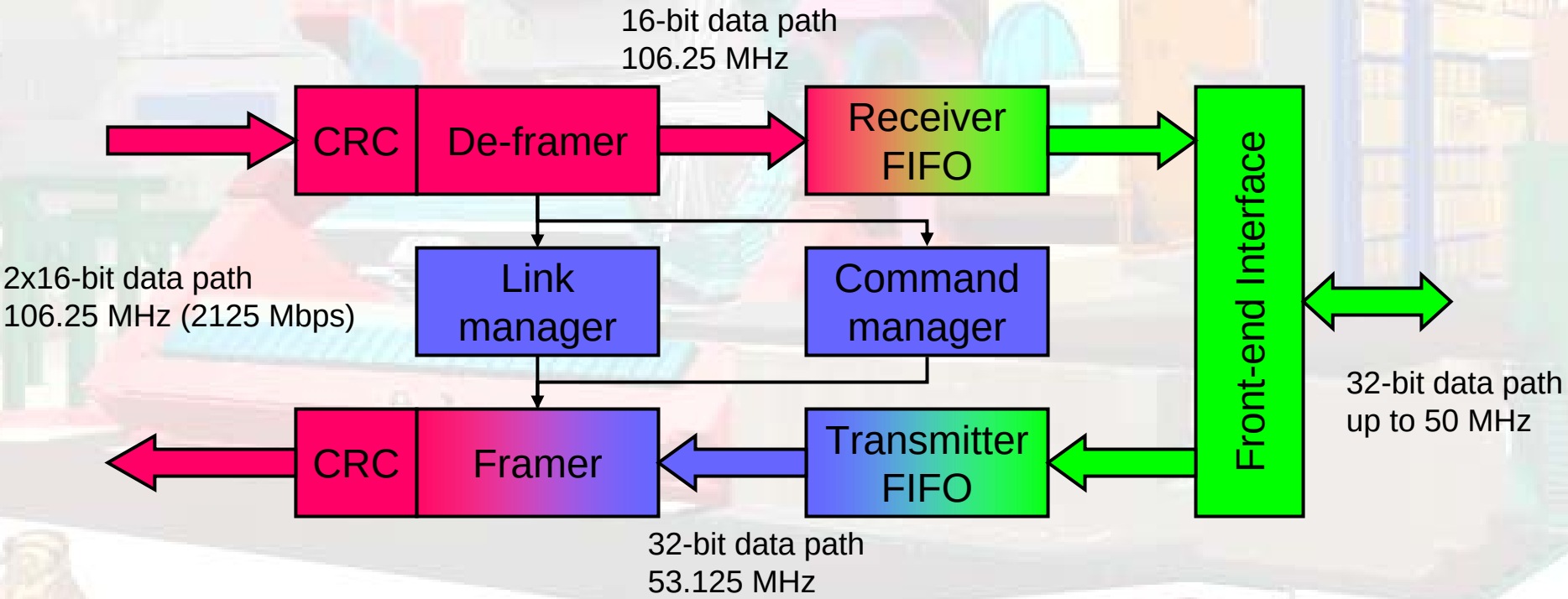
Difficulties

- Read port of the internal FIFO memory is slow
  - link clock must be divided using PLLs
  - clock boundary crossing (from TXCLK/2 to TXCLK)
- Too many clock signals and domains
  - five clock signals, including two high-speed clocks toggling at 110 MHz
  - only four global clock lines are available in the device
- Dual-port FIFO flags are generated asynchronously (glitches)

Solutions

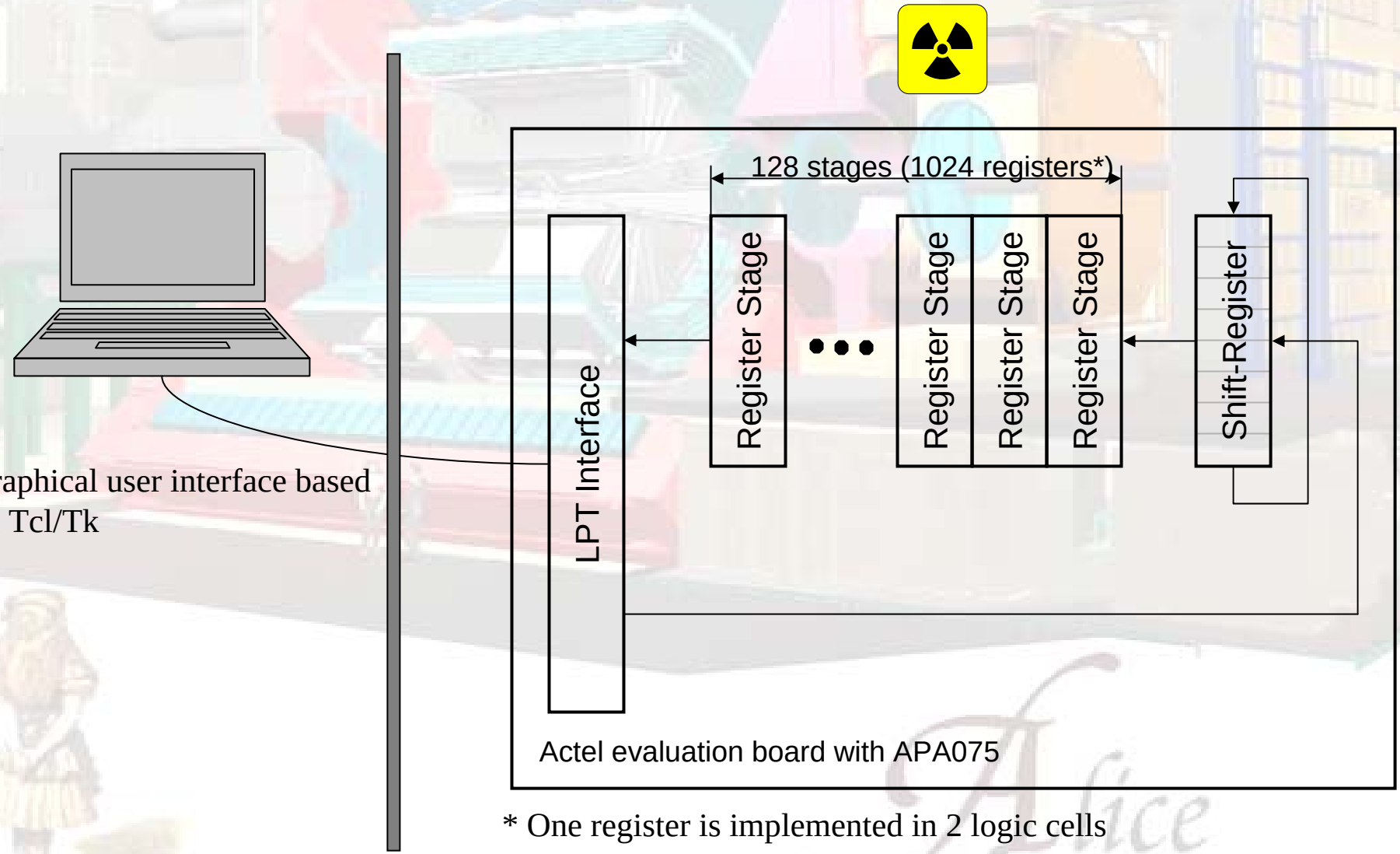
- Use internal PLL to generate TXCLK/2
  - it fixes the delay between TXCLK and TXCLK/2 clock signals
  - it allows timing budget calculations
- Improve the receiver logic to run at 110 MHz
  - it eliminates the need of the divided clock
- Custom dual-port memory has been designed

Firmware (2/2)



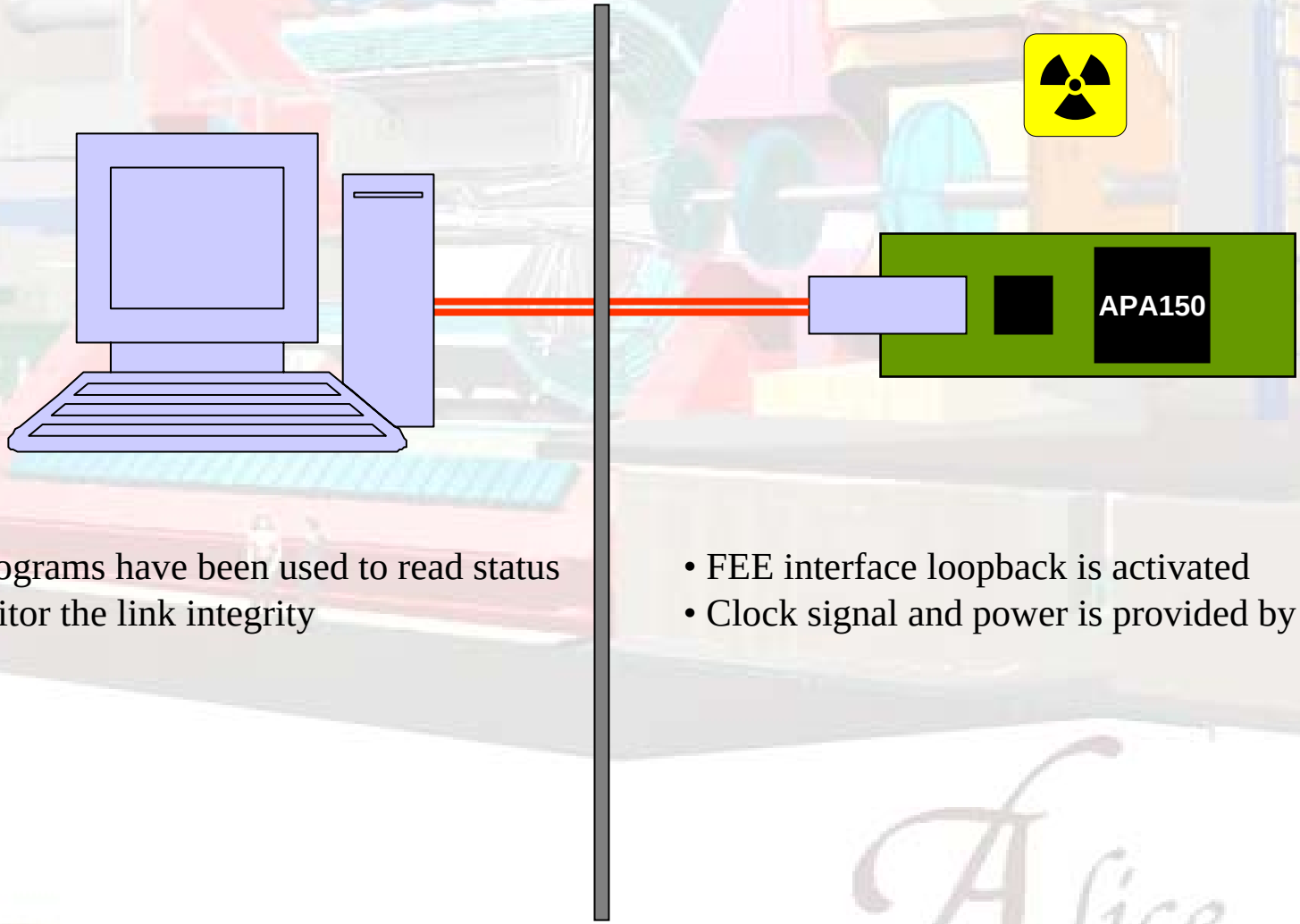
Legend:
Link clock domains (RX and TX)
Divided link clock domain
Front-end clock domain

Radtol Tests – Testbed no. 1



* One register is implemented in 2 logic cells

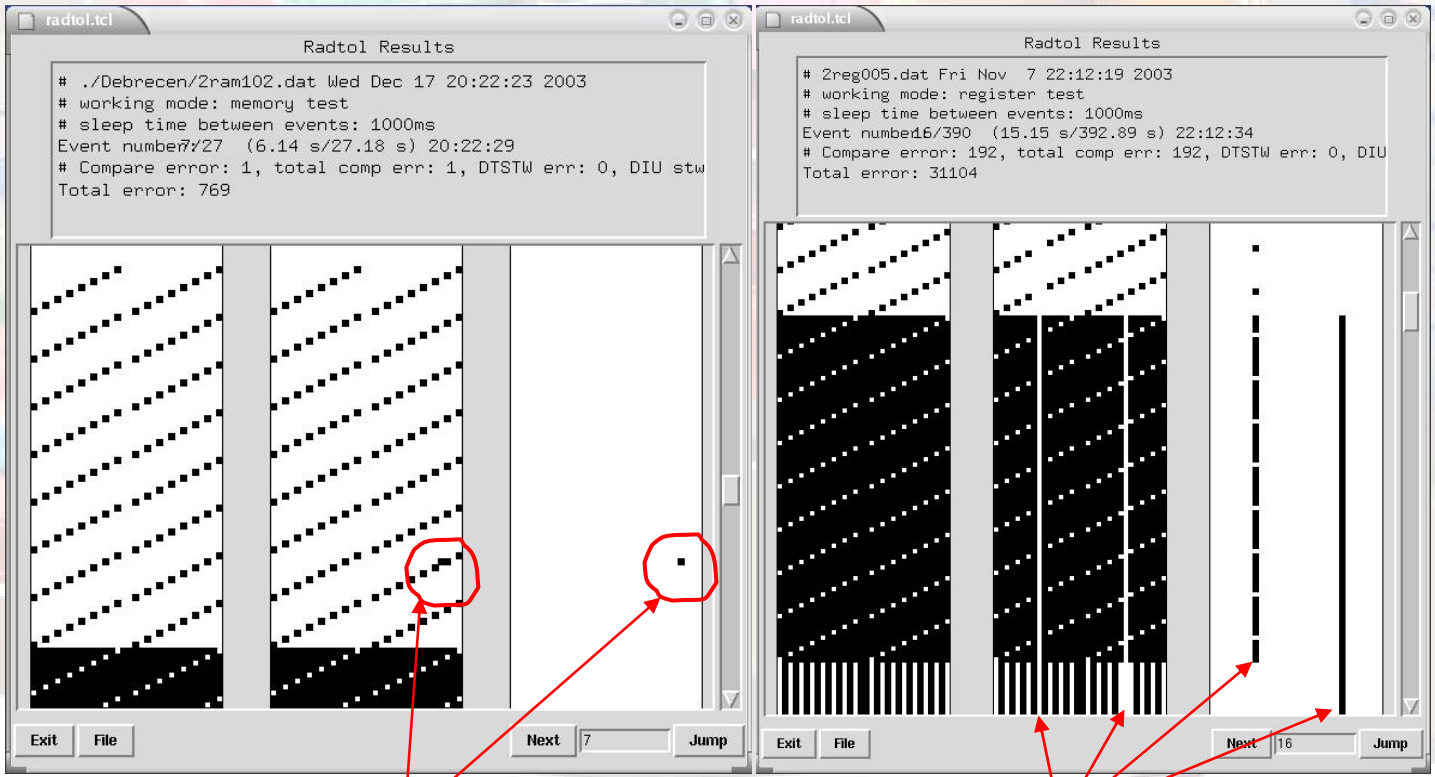
Radtol Tests – Testbed no. 2



- RORC programs have been used to read status and to monitor the link integrity

- FEE interface loopback is activated
- Clock signal and power is provided by external source

Radtol Tests – Software



Bit-flip

Configuration error

Radtol Tests - Results

May 2004, TSL, Uppsala, Sweden

- Tests were done using the evaluation board (APA075)
- Proton beam @ 171, 94 and 48 MeV
- No configuration loss

June 2004, ATOMKI, Debrecen, Hungary

- Tests were done using the evaluation board (APA075)
- TID tests with Co^{60}, dose rate of approx. 20 krad/h
- No problem up to 12 krad, when the device stopped functioning
- After 1 hour at room temperature the device started to work (annealing)

March 2005, ATOMKI, Debrecen, Hungary

- Tests were done using both the evaluation board and the new SIU (APA150)
- Neutron beam with the energy < 15 MeV
- No errors have been detected on the evaluation board ($5*10^{10}$ n/cm^2)
- One error on the SIU provoked link down after 22 minutes (10^{11} n/cm^2). It could be fixed by cycling the power of the card.

Status

Hardware

- The schematic was finalized after Actel released the information about the migration from ProASIC+ to ProASIC3
- The PCB has been designed to be compatible with both families
- Two prototype boards have been manufactured
- No design error has been found so far

Firmware

- Modules have been ported from the present DDL firmware
- Timing critical modules are being reengineered and optimized
- Complete firmware is being simulated and then tested on real hardware
- DDL transactions are being tested using the RORC utilities
- Long term tests are being executed using DATE

Planning

- New irradiation tests using the fully functional SIU firmware in April
- Climate chamber tests in April – May
- Production Readiness Review (PRR) in May
- Production of small series for TPC tests at Point 2