Front-End Card Interface of the RCU

- Readout network (ALTRO Interface)
- Local Slow Control

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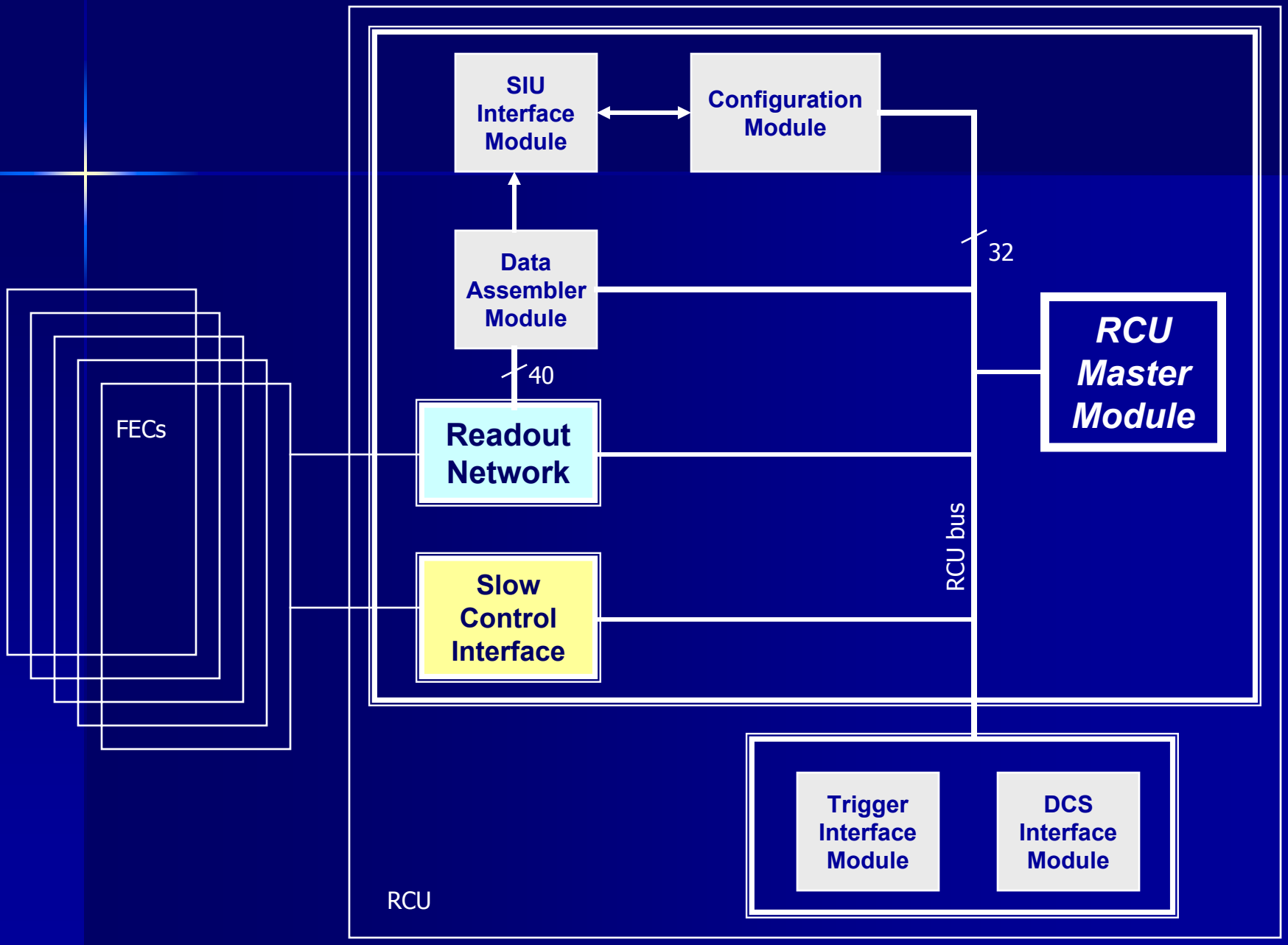
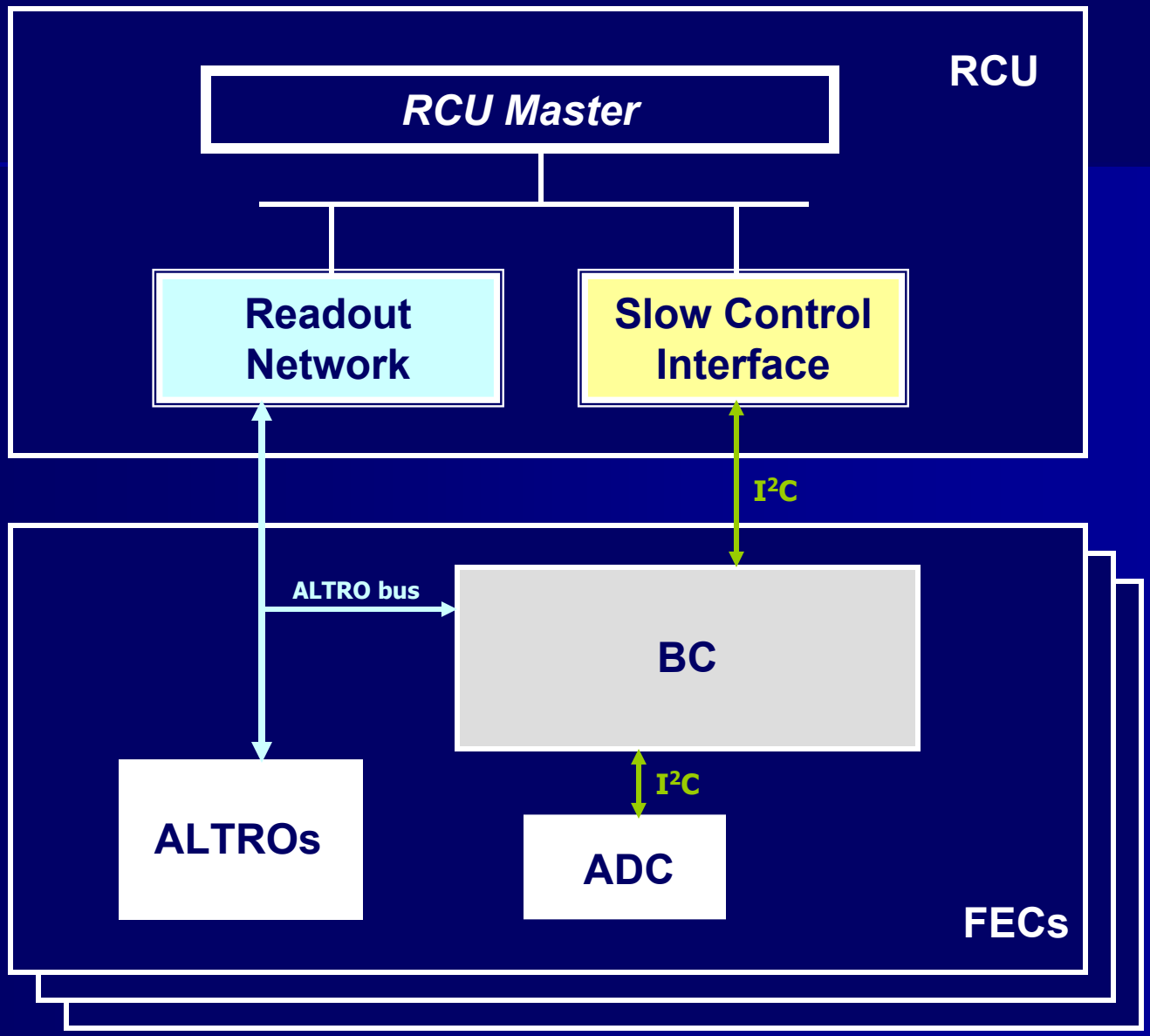
RCU: functional overview



Block diagram

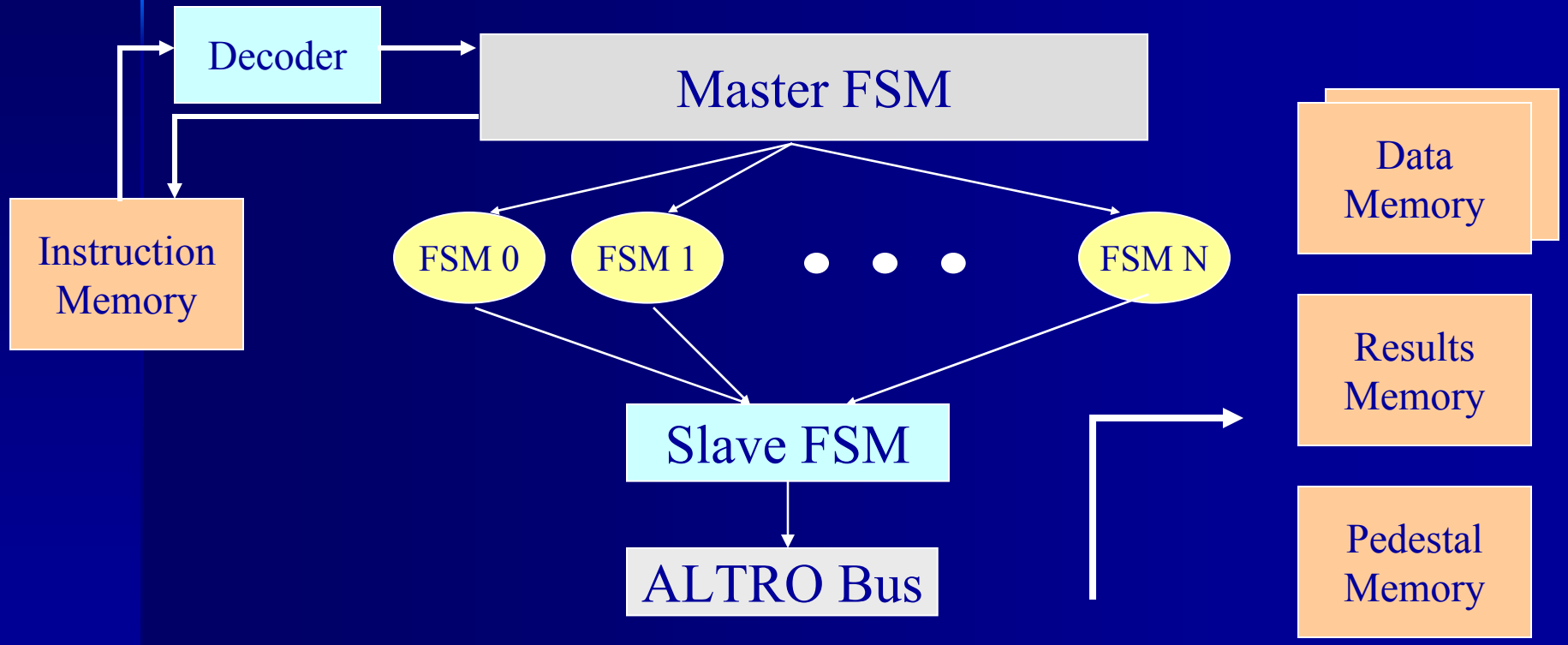


Readout network

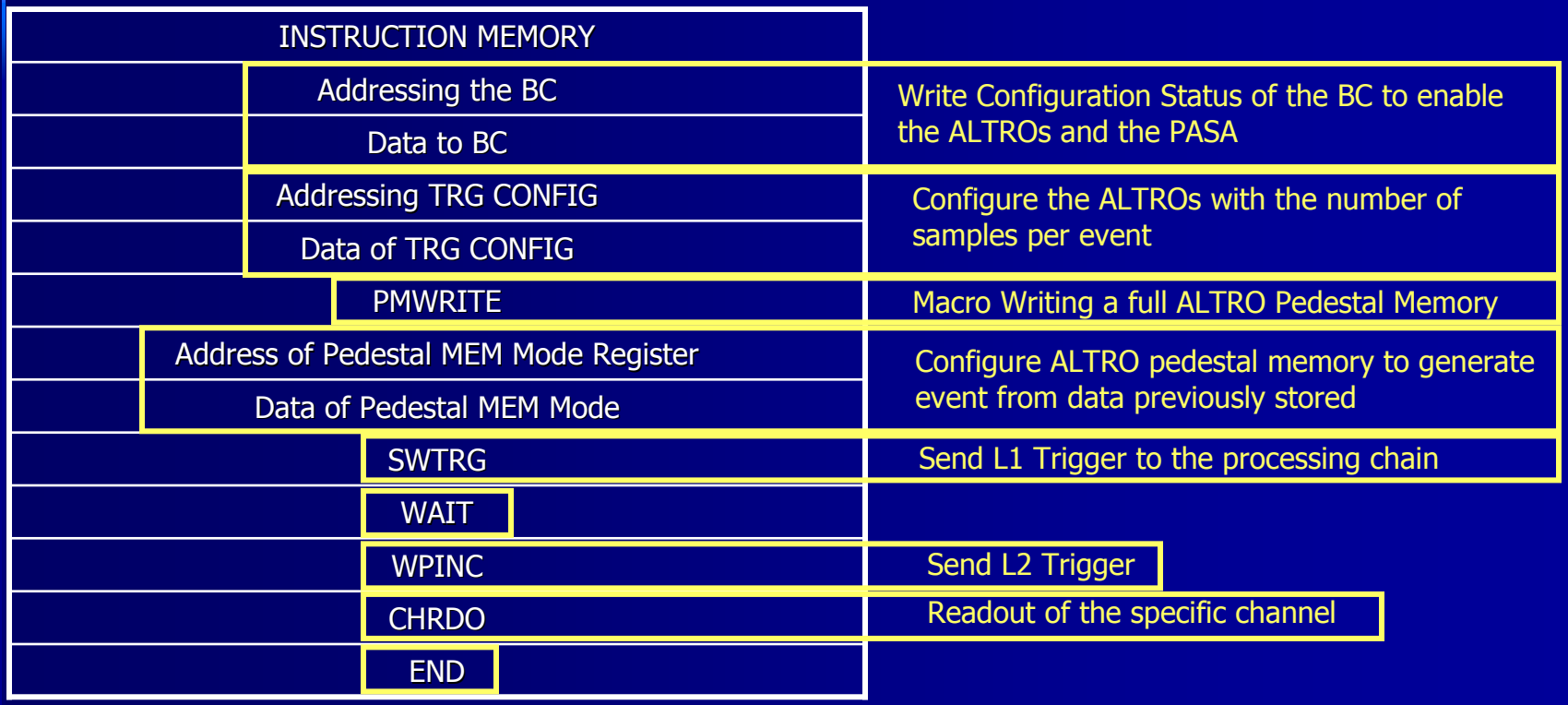
1. *Provides communication between the RCU and the ALTRO chips for Configuration and Readout.*
2. *Provides a simple and direct interface, as slave, to the DDL-SIU, DCS -Trigger Board and the RCU master.*

- 4 different memories
  - *INSTRUCTION MEM* -> ALTRO commands and macros
  - *DATA MEM* -> Double "ping-pong" data buffer. One channel black event/buffer
  - *PEDESTAL MEM* -> Replica of ALTRO Ped. Memory. Used for both test and configuration purposes
  - *RESULTS MEM* -> Stores value of registers read from ALTRO
- Decoder
- Counter Table
- FSM

Readout Network: *FSM Hierarchy*



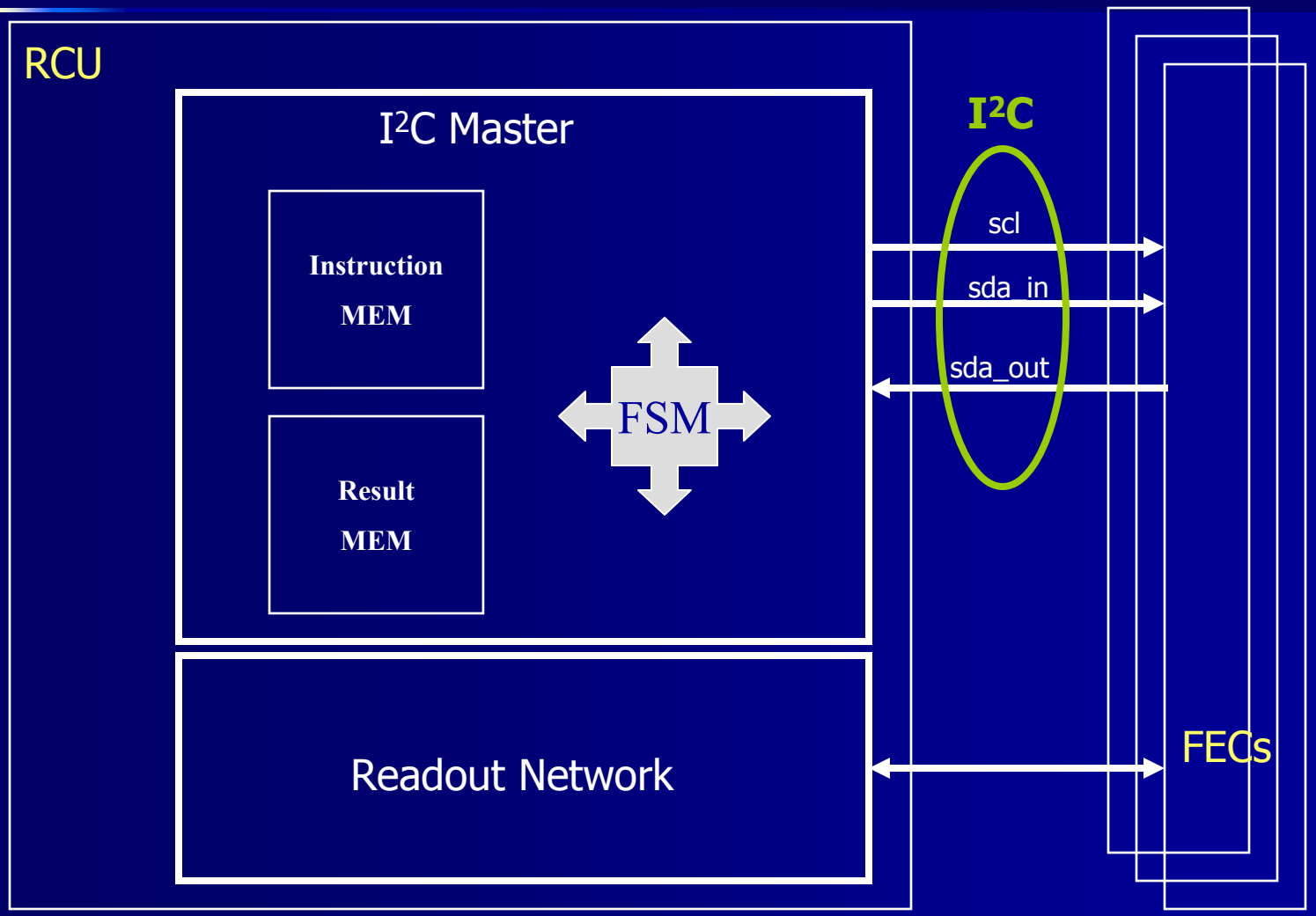
Readout network: *RCU Macro Instructions*
Sequence used in hardware test



Local Slow Control

- Dedicated bus connection RCU – BC (I^2C Protocol)
- Configure the power state of all FECs
- Monitor power and temperature
- Interrupts
- Read status parameters (errors)

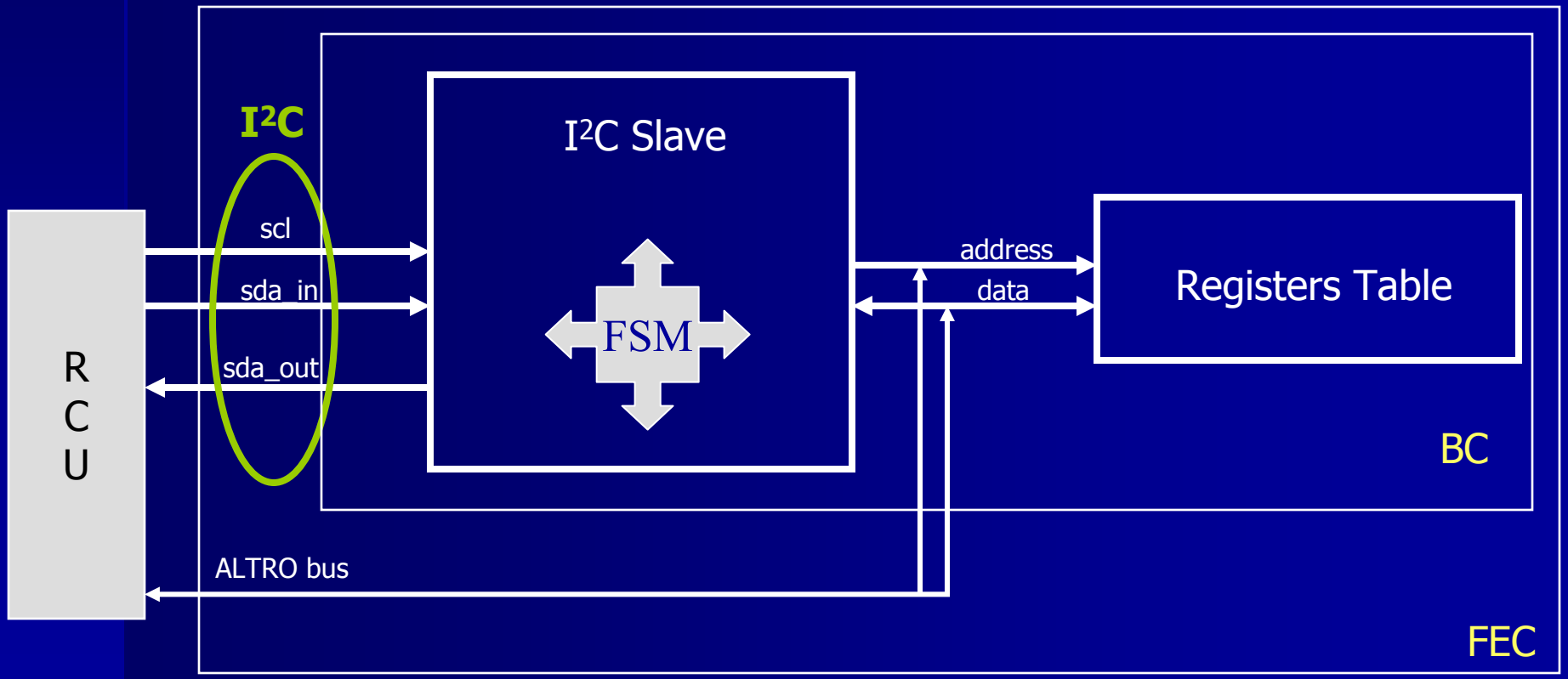
Slow Control: *block diagram*
RCU



Slow Control: *block diagram*
Board Controller (FEC)

RCU is able to

- write and read the Register Table
- send commands



Registers Table

Threshold Registers

Value from the ADC

Reg. Addr	Mnemonic	Reg. Name	Width	Acc. Mode	Allow Bcast	Meaning
01	T_TH	Temperature Thr.	10	R/W	Y	Maximum Temperature Threshold
02	AV_TH	AV threshold	10	R/W	Y	Minimum Analog Voltage Threshold
03	AC_TH	AC threshold	10	R/W	Y	Maximum Analog Current Threshold
04	DV_TH	DV threshold	10	R/W	Y	Minimum Digital Voltage Threshold
05	DC_TH	DC threshold	10	R/W	Y	Maximum Digital Current Threshold
08	TEMP	Temperature	10	R	N/A	Temperature Value
09	AV	Analog Voltage	10	R	N/A	Analog Voltage Value
0A	AC	Analog Current	10	R	N/A	Analog Current Value
0B	DV	Digital Voltage	10	R	N/A	Digital Voltage Value
0C	DC	Digital Current	10	R	N/A	Digital Current Value
10	L1CNT	L1 Counter	16	R	N/A	Number of L1 Trigger Received
11	L2CNT	L2 Counter	16	R	N/A	Number of L2 Trigger Received
12	SCLKCNT	Sampling clk counter	16	R	N/A	Sampling Clock counter
13	DSTBCNT	Data Strobe Counter	8	R	N/A	Number of Data Strobe in the last Read - Out
14	CSR0	Configuration Status 0	14	R/W	Y	Interrupt – Mask Register
15	CSR1	Configuration Status 1	14	R	N/A	Error Status Register
16	CSR2	Configuration Status 2	16	R/W	Y	Card Configuration Status Register

Registers Table, commands

Reg. Addr.	Mnemonic	Reg. Name	Width	Acc. Mode	Allow Bcast	Meaning
18	CNTLAT	Counters Latch	-	W	Y	Latch L1, L2, SCLK counters
19	CNTCLR	Counters Clear	-	W	Y	Clear L1, L2, SCLK counters
1A	CSR1CLR	Config Status Reg1 Clear	-	W	Y	Clear Error Status Register
1B	ALRST	ALTRO Reset	-	W	Y	Reset all the ALTROs
1C	BCRST	BC Reset	-	W	Y	Set default values in registers of BC
1D	STCNV	Start Conversion mADC	-	W	Y	Start Conversion / Readout Monitor ADC

Registers Table

Reg. Addr.	Mnemonic	Reg. Name	Width	Acc. Mode	Allow Bcast	Meaning
01	T_TH	Temperature Thr.	10	R/W	Y	Maximum Temperature Threshold
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09	AV	Analog Voltage	10	R	N/A	Analog Voltage Value
0A	AC	Analog Current	10	R	N/A	Analog Current Value
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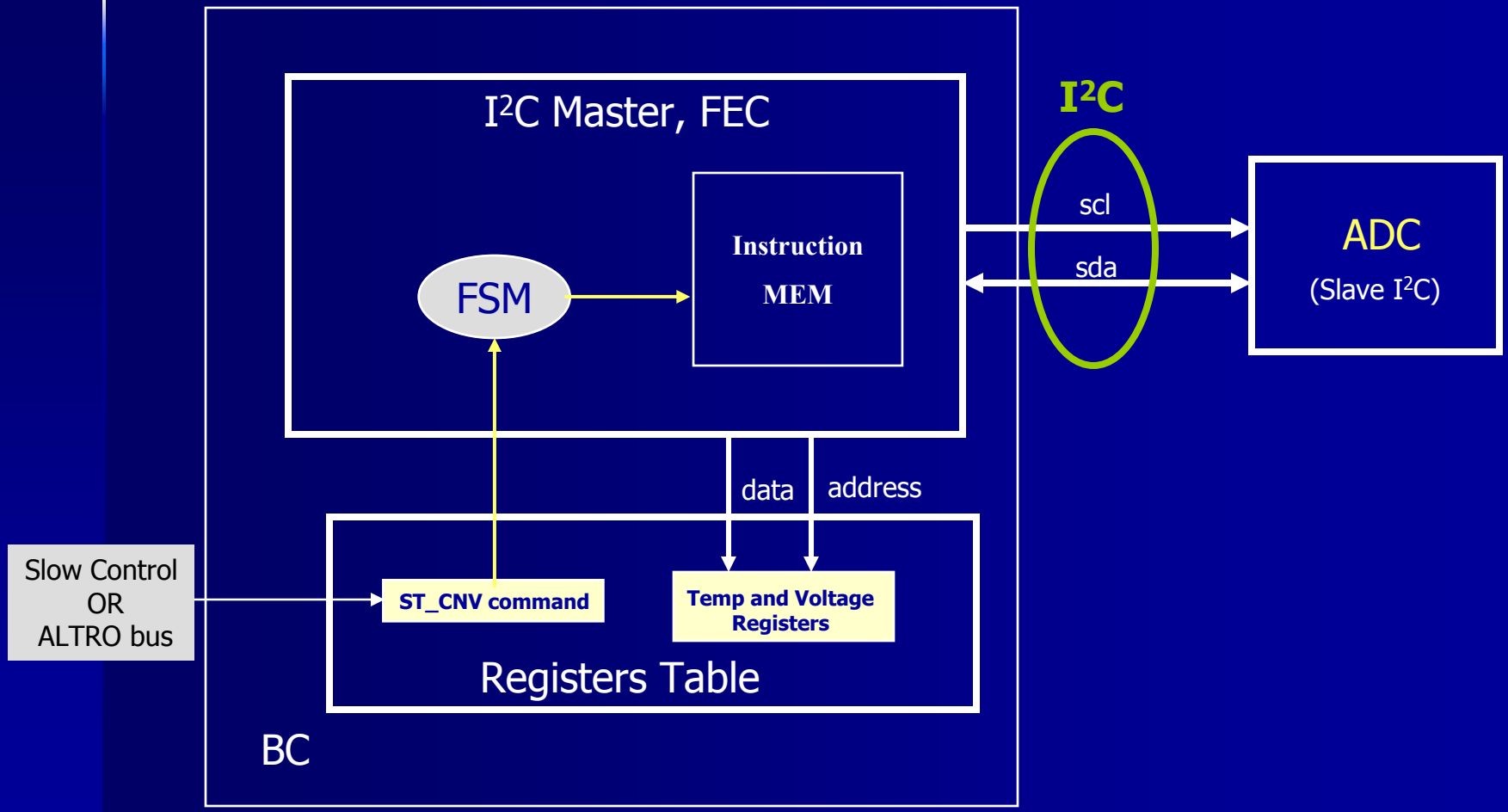
1D	STCNV	Start Conversion mADC	-	W	Y	Start Conversion / Readout Monitor ADC

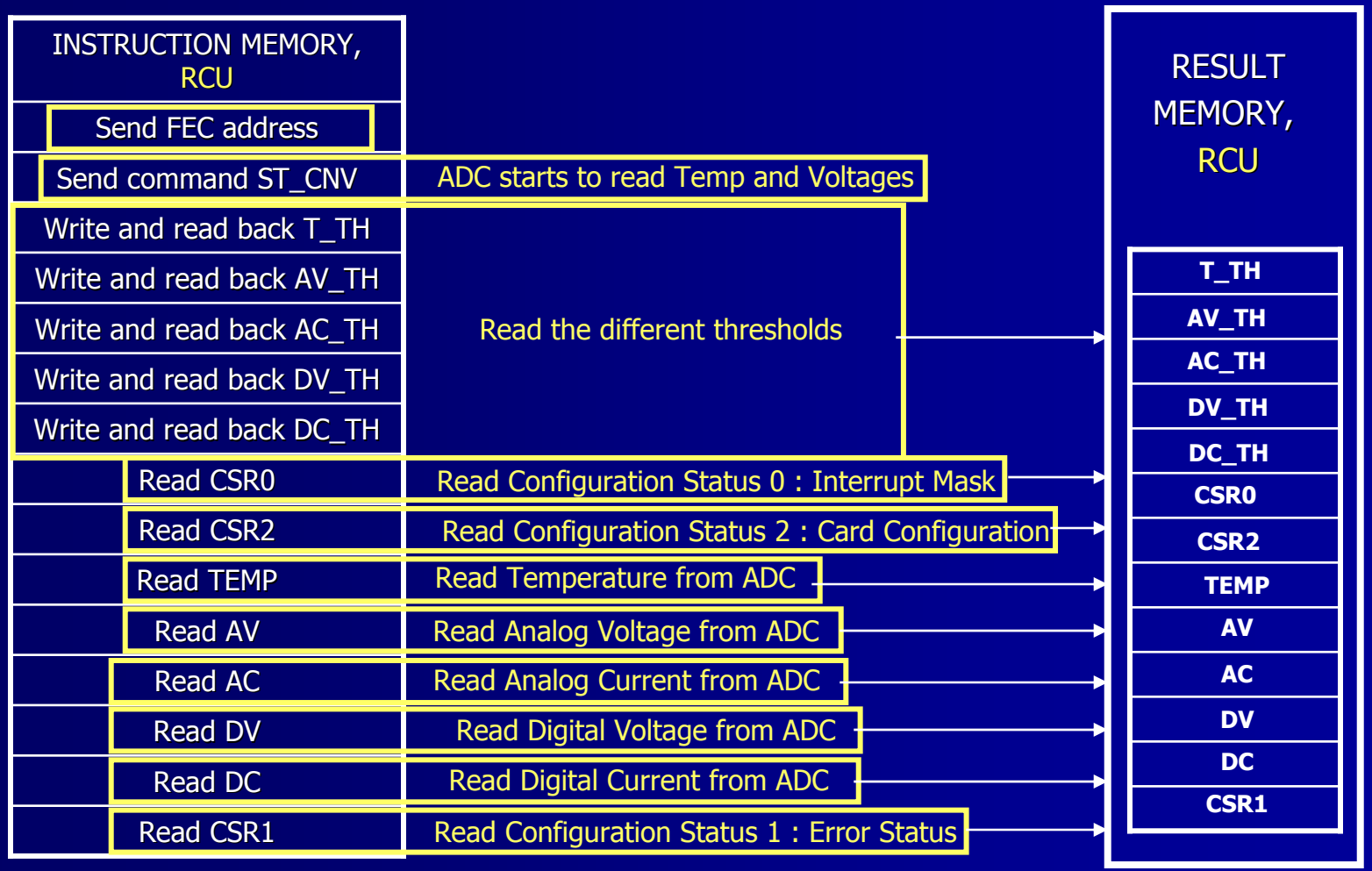
from ADC (AD7417):
4 channel ADC with an on-chip Temperature sensor

Readout of the ADC



SC Interface:

Sequence used in hardware test



Test Set - up

- Using the R&C backplane with several FECs and the new RCU board
- Status Analyzer
- Pattern generator

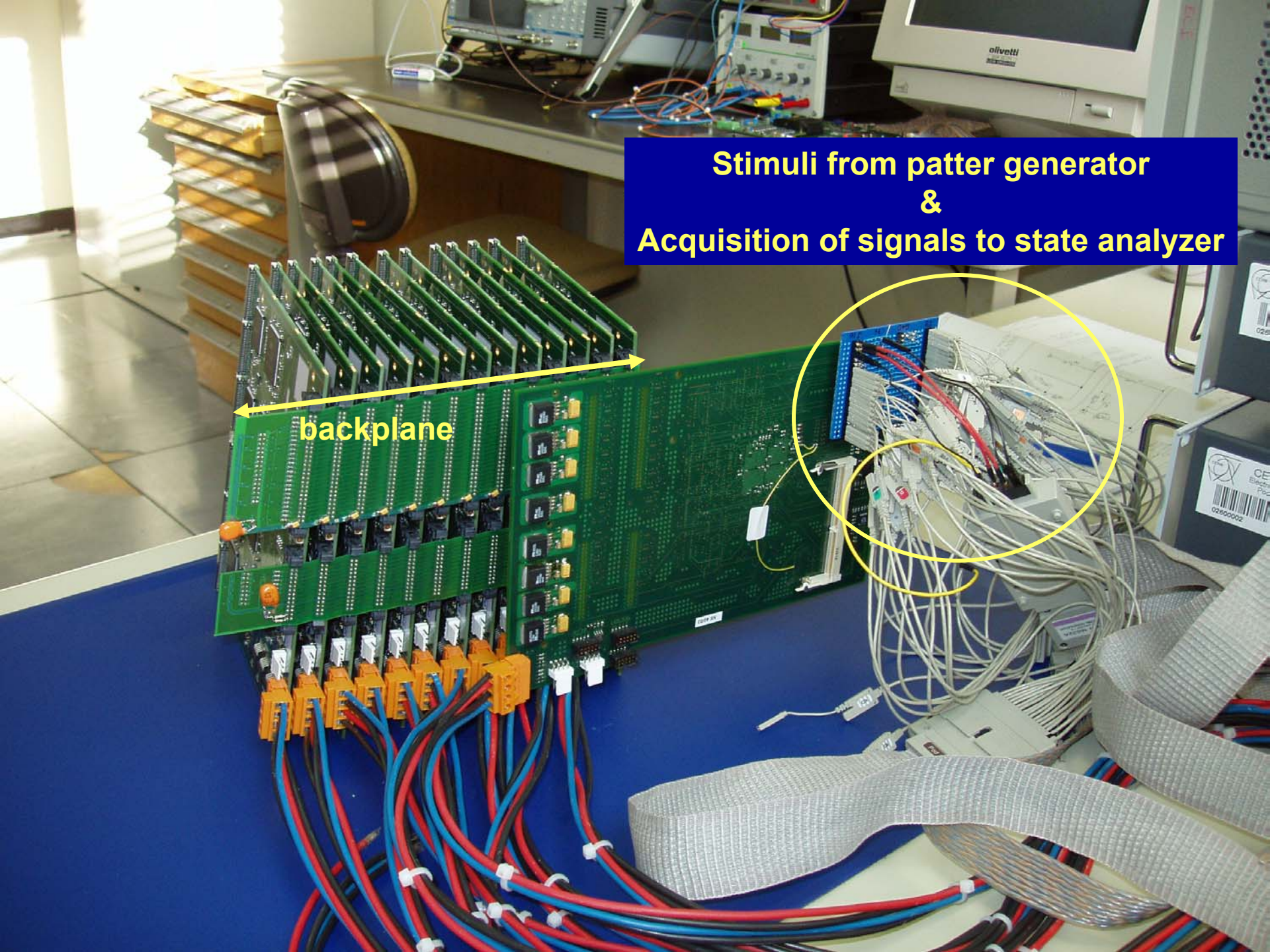
} Using an adaptor card with the CMC connectors for stimuli and probing

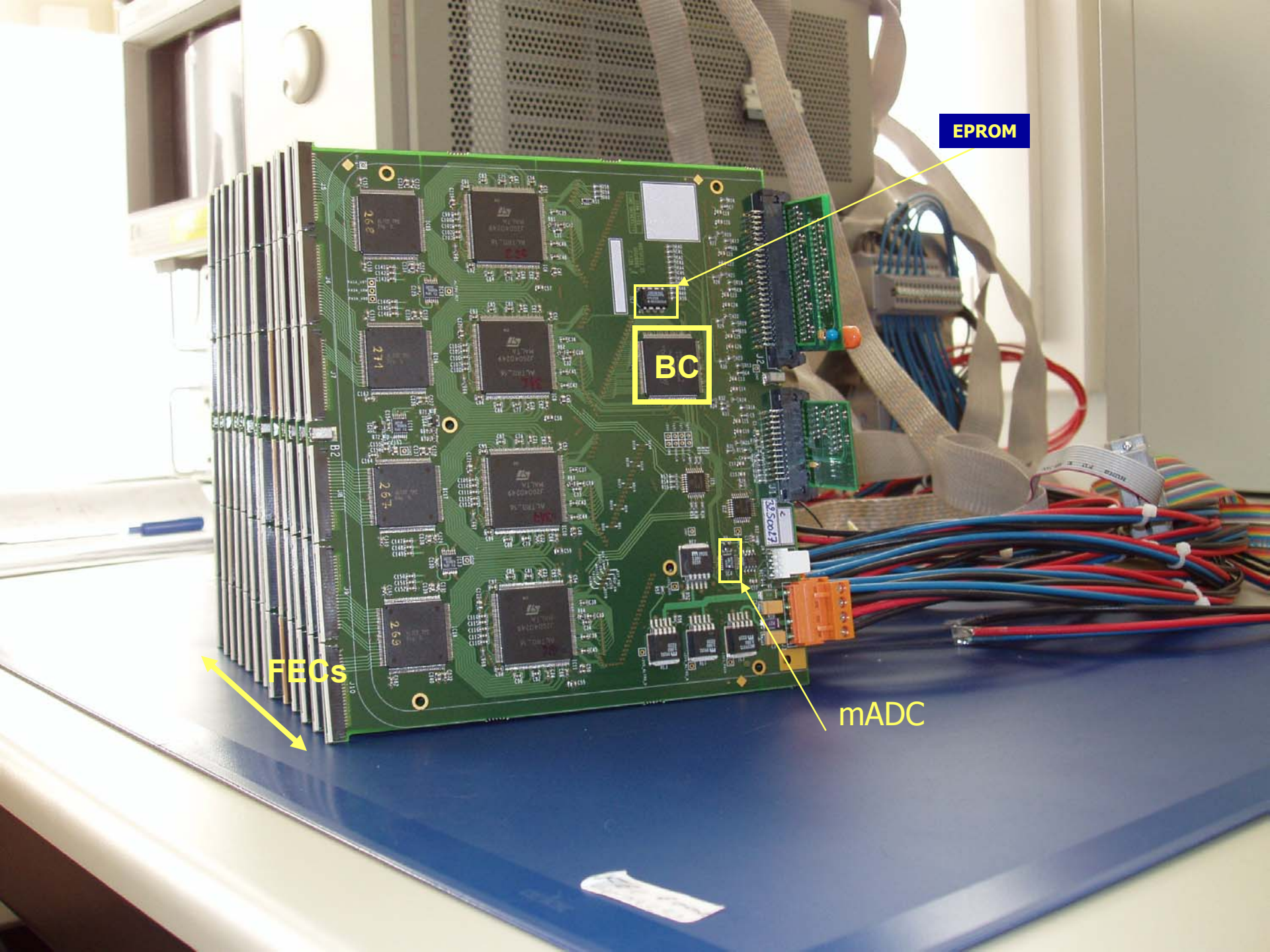
- R/O clock generated with a 40 MHz quartz oscillator
- Sampling clock is derived from r/o clk using the FPGA PLL
- Firmware uploaded using the ALTERA Byte Blaster

- Some pictures …

Connectors RCU – backplane


Adaptor Card:
RCU connectors – State Analyzer


Stimuli from patter generator
&
Acquisition of signals to state analyzer
backplane


EPROM
BC
FECs
mADC

Present Status

- Readout Network
  - Basic FEC communication functionality, tested **OK**
    - Read/Write ALTRO registers
    - Configure Pedestal Memories
    - Send L1-L2 triggers and Event Readout
  - No electrical or timing problems were detected **OK**

- Slow Control
  - Access to the Register Table to write and read from RCU, tested **OK**
  - Answers to the commands, tested **OK**

- Still to be accomplished: **X**
    - Integration with other RCU modules
    - Testing of the full chain: PASA ->DDL/DCS
    - Answers to the interrupt line from the FEC