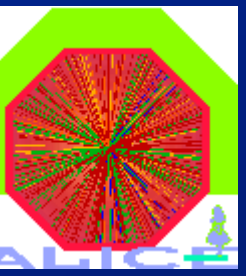
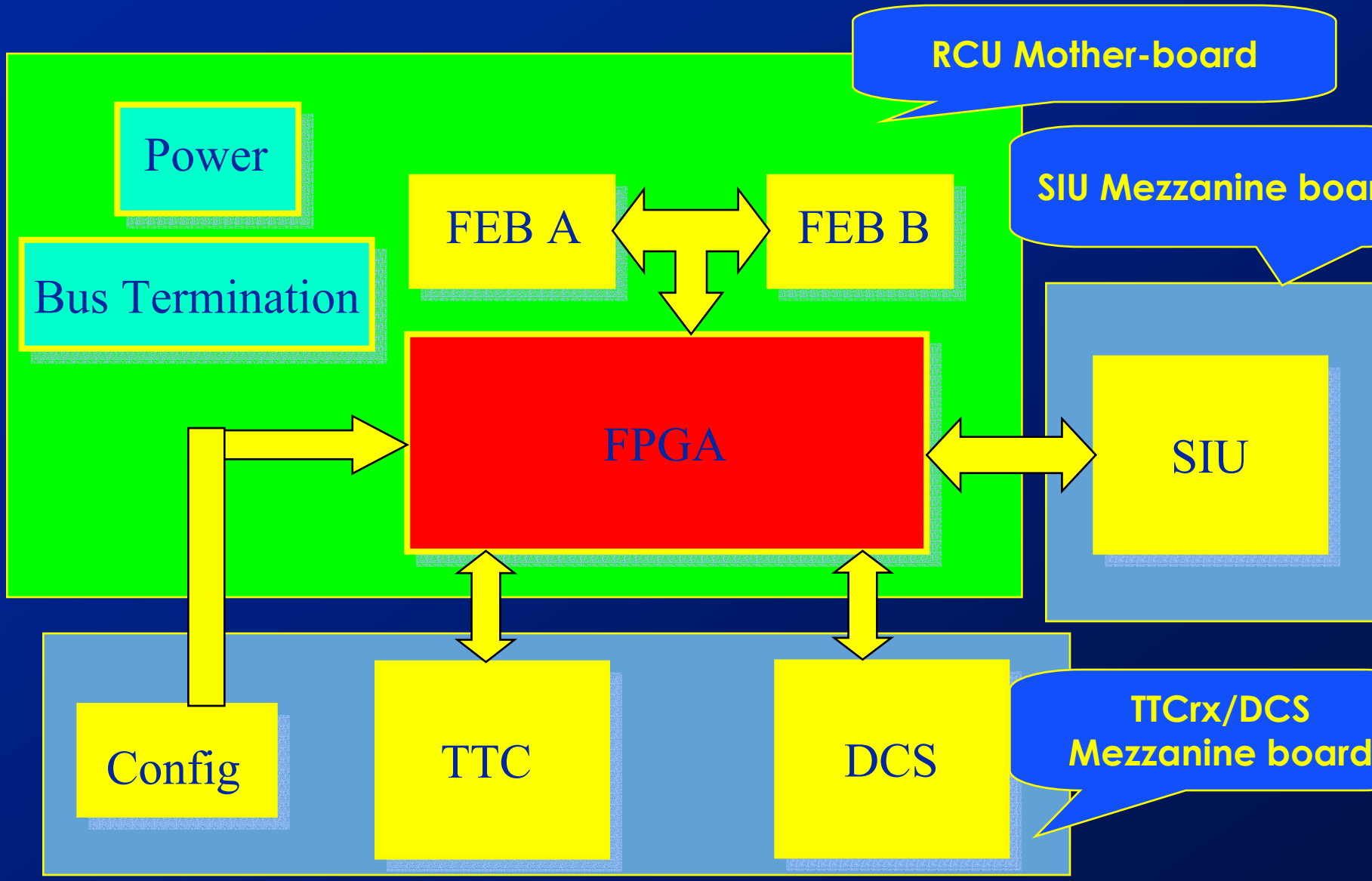
Readout Control Unit Status

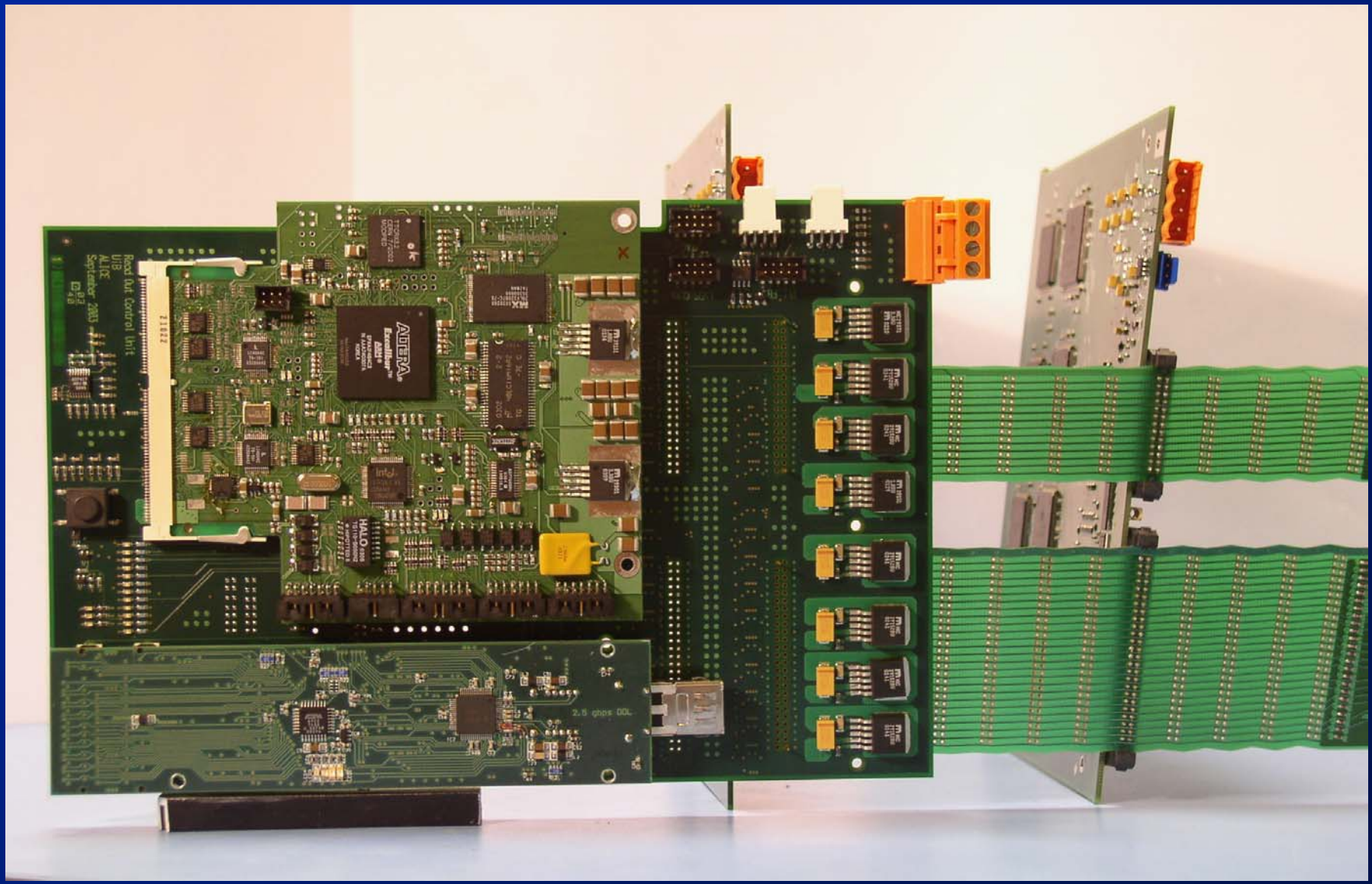
- Overview
- RCU card and sub-cards
- Status of different modules/tasks
- Milestones



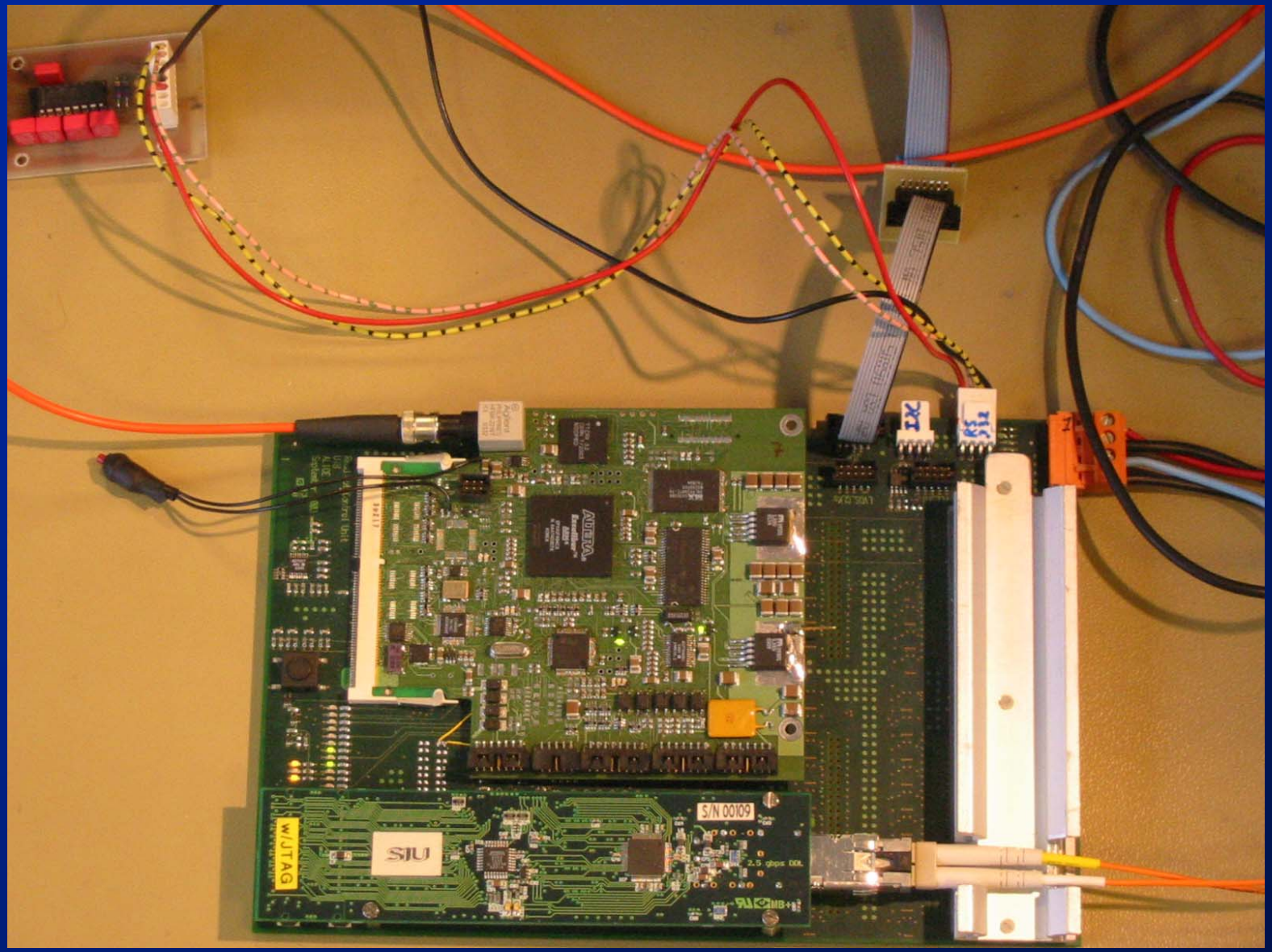
RCU Main Building Blocks Implementation



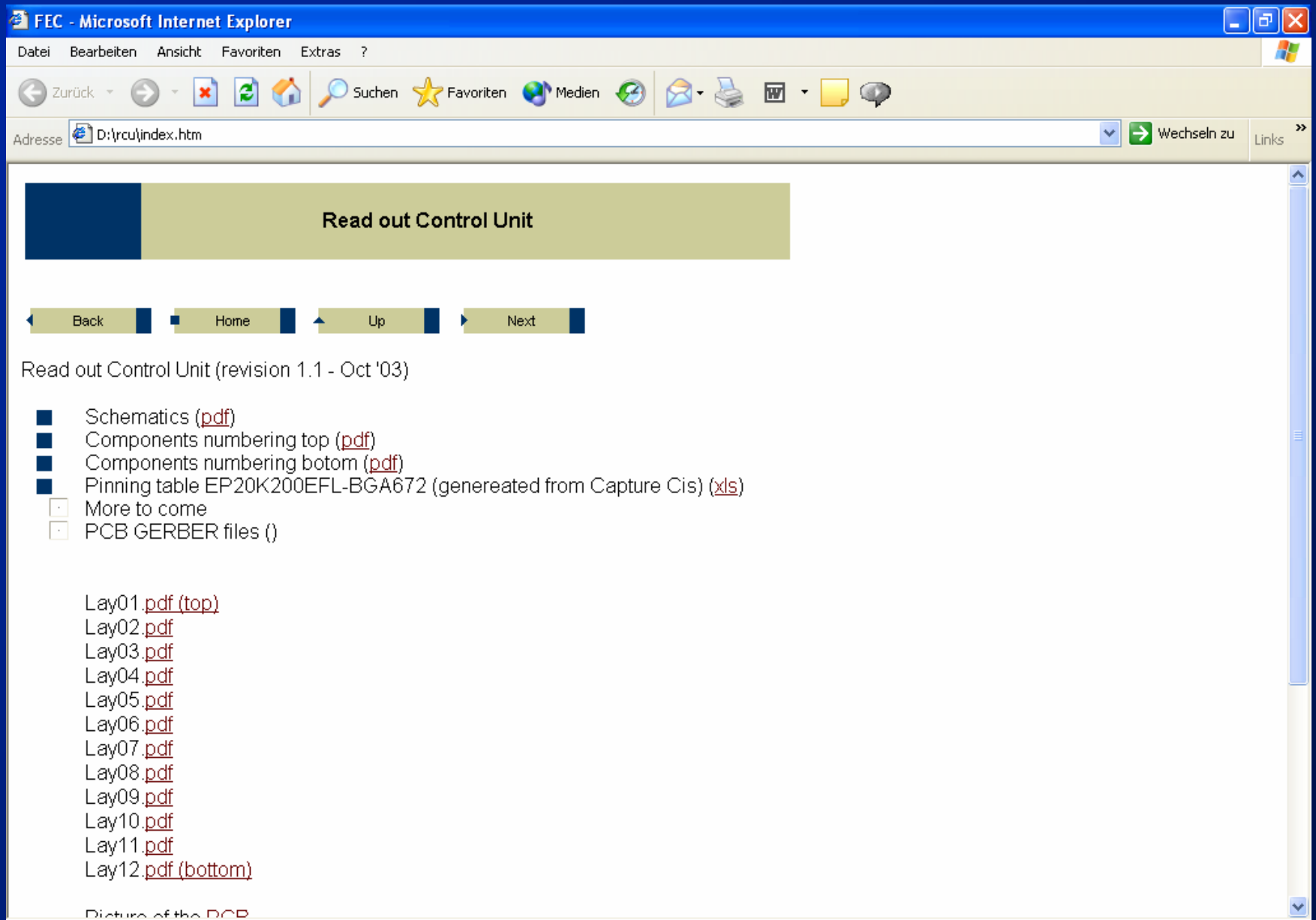
RCU card with FEC



RCU Board in the Lab



RCU-design Web Page



Internal RCU Bus - Revised

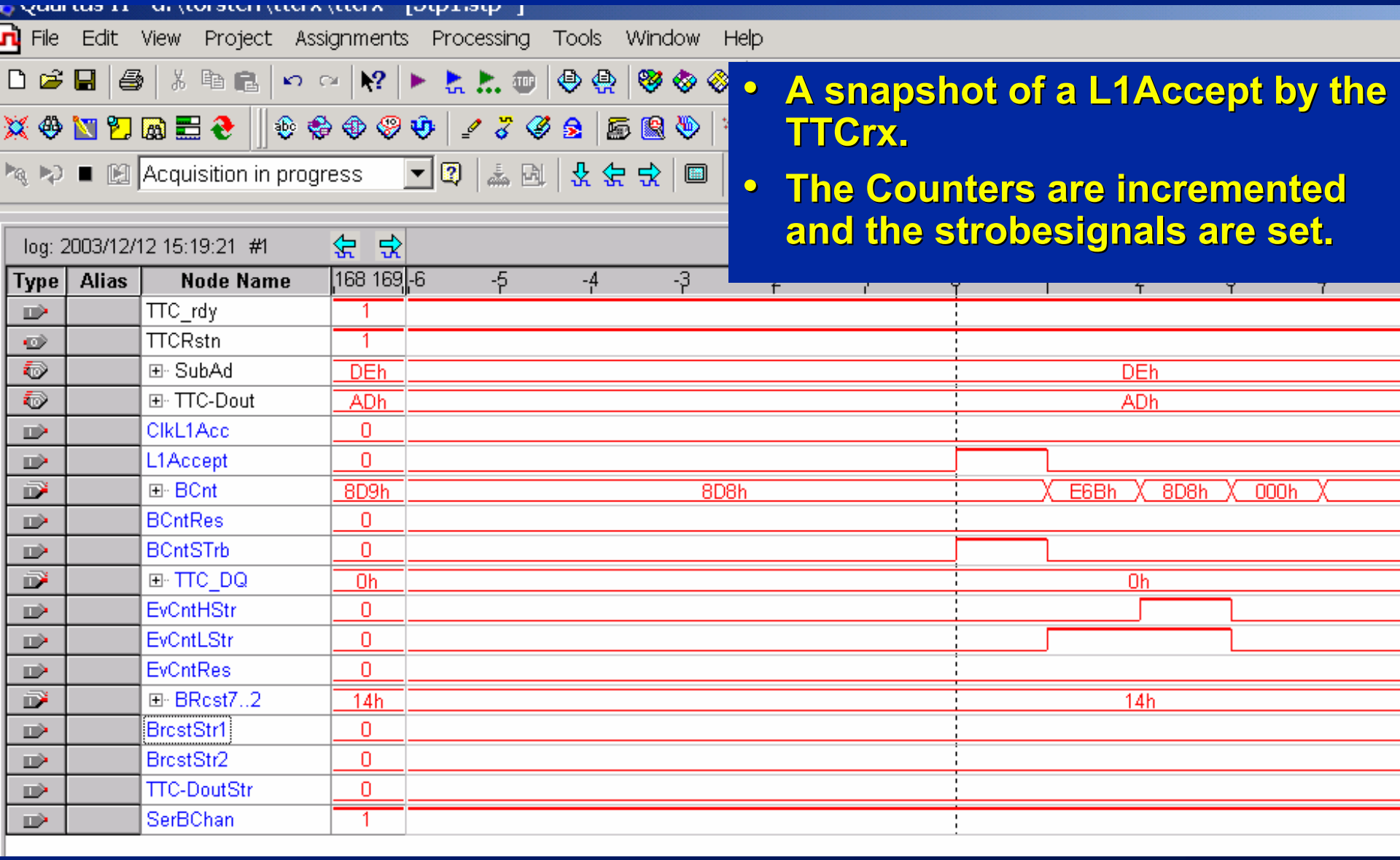
- **BUS Master Interface**

```
clock     1  --> bus clock
rst_n     1  --> bus reset
b_addr   16  --> address
b_data   32  <-> data
b_RnW     1  --> Read/Write : 1=Read/0=Write
b_cstb_n  1  --> Common Strobe: master indicates valid address/data
b_ack_n   1  <-- Acknowledge: target indicates valid transaction
```

External Communication

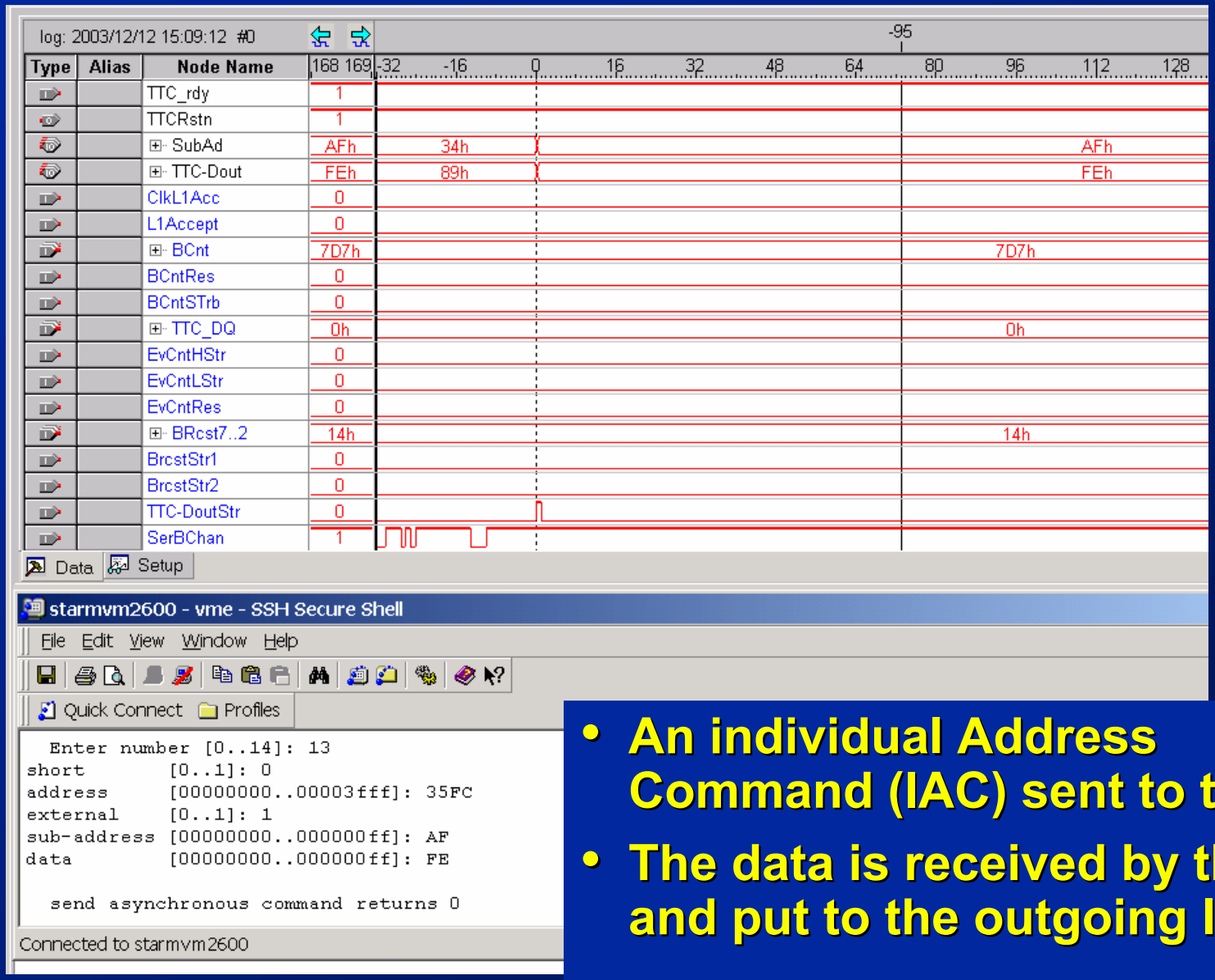
- RCU <-> DCS — DIM Server Client Scheme over ethernet
- RCU <-> Trigger — VME based test setup
- SIU <-> DIU — pRORC based Test setup
- RCU <-> FEC — Front End Card Interface

TTCrx



- A snapshot of a L1Accept by the TTCrx.
- The Counters are incremented and the strobesignals are set.

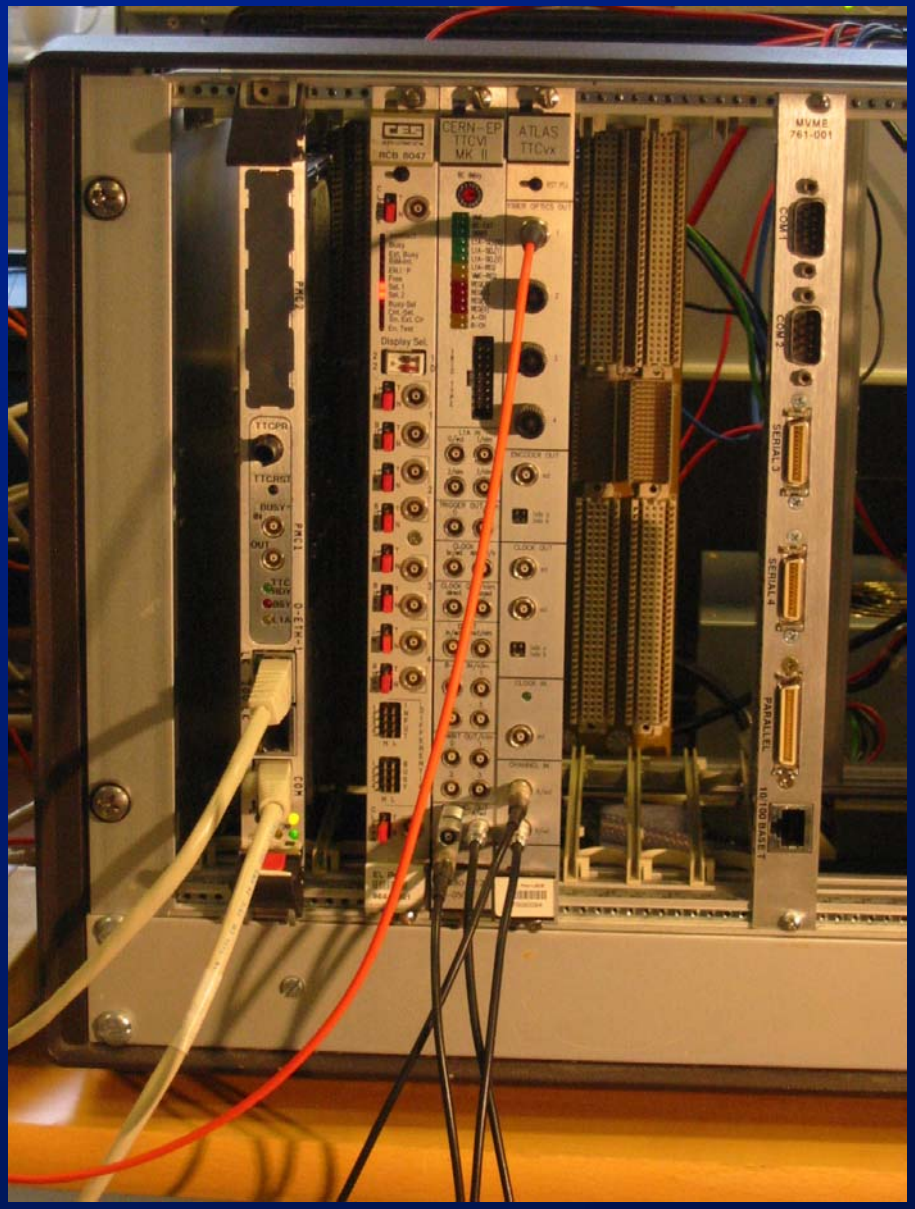
TTCrx



- An individual Address Command (IAC) sent to the chip.
- The data is received by the chip and put to the outgoing lines.

RCU <-> Trigger

- VME based test setup:
  - VP 110 CPU board running LINUX
  - TTCvi, TTCvx
- TTCrx chip communication has been tested successfully

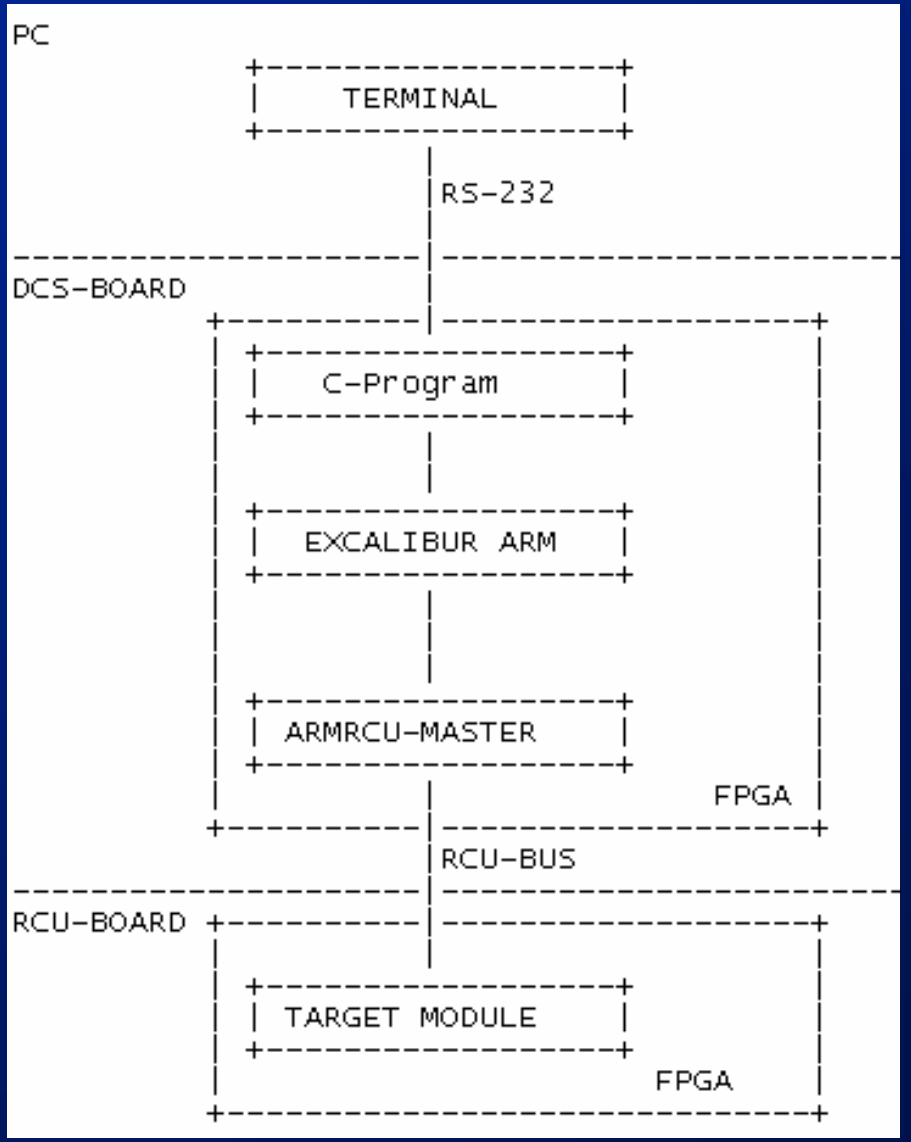


RCU <-> DiU

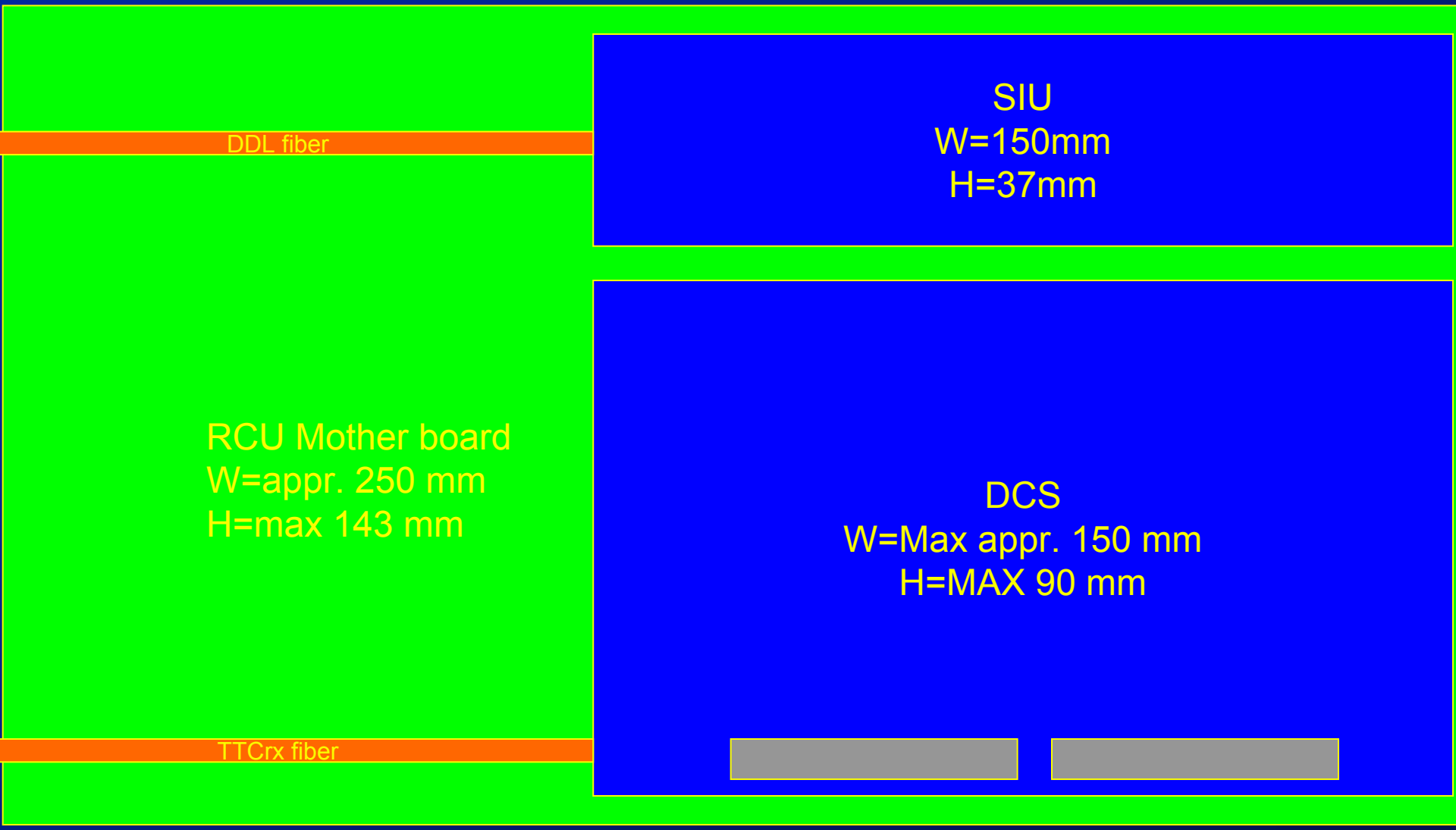
- pRORC based Test setup
- The Data Assembler Module also contains a pattern generator
- The PG can be configured and started by writing to the command register
- Bidirectional functionality implemented
- Has been successfully tested with the SIU-DIU link

A simple RCU module debugging environment

- The ARMRCU design provides a simple interface to enable the user to test RCU target modules.
- Based on the Excalibur ARM connected to a RCU master module.
- A simple C-program makes it possible to execute RCU bus transactions as reading and writing from/to a RCU target module.
- Altera SignalTap is used to capture and store signal activity from any internal device node



RCU Board Final Layout



Milestones

- **Milestones:**

• Radiation tests:	Ongoing
Oslo Cyclotron	Next Beam Time - March 2004
Uppsala TSL	Next Beam Time - March 2004
• Final PCB Layout:	June 2004
• Partial System Integration	March 2004
• Beam Test (3 RCUs)	May 2004
• Qualification of the final design	October 2003-May 2004
• Production of the final prototype	June 2004-July 2004

Open issues

- Migration to Actel