ALICE - TPC FEE

Requirements and procedures for the acceptance tests of the ALICE TPC FEE

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March 2001

Chapter

1

Requirements and Procedures

1.1 Introduction

This chapter describes the requirements for the production testing of the different components of the ALICE TPC front-end electronics (FEE). It is meant to provide pass/fail criteria based on the analysis of data taken during the screening of the components. The purpose of the test is the qualification of good components to be delivered for mounting on the TPC detector (database filled with all electrical parameters and identifiers of the components).

The architecture of the ALICE TPC FEE and a full description of its components are described in the "ALICE TPC Technical Design Report". The system building blocks and the system architecture are depicted in fig. 1 and fig. 2 respectively.

The front-end electronics for the ALICE TPC consists of 570000 channels. A single readout channel is comprised of three basic components: an amplifier/shaper, an ADC and a digital circuit. The amplifier/shaper (PASA) is contained in an ASIC, which integrates 16 channels, while the digital circuit (ALTRO) is contained in an ASIC that incorporates 8 channels. Although the baseline design is based on a commercial off-the-shelf component, it might be possible that in the final design the ALTRO chip incorporates also the ADC and 16 channels instead of 8. The complete readout chain is part of the front-end card (FEC) that contains 128 channels. The basic components are packaged and mounted on the FEC with surface mounting technology. A readout control unit (RCU) controls a group of FECs (up to 32). The rest of the components mounted on the FEC and the RCU are commercial components. In summary, there are two types of components and two types of boards to be tested:

- PASA 40000
- ALTRO 80000
- FEC 5000
- RCU 200

1.2 Amplifier / Shaper circuit

The first step in the test consists in measuring the power consumption of the chip. All chips that show correct power consumption are tested without stopping due to the failure of any one test. This approach is driven by the necessity of having full information on all the chips produced.

The functionality of the analogue chip is tested using an external calibration circuit that injects a given charge into the 16 inputs, one at a time. The amount of charge varies over 5 different values. Each time all 16-output signals are measured. The full set of tests is performed for several (up to 3) values of the supply voltages. From these measurements the following parameters will be derived:

1. Output DC Offset
2. Conversion Gain
3. Equivalent Noise Charge
4. Linearity
5. Shaping Time
6. Channel to channel cross talk

An "on board" voltage regulator, equipped with the ON/OFF feature, supplies the chips under test. Therefore to insert and remove a new set of chips, the test board does not need to be completely power down; only the board sector where the chips are being plugged undergoes the power cycle. A test-board controller, based on FPGA, controls the voltage regulator. The latter has to be tailored such that the maximum current it can deliver does not destroy (fuse the bonding wires) the chips under test. In this way, the nominal value of the supply voltage can be immediately applied to the chips. The circuit depicted in fig. 1.3 can measure the current absorbed by the chip. The measurement of the current is done in static conditions for the three values of the supply voltages, which correspond respectively to minimal, typical and maximal rating conditions.

The charge signal is created by sending a rectangular pulse into a capacitor (~1pF) in series with the input of the amplifier (fig. 3). The value of the charge should take the values $(4.8 + 35 \times I)$ fC with $I = 0,1,2,3,4$, which correspond to signals from 1 to 30 MIP. A 10-bit 20-MSPS ADC converts the output signals. The outputs of the amplifier are multiplexed, converted by a 10-bit 20-MSPS ADC, and eventually processed by an FPGA.

The first step consists in measuring the output signals while the inputs are closed to ground. From this data sample, the DC offset of all the channels can be obtained. The number of samples to be acquired for this measurement is 100 per channel, which corresponds to an acquisition time of about 5us per channel.

The second step consists in injecting a charge signal in the amplifier inputs, one at a time. This is done by means of an analogue switch (1 to 16). The input signal consists of a train of 100 rectangular pulses with a width of 4us and a period of 8us (see fig. 1.4). The pulse train has a total duration of 800us, leading to a total time of 12.8ms to loop over the 16 channels. This measurement is repeated for the first 4 values (lowest) of the input charge signal. For the highest value of the input signal, the pulse train is applied 16 times on each of the 16 inputs. For each pulse train, a different output is red out. In this way the channel-to-channel cross talk can be measured. The total time required for the overall measurement is about 256ms.

Each input rectangular pulse creates an output semi-gaussian pulse whose amplitude is proportional to the charge borne by the input signal. In order to extract the amplitude and the full-width-half-maximum information, the digitised pulses have to be reconstructed with a polynomial fit. From each reconstructed pulse we extract two numbers:

1. A: amplitude;

2. W: width (FWHM)

We use 4 indexes to refer to these two quantities measured for the different input pulses and channels. The first two indexes - n and m (n, m = 0, 1, 2, …, 15) - refer to a measurement of the output pulse in channel n when the input pulse is injected in channel m. The third index j (j = 0, 1, 2, 3, 4) refers to the amplitude of the input signal. The fourth index k loops over the number of rectangular pulses within a train of given amplitude. The following 32000 number will be derived for each chip:

A_{nnjk}, W_{nnjk}: n = 0, 1, 2, …, 15; j = 0, 1, 2, …, 99; k = 0, 1, 2, 3

A_{mnjk}, W_{mnjk} m, n = 0, 1, 2, …, 15; j = 0, 1, 2, …, 99 ; k = 4.

- The mean value of the amplitudes divided by the corresponding input charge gives the conversion gain:

$$\text{Conversion gain} = \langle A_{nnjk}/Q_k \rangle$$

- The standard deviation of the distribution of the amplitudes, divided by the conversion gain, gives the noise:

$$\text{Noise} = \sqrt{E[((A_{nnjk} - \langle A \rangle_{nj}) / \text{conversion gain})^2]} \quad j = 0, 1, \ldots, 99; \quad k = 0, 1, \ldots, 4$$

- The mean value of the FWHM is computed using all the measurements:

$$FWHM_n = E[W_{nnjk}] \quad j = 0, 1, 2, \ldots, 99; \quad k = 0, 1, \ldots, 4$$

- To compute the linearity, the amplitudes of the output signals corresponding to the 5 different input signal are linearly fitted. The mean squared error between the best linear fit and the sample of measured amplitudes will be taken as measurement of the linearity.

1.3 ALTRO chip

1.3.1 Power consumption

The measurement of the power consumption will be done under static and dynamic conditions. A static condition means here a free running clock but static values on all the other inputs. The dynamic conditions correspond to a variable data pattern on the input data ports while the processing circuits are activated by the trigger signal.

1.3.2 Functional test

The post-fabrication tests are performed to detect the small percentage of devices that are faulty, as a result of various defect mechanisms present in the fabrication and packaging process. This involves identifying the correctly functioning devices, but not characterising their dynamic performance.

The acceptance test applies a set of static test vectors and measurements. These verify the input-to-output transfer of the ASIC, and check its static specifications such as input and output cell parameters. The static vector tests and measurements that will be applied to the ALTRO chip are summarised hereafter.

1. Short circuit tests on all pins.

2. Power supply current (IDD) test with 3.3V supply, at start of test vector sequence.
3. Input pin leakage current test with maximum supply voltage (VDD).
4. Functional Test (full FT sequence) at nominal VDD and nominal input levels.
5. Full functional test at minimum VDD and nominal input levels.
6. Full functional test at maximum VDD and nominal input levels.
7. Full functional test at minimum VDD and input voltage levels set at data-sheet limits.
8. Full functional test at maximum VDD and input voltage levels set at data-sheet limits.
9. Stand-by IDD test with maximum VDD at end of vector sequence
10. Output low voltage test at minimum VDD.
11. Output high voltage test at minimum VDD.
12. Leakage current test on high impedance outputs at maximum VDD
13. Optional parametric testing

Each time the functional test vector sequence is applied it is repeated a number of times (up to 10 times for each input plus initial run). Each input (including the clock) is individually advanced and retarded in steps of 10ns up to a maximum skew of 50ns, to test for circuit sensitivity to input skews. With a properly functioning circuit and static test vector sequence, the output vectors remain unchanged from the non-skewed cause during these tests.

Dynamic tests such as propagation delay or set-up and hold time measurement are not performed. The test vectors are applied at a standard rate (1MHz) to ensure that the circuit is stable when the output data is sampled. There are too many combinations of possible dynamic measurements that might be required for them all to be applied to every device. However, only a few of these results would supply useful information about the device. For parametric measurements to be a realistic proposition, it is necessary to identify the measurements that are significant.

The production acceptance tests verify that the performance of a device is in accordance with its functional specification as defined by simulation results. The FT sequence consists of 128K test vectors. This set of test vectors is defined in order to exercise the highest possible number of internal nodes and achieve the highest fault coverage. The production faults that are not covered by the test vectors are not functionally relevant.

In case of a test failure, additional tests have to be performed to evaluate the severity (importance) of the detected faults. For example, single bit errors in the least significant bits of the pedestal and data memories can be tolerated. A classification of the errors will be produced as result of the chip fault simulation.

1.4 Front End Card (FEC)

1.4.1 Power consumption

The FEC is powered by means of two supply voltages (+V1, +V2) and a common ground. The corresponding currents I1 and I2 at the input of the board have to be measured. From these two main supply voltages, for each of the 4 sections of the FEC, four supply voltages are derived and distributed (+2.5V for the ADCs, +2.5V for the digital circuits and +3.3V for the PASA). All these voltages can be measured by means of the local slow

control circuit. Optionally, the measurement of the voltage regulators output voltages can be cross-checked by a direct measurement done by means of test needles.

1.4.2 Power consumption

- Test (write/read access) of all the memory elements of the Board Controller and ALTROs:
  - Configuration / Status registers of the Board Controller;
  - Configuration / Status registers of the 16 ALTROs;
  - Pedestal and Data Memories of the 16 ALTROs.
- Then the ALTROs are set in test mode. The pedestal memories are filled with predefined patterns and a trigger signal starts the data processing. The data pattern will exercise all ALTROs, the internal data bus, the GTL transceivers, and the connectors.
- Test of the input connectors, amplifiers, ADCs, and digital connection between ADCs and ALTROs. An external circuit injects, into one of the 128 inputs at a time, a given signal, whose amplitude can vary over 5 different values. Each time, all 128 channels are read out.

The full set of tests is performed for several (up to 3) values of the supply voltages.

1.5 Burn-in test

After mounting on the TPC the exchange of defective FECs is rather time consuming. For this reason it is planned to eliminate weak cards even before mounting them on the detector by exposing them to an extensive burn in test.

For this purpose a set of front-end cards, corresponding roughly to the number in one “readout crate” (i.e. about 20 cards), are placed in a thermally isolated box. This set of cards is read out either by an RCU (dependent on availability at the time) or by a special PCI interface card being developed presently as a prototype for the RCU.

Since the cards are isolated from the environment, they will heat up relatively fast (total heat dissipation for 20 cards is about 200 Watts) to a temperature between 50 and 60 degrees ^{0}C. At this point the power can be switched off (or a fan can be started) to cool the system down to room temperature. During the thermal cycle the functioning of the cards will be continuously monitored. Several warm-up/cool-down cycles in the isolated box are foreseen requiring about 10 hours of operation in total.

This test requires injection of charge into all channels under test. Thus some effort has to go into the design of a system of boards providing the proper signals to pulse all channels.

1.6 Recording of information

The For statistical analysis and proper bookkeeping it is foreseen to attach a barcode to all chips and FECs. In addition the FECs will have their identification number stored in a PROM accessible by the slow control system (via the RCU). Correspondingly all the test stations need to be equipped with bar code readers in order to allow automatic identification of cards and components. A proper database has to be chosen according to the standards used in Alice (i.e. Oracle, Objectivity, ROOT...).

Chapter

2

Test set-up

2.1 Introduction

A block diagram of the system to test the TPC FEE components is shown in fig. 2.1. It is based on three basic functional units. The first unit, specific for each component under test (ASTF - **A**pplication **S**pecific **T**est **F**ixture), is dedicated to provide the supply voltages, to generate and apply the stimuli signals, and to probe the response of the circuit to the stimuli. The second unit – RIC (Readout Interface Card) - is an interface between the ASTF and a commercial PCI card, and is based on the FEC interface to the RCU. The third unit is a readout control unit, and is based on a commercial PCI card equipped with a custom mezzanine card. It emulates, as far as the readout protocol is concerned, the RCU and will be referred as PCI-RCU.

2.2 Test set-up for the PASA

fig. 2.2 (ASTF for the PASA);

2.3 Test set-up for the ALTRO

The ASTF for the ALTRO is depicted in fig. 2.3. During the functional test the output signals are sampled by the FIFO-memories. By adjusting the delay device, the sampling time can be adjusted compared to the output signals. The resistors have a dual function. The first is to give the output signals a certain load during all tests. The second use is to measure the output leakage current. This is done with the outputs in a high impedance state. The ADC measures the voltage drop over the resistors. The analogue switch selects one output at a time. The ADC is also used to measure the high and low output voltage levels during static conditions.

Figure 2.4 shows the test of the input signals. A test pattern is stored in the FIFO-memory. This pattern is transferred to the chip through the drivers. By varying the supply voltage to the drivers the output levels from the drivers can be adjusted. In this way it is possible to see that the inputs are tolerant to signals that are on the limit of the tolerances. The input leakage current can be measured by putting the drivers in a high-impedance state and measure the voltage drop over the resistors. It should be noted that the leakage currents from the drivers are included in the result.

2.5 Test set-up for the FEC

A block scheme of the test set-up for the FEC is shown in figure 2.5. The different parts of the test set-up are described below. A card that is going to be tested is put into a fixture. The fixture makes it possible to connect to the card by a combination of ordinary

connectors and test needles. The needles makes it possible to assess internal points that are not routed to any connector. The power and slow control signals can probably also be applied through test needles. Even the bus-interface signals can go through the same type of needles. The charge signals will most probably require that cables be connected to the input connectors. Most of the signals are connected through the test control board. This board is in turn connected to a PC that controls the whole test.

Power consumption and voltages

The supply voltages to the board are adjustable so the board can be tested under both normal conditions and with the voltages at the limits. The supply currents can be measured during the whole test. There is a current limit on the supply to avoid destroying the board in case of a shortcut or some other fatal error on the board. All outputs from the voltage regulators on the board itself can be measured through test needles.

Slow control

The slow control interface is connected trough the test control board to the PC. The test control-board simulates the normal (or a bit worse) load on the signals.

Bus interface

In the same way as for the slow control signals, all the bus signals are connected trough the control board to the PC. The signals are loaded to simulate the normal working conditions when many FEC boards are connected to the same bus.

Charge input

The charge signals are produced in the same way as described in the test of the PASA. The only difference is that in this case we need to be able to inject charge into 128 channels.

The test procedure

The test starts by applying the supply voltages at nominal values. The supply currents and the output voltages from the internal regulators are then measured. If any of this are out of their limits, the test is interrupted and the power is switch off. This is done to avoid destroying the board in case of a sever error. In the next step, the slow control interface and the board controller is tested. This test is done by writing and reading from all the registers in the board controller.

After this, the registers in all the ALTROs are tested by writing and reading them. Then the pedestal and data memories are tested. This is done more to see if the slow control interface and the board controler is working rather then testing the ALTROs. Then the ALTROs are tested more properly by writing and reading to the registers and memories, but this time through the bus interface. Finally in this part of the test, the pedestal memories are filled with a predefined pattern. Then a trigger signal starts the data processing. The data pattern will exercise all ALTROs, the internal data bus and the GTL transceivers. When all the digital parts are tested, the ALTROs are configured to receive and process real pulses. The charge pulser then injects pulses of different amplitudes on one channel at a time. For each pulse a trigger is sent to the ALTROs. The resulting events are read out and analysed.

Finally the input voltage is first set to their minimum level, and then to their maximum level. The outputs from the on board regulators are measured during this test.

2.6 Readout Software