**The ALICE TPC Readout Control Unit (RCU)**

The TPC Readout Control Unit (RCU) (see figure 1) [1, 2] is responsible for controlling the readout of the TPC, and initializing and monitoring the Front-End Cards (FECs). In total 216RCUs will connect 4500 FECs, with a maximum of 25 cards connected to each RCU.

The amplifying, shaping, digitizing, processing and buffering of the TPC signals is done on the FECs [3].A custom designed integrated circuit, the Pre-Amplifier Shaper (PASA), takes care of the conditioning of the input signal coming from the detector pad plane. A second custom ASIC, the ALTRO (ALICE TPC Read Out) [4], is dedicated to the digitalisation and the further processing of the digitized data. This chip is initialised and controlled directly by the RCU. The communication between the RCU and the ALTROs on the Front-End Cards (FECs) is made via a VME-like custom protocol, where the electrical and physical layers are implemented respectively in the GTL-standard technology and on an especially designed PCB backplane.

The RCU collects the data from the FECs, re-formats the event data and sends the packed to the Data Acquisition Data Link (DDL) by means of the Source Interface Unit (SIU) mezzanine. In addition, the RCU monitors and initialises the FECs. The supervision includes readout of events for monitoring purposes, statistics (readout of number of datastrobes and number of triggers received), temperature variation monitoring, current measurement and power consumption monitoring for hardware fault detection which will be achieved via a separate slow-control bus. The initialisation of the ALTROs is done via the main readout bus, while the power state of each FEC is controlled by dedicated point-to-point lines. All the Slow Control relate signals, the ALTRO Readout data bus, the Control lines and Card Power enable signals are physically implemented on the same backplane.

A readout sequence of the TPC is initiated by a common ALICE trigger-signal. The trigger is distributed to the RCU by the central trigger processor. The Slow Control bus from the RCU is connected to the central Detector Control System (DCS) of the ALICE experiment by the same mezzanine card interfacing with the Trigger and Timing link: the DCS board.

The use of SRAM-based FPGA required special attention to Single Event Upset. To monitor the functionality of the chip, the configuration memory of the main FPGA (VirtexII-pro from Xilinx) is continuously readout by an on-board flash-based microcontroller and compared with a mask stored in a local flash memory. Whenever an error is detected, the microcontroller is able either to reload the complete firmware of the FPGA or reconfigure just the local logic afflicted by SEU (scrubbing technique). Newer version of the firmware can be uploaded by the use of the DCS link.
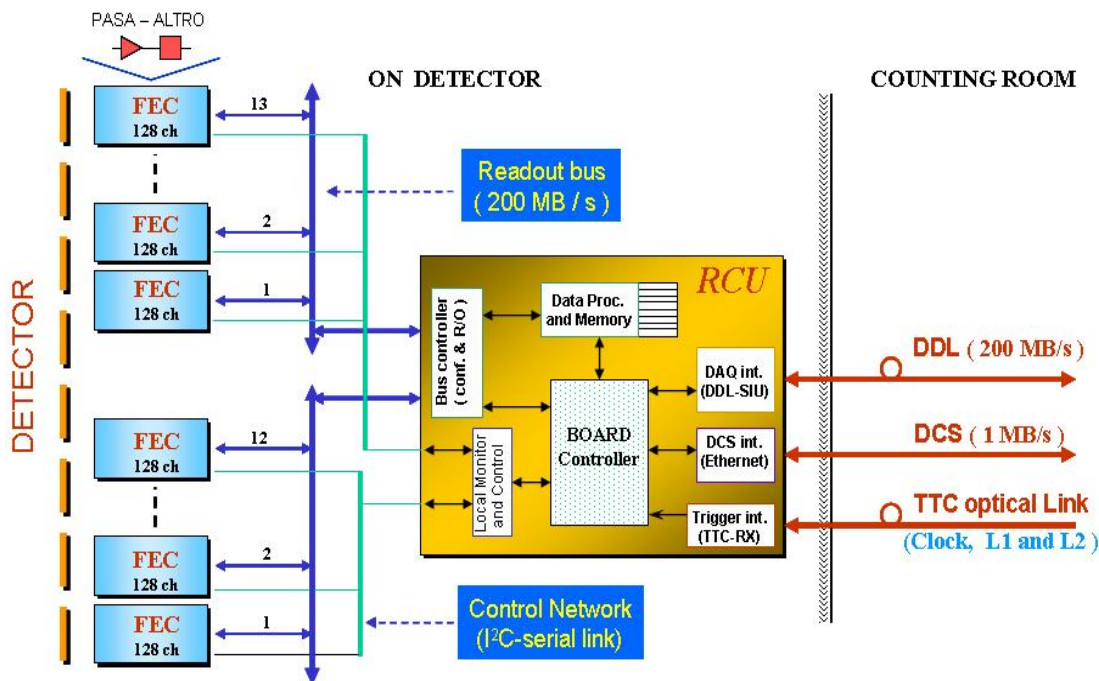
**Figure 1** Front-end electronics system architecture and Readout Control Unit.

The photographs of the top and bottom side of the Readout Control Unit are shown in figs. 2 and 3.

The Top side of the board is equipped with the connectors meant for the Jtag chain of the FPGAs, the connectors for the two mezzanine cards (SIU and DCS board), the main power supply connector for the inputs of unregulated 3.3V (peak current absorption: up-to 3 A) and 4.3 V(current absorption up-to 2A) and a 2mm SMD Ground socket. An optional high-speed signaling connector (J3) can be assembled to inject different level Triggers, as well as extract detector readout informations like Busy, in a FPGA-firmware programmable way. In addition to a 40MHz SMD oscillator (auxiliary board clock generator, when the DCS card is not providing the signal) and a number of passive components, 6 LDO power regulators in TO263-5 package are identifiable with the respective tantalum capacitive networks. Those regulators are for the supply of the GTL terminations voltages (both RCU on board and backplane), FPGA core FPGA I/O banks and other components assembled on the RCU board.

On the RCU bottom side four connectors are dedicated to the readout backplane connections. The GTL transceivers are located close to the connectors themselves, while other active LVDS/LVPECL transceivers take care of the distribution of the timing

signals. The resistors for the on-board GTL termination network, together with some filtering capacitors and other passive components are distributed on the board bottom side, as well as the VirtexII-pro FPGA, the Macronix Flash memory and the FPGA re-configuration microcontroller (Actel Pro-Asic+) with related power regulator.

The complete package type of the components is reported in the Bill of Material of the manufacturing dossier.
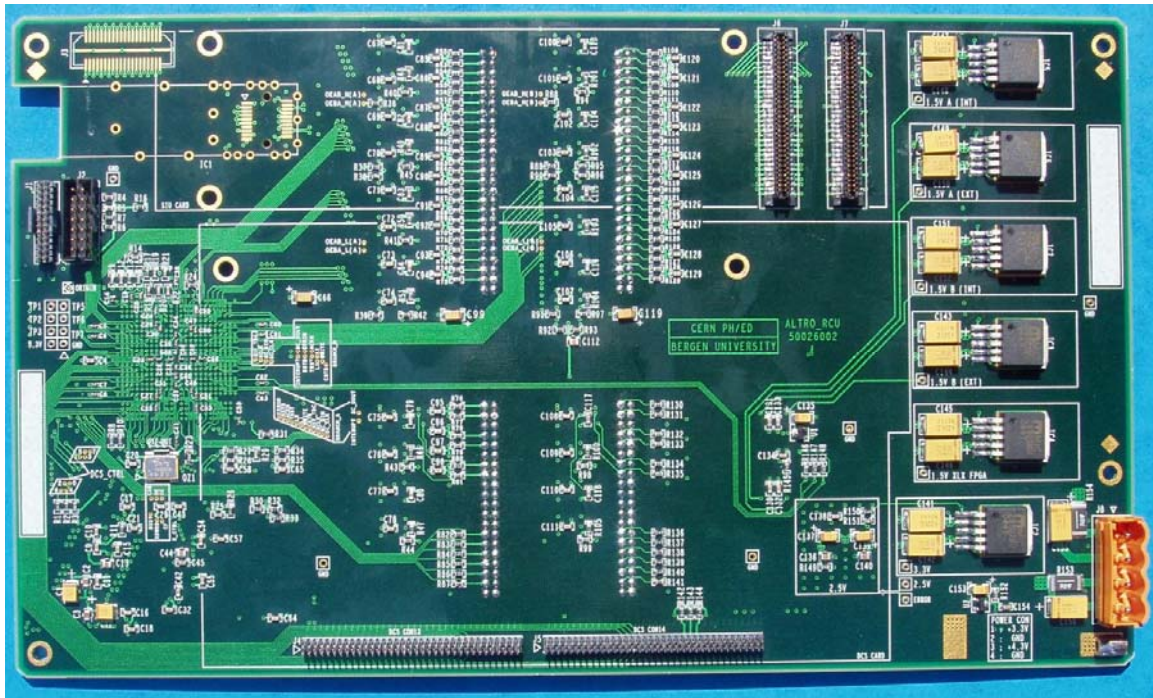
Figure 2. RCU Top view. The Class-6 PCB dimensions are: 230mm Width and 135mm Height.
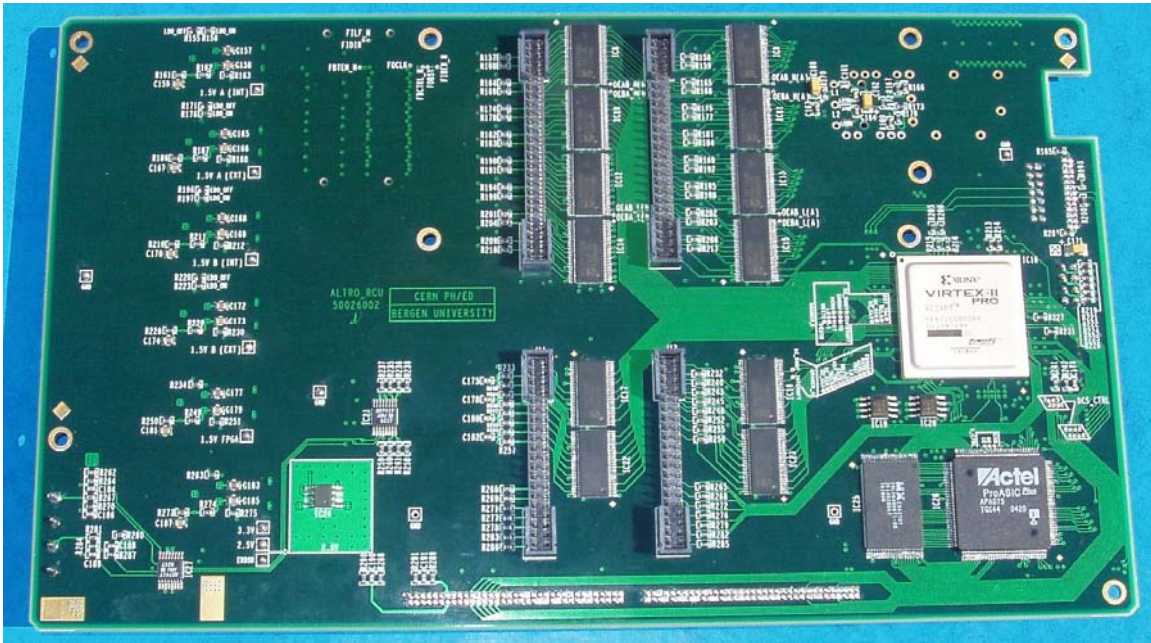
Figure 3. RCU Bottom view

References:

[1] ALICE collaboration, **Technical Design Report of the Time Projection Chamber**, CERN/LHCC 200-001 (2000).
[2] **The ALICE TPC Readout Control Unit**, Proceedings of the 10th Workshop on Electronics for LHC and future Experiments, 13-17 September 2004, Boston, USA[3]
[3]**Performance of the ALICE TPC Electronics** , Proceedings of the 9th workshop on Electronics for LHC Experiments, Amsterdam, 29 Sep - 3 Oct 2003
[4] **The ALTRO Chip: A 16-channel A/D Converter and Digital Processor for Gas Detectors** , IEEE Transaction on Nuclear Science, Vol. 50 N. 6, December 2003