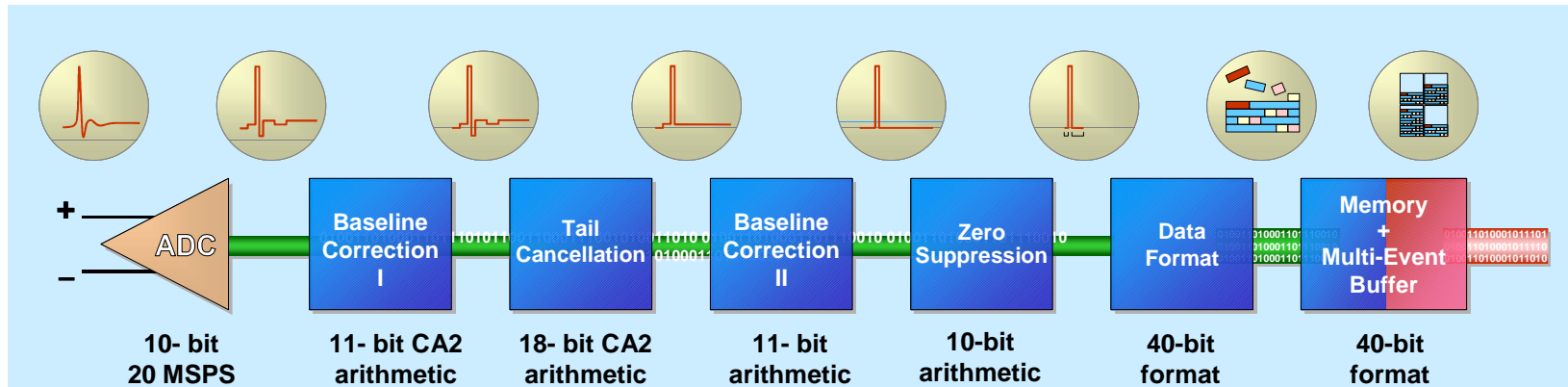


Contents

- **ALTRO Implementation**
- **ALTRO Test Setup and Equipment**
- **ADC Characterisation**
- **Noise and Crosstalk**
- **Power Consumption**
- **ALTRO Testing Strategy**
- **Functional and Physical Validation**
- **Yield Results and Considerations**
- **Conclusions**

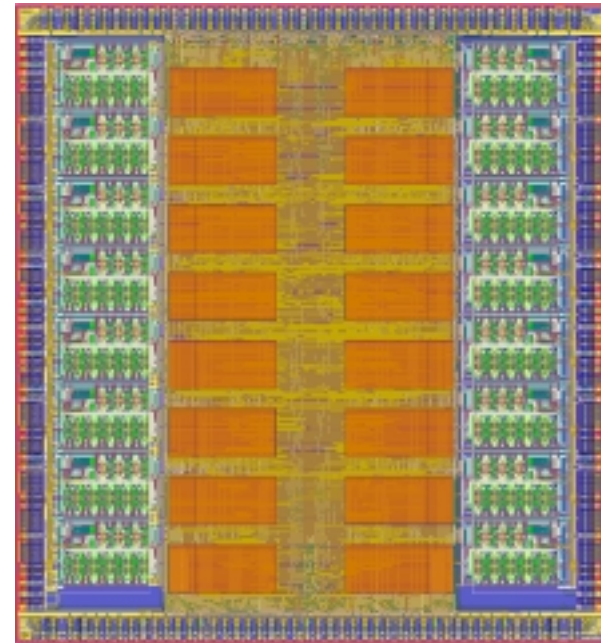
ALICE TPC READOUT CHIP (ALTRO-16)



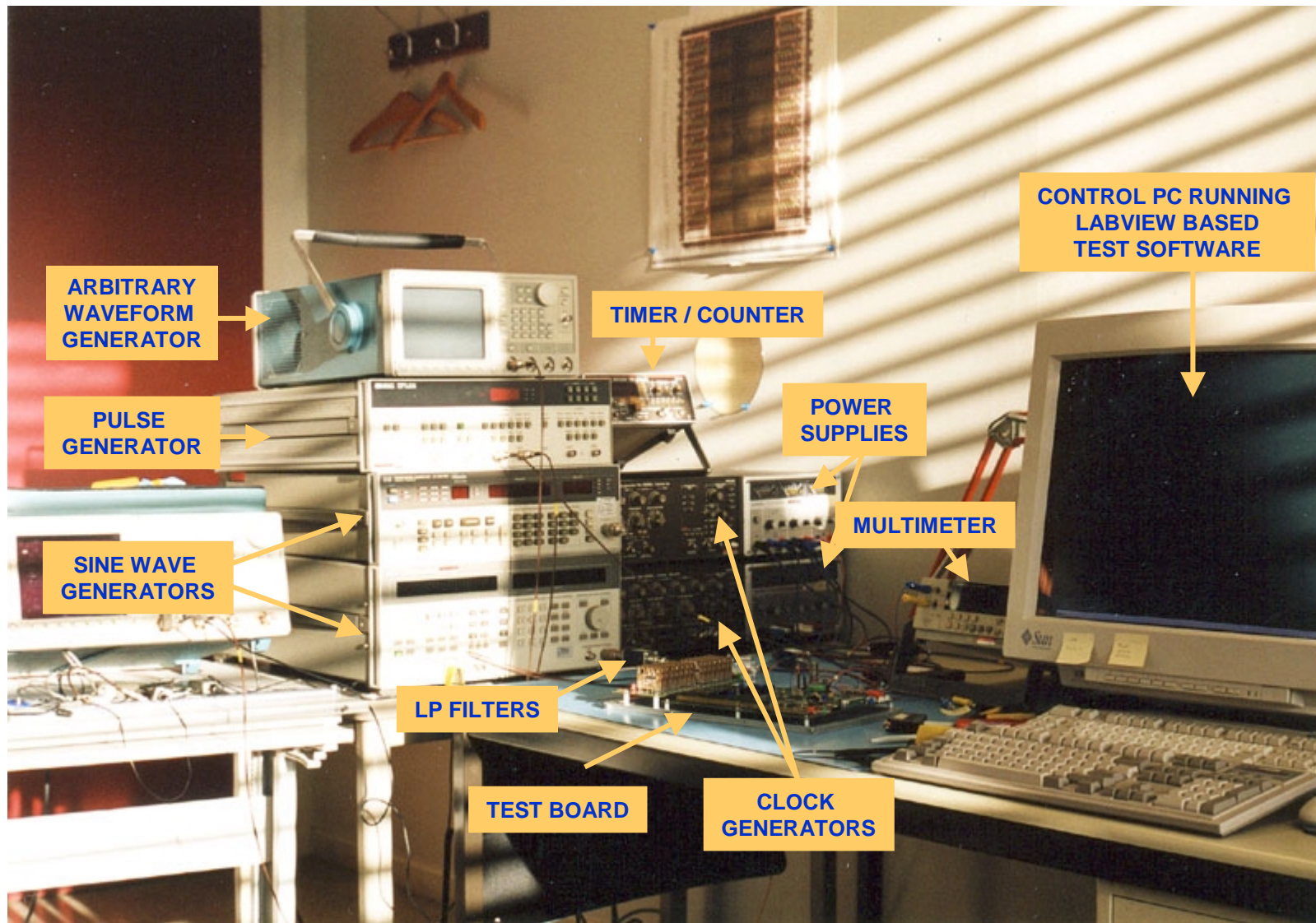
- MAX SAMPLING CLOCK 40 MHz
- MAX READOUT CLOCK 60 MHz

16-ch signal digitizer and processor

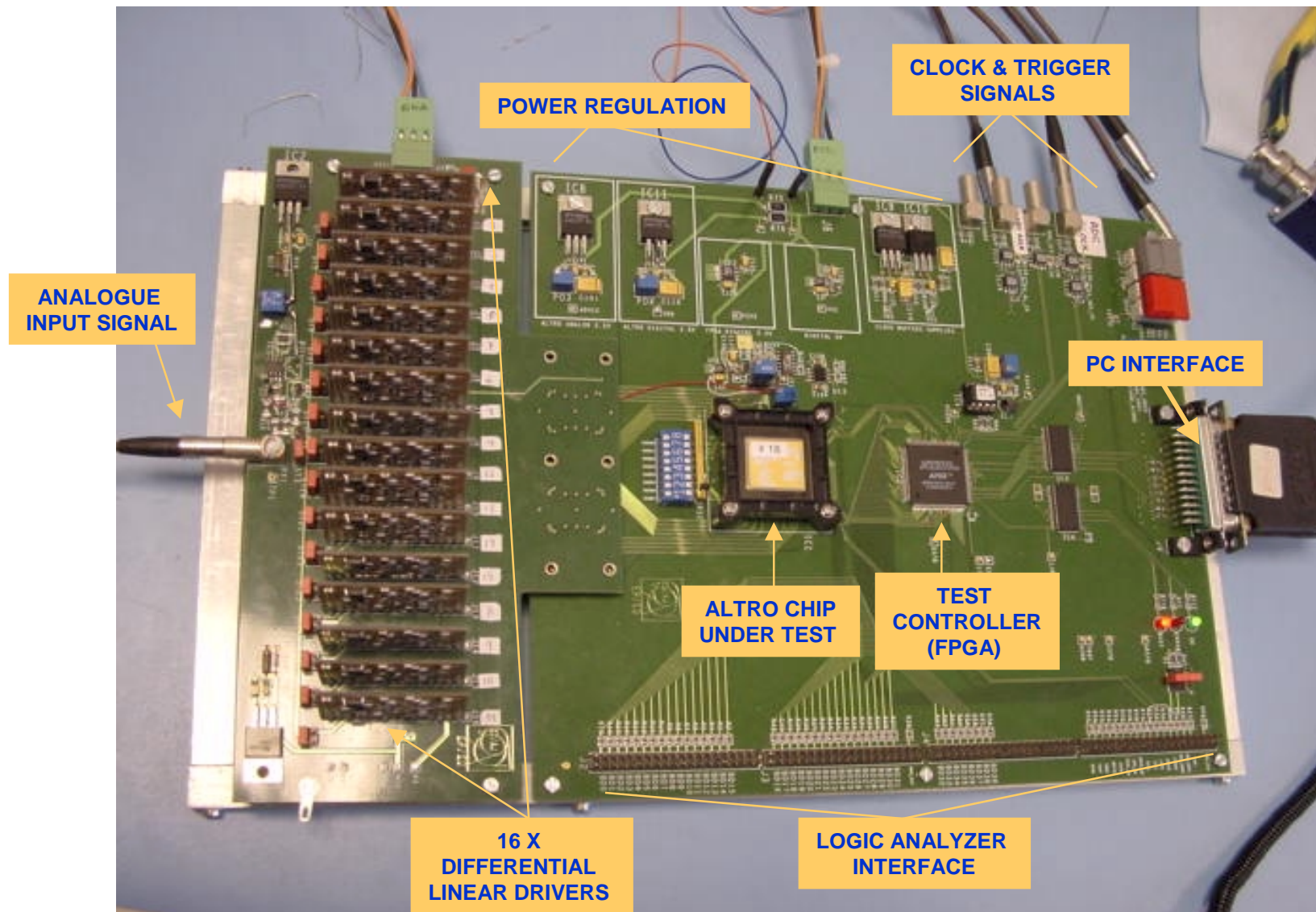
- ◆ HCMOS7 0.25 μm (ST)
- ◆ area: 64 mm²
- ◆ power: < 20 mW / ch
- ◆ prototype delivery: Feb '02
- ◆ 300 samples fully tested



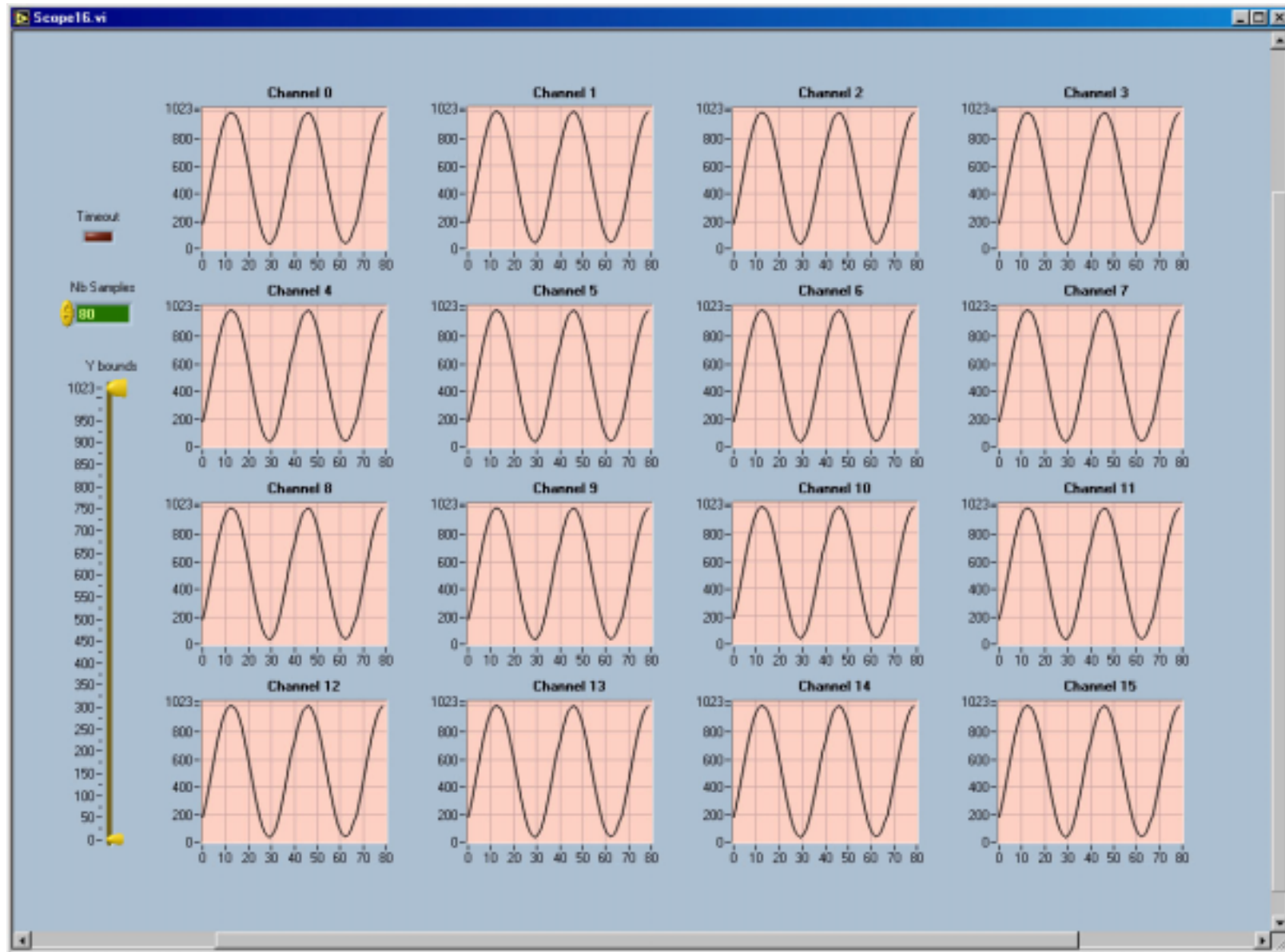
ALTRO Test Setup



ALTRO Test Board

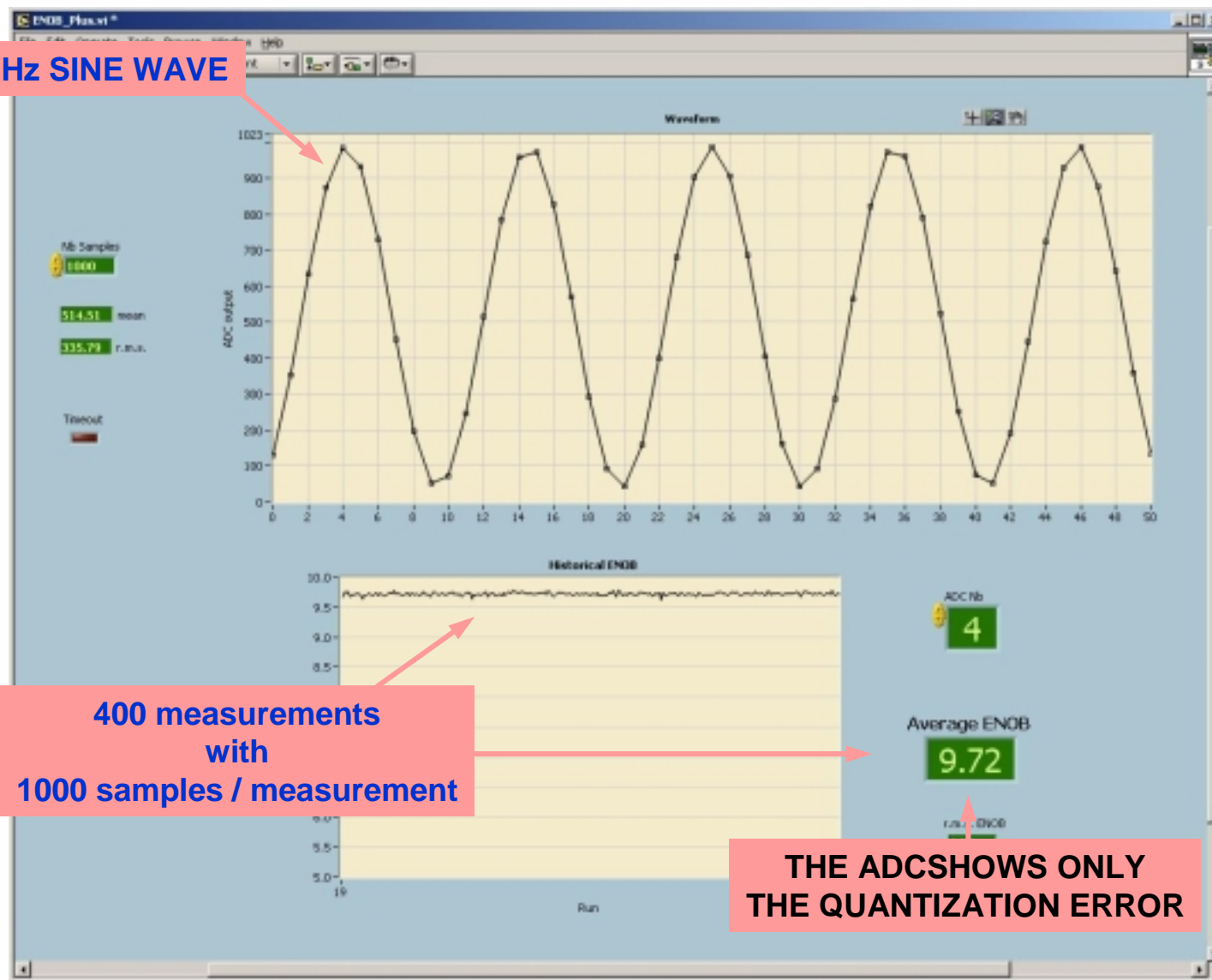


16 channels in one shot



Effective Number of Bits (ENOB)

1MHz SINE WAVE

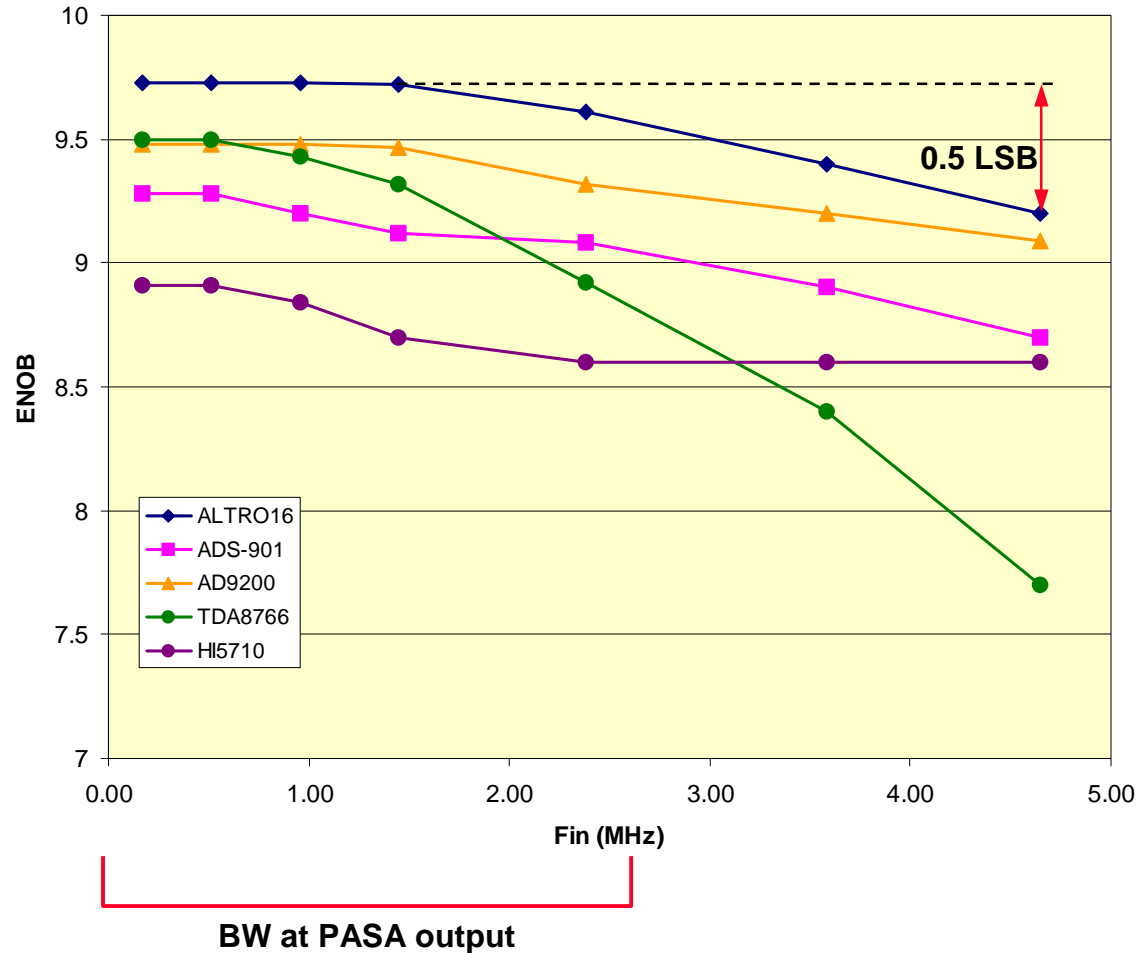


400 measurements
with
1000 samples / measurement

THE ADC SHOWS ONLY
THE QUANTIZATION ERROR

ENOB vs Frequency

Effective Number of Bits vs Input Frequency



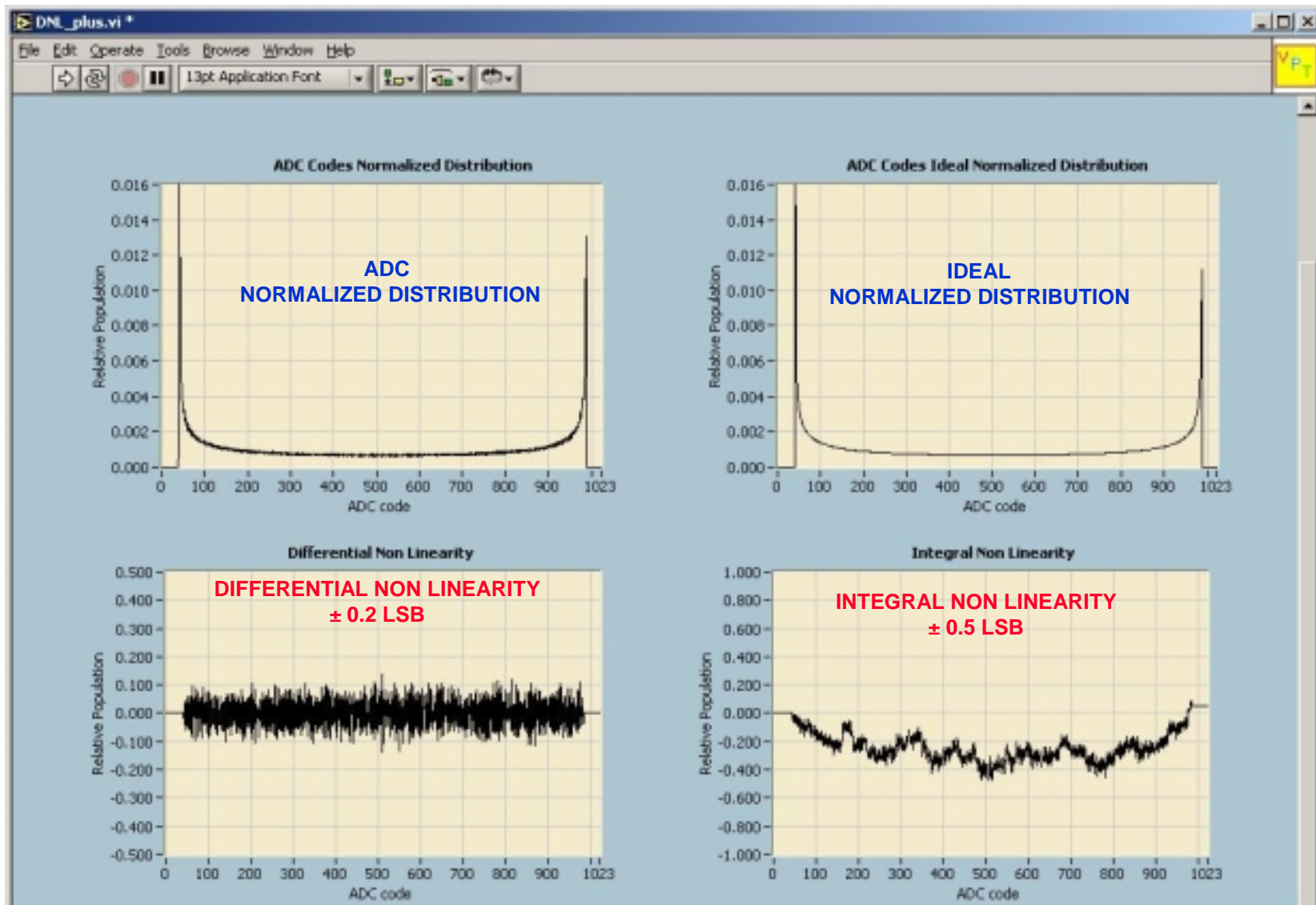
Quartz Jitter:
 25ps r.m.s.
 100ps absolute

Amplitude Uncertainty:

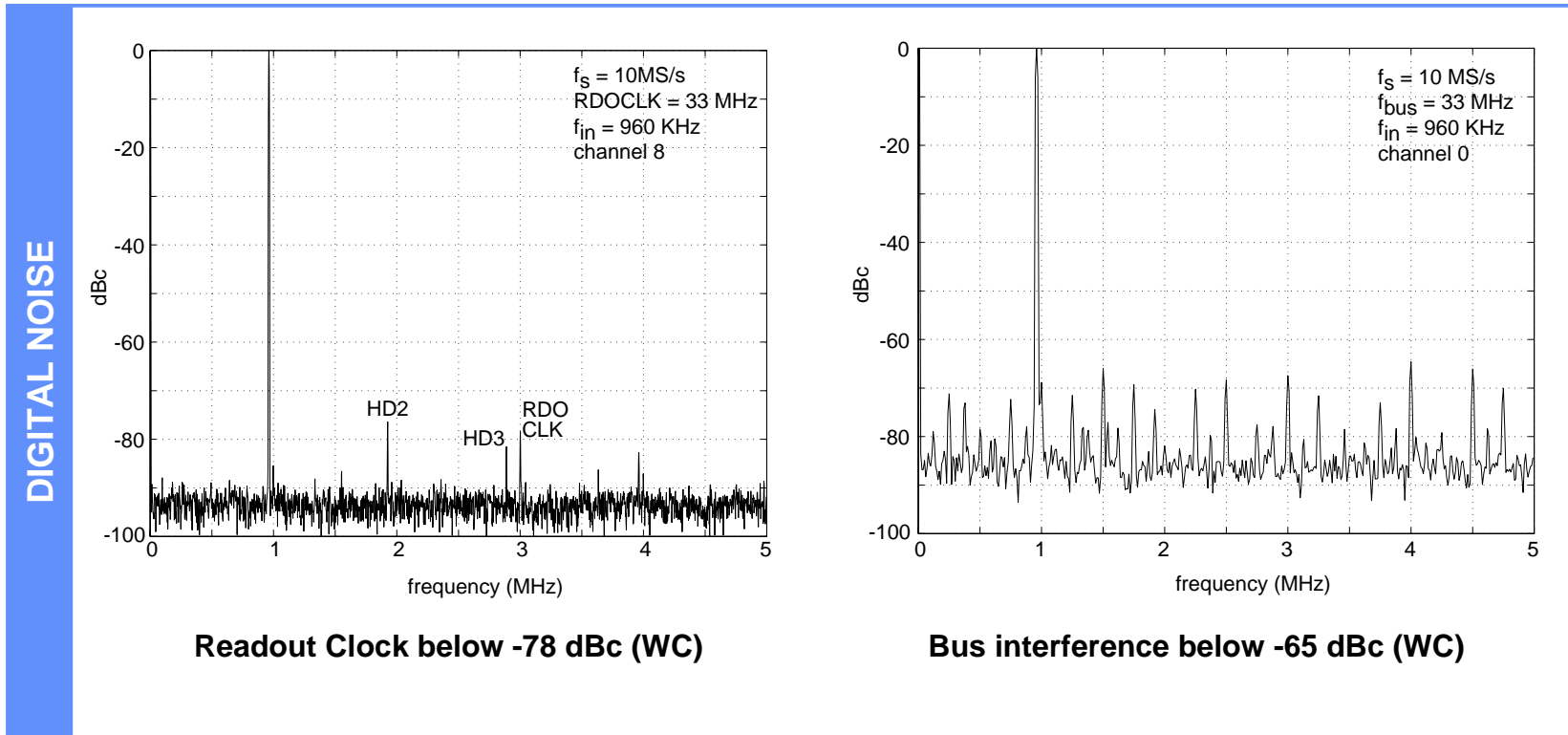
$$\frac{\text{jitter}}{4 \cdot f_{in}} \cdot 2^{10}$$

0.5 bits at 4.8 MHz

Differential and Integral Non-Linearity



Crosstalk and Digital Noise



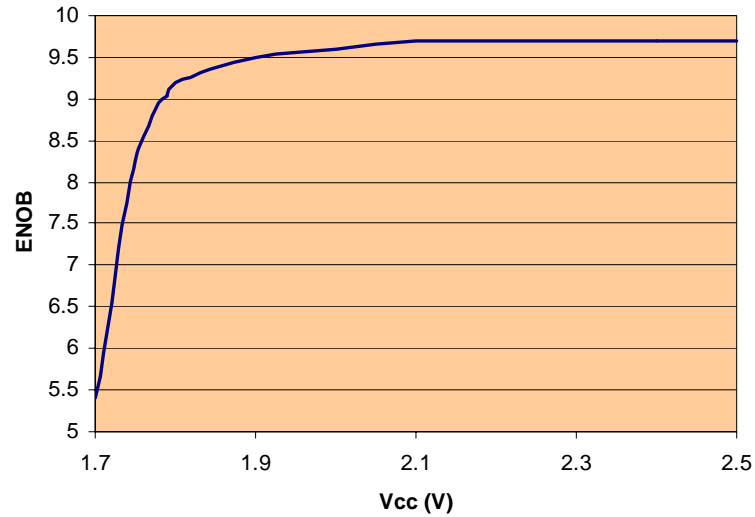
CHANNEL-TO-CHANNEL CROSSTALK

$F_{in} = 1 \text{ MHz}$ 0.05 LSB rms (-80 dBc)
 $F_{in} = 5 \text{ MHz}$ 0.2 LSB rms (-68 dBc)

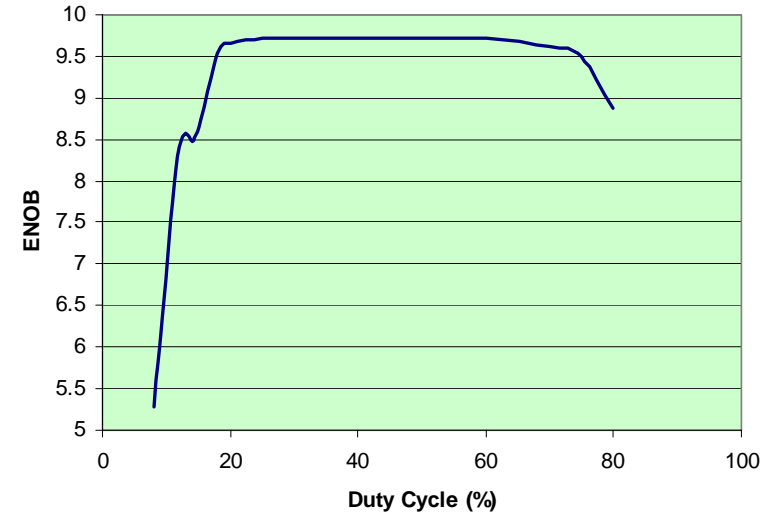
Dynamic Range of a 10-bit ADC: 60 dB

Chip Performance

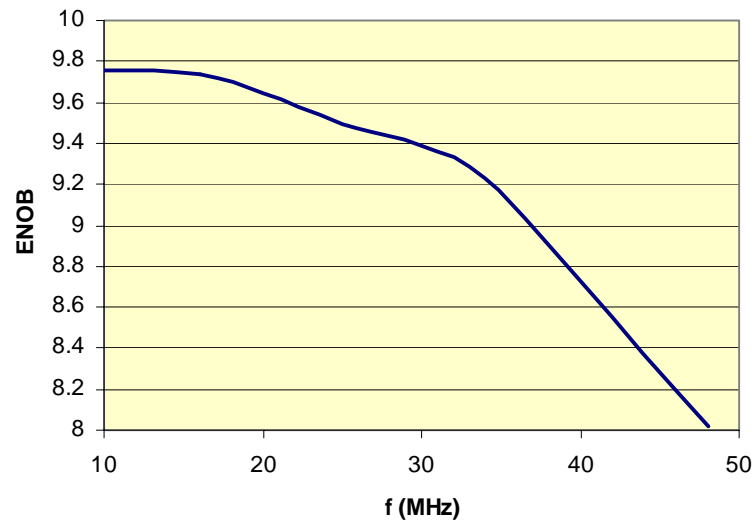
ENOB vs Analog Vcc



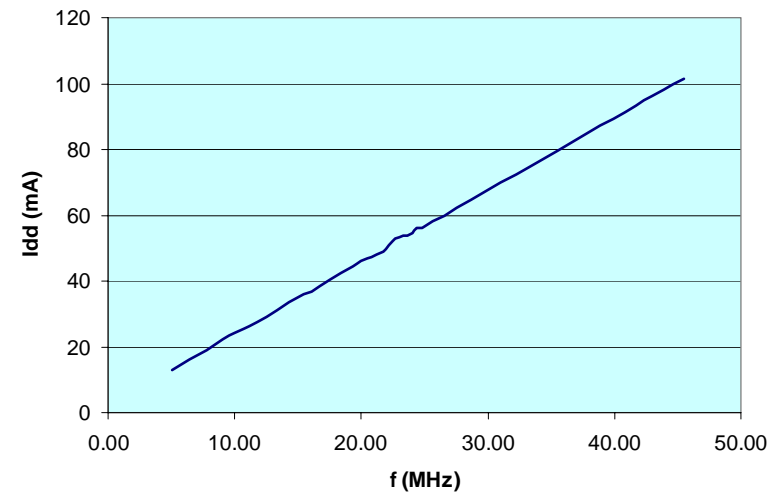
ENOB vs Duty Cycle



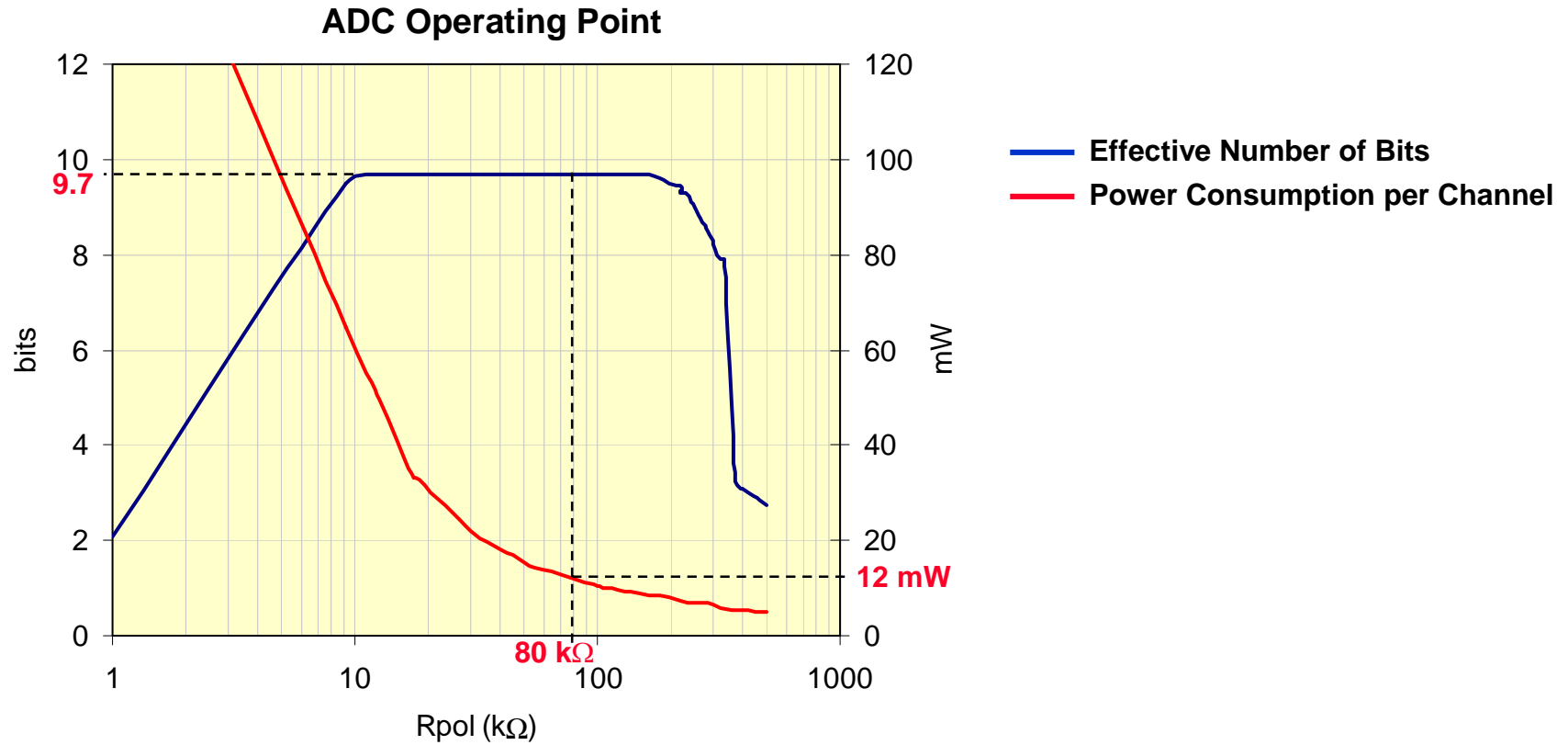
ENOB vs Sampling Frequency



Digital Power Consumption vs Sampling Frequency



Power Consumption



ONE CHIP

Digital leakage current	1.2 mA
ADC Clock Tree (10 MHz)	23 mA
Readout Clock Tree (40 MHz)	1.4 mA
Processing Logic during Trigger (1%)	28 mA
16 ADCs at 10 MS/s	77 mA

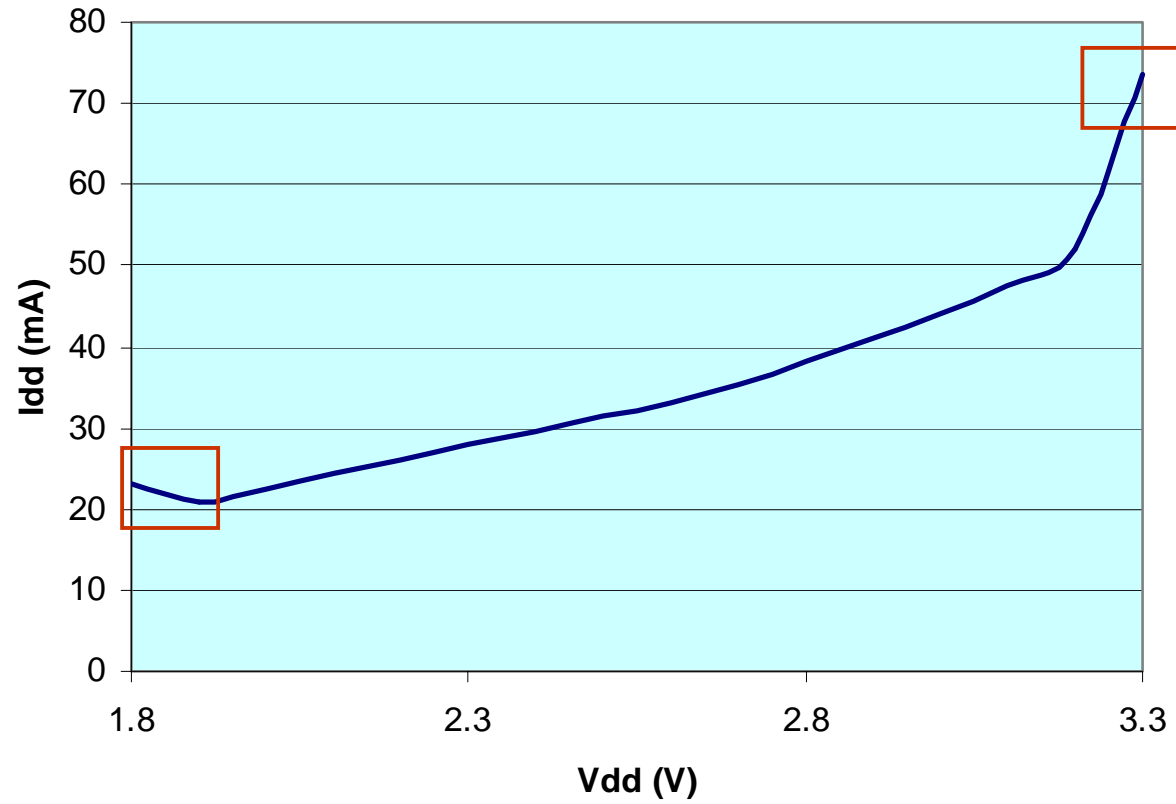
Average Power Per Chip

257 mW

Average Power Per Channel

16 mW

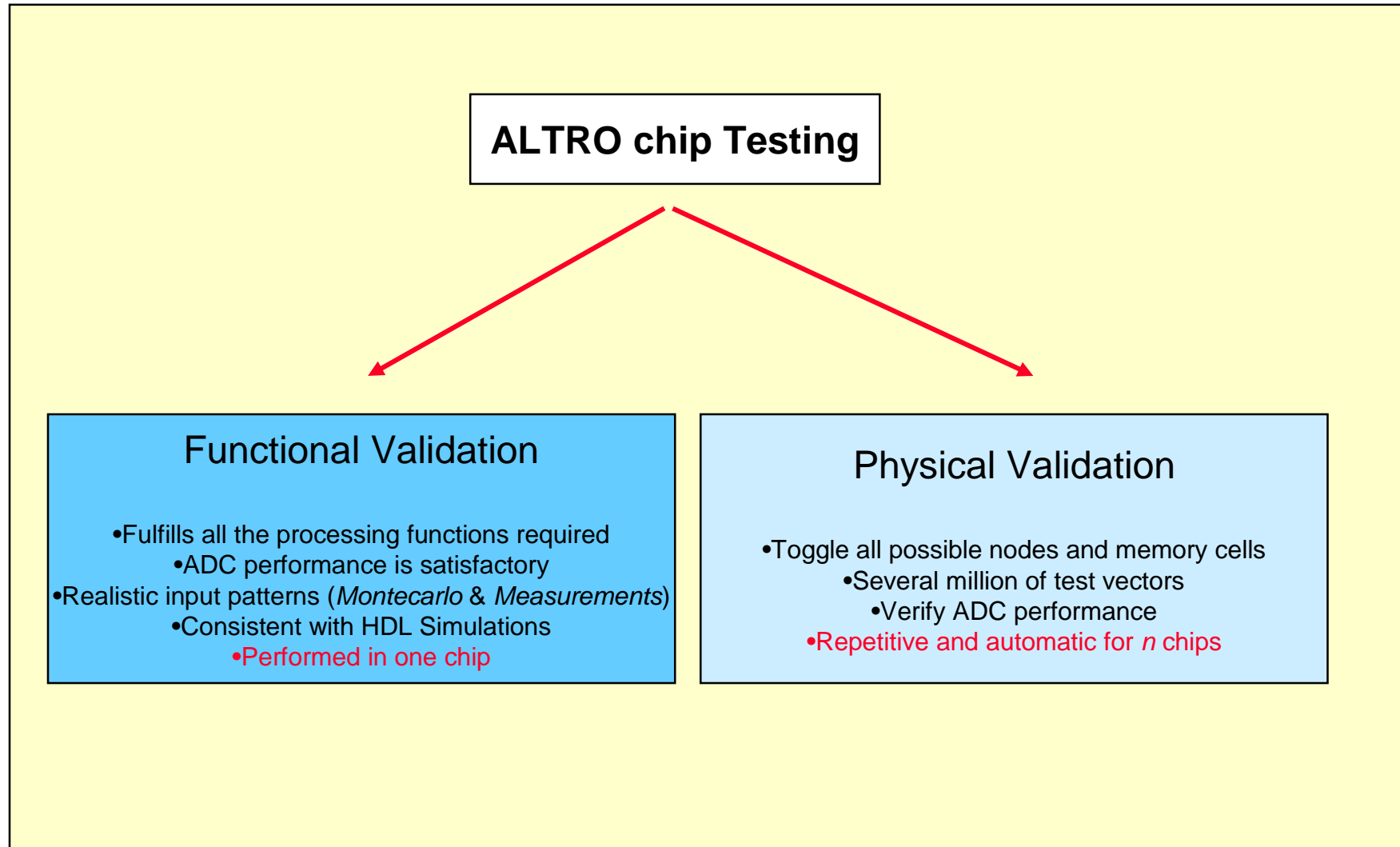
Current vs Digital Supply



ADC CLK : 10 MHz
 f_{in} : 900 KHz
 I_{pol} : 30 μ A (internal resistor)
 V_{cc} : 2.5 V

ALTRO not responding

Testing Strategy



Functional Validation: Register Control Panel

Baseline Correction 1

Mode: $f(t) - f_{pd}$

VPD: 508 FPD: 0

Power Save:

Polarity: Norm Inv

Write PM from File Write All PM from File

Multi-Event Memory

Event Buffers: 4 8

empty full

Write Pointer: 0

Read Pointer: 0

Available Buffers: 4

Last Event Length: 0

Errors

- Readout Error
- Trigger Overlap
- Instruction Error
- Parity Error

SEU

Interface

- Double Upset
- Simple Upset

Memory Unit

- Double Upset
- Simple Upset

Tail Cancellation Filter

Enable

K1: 0.99560	L1: 0.99237
K2: 0.80395	L2: 0.76893
K3: 0.75737	L3: 0.76547

Baseline Correction 2

Enable

LO Threshold: 7 HI Threshold: 7

Presamples: 1 Postsamples: 1

Zero Suppression

Enable

Offset: 0

Glitch Reject: Off

Threshold: 0

Presamples: 0 Postsamples: 0

Trigger

Samples per Event: 0

Trigger Delay: 0

Pretrigger: 0

Trigger Counter: 136

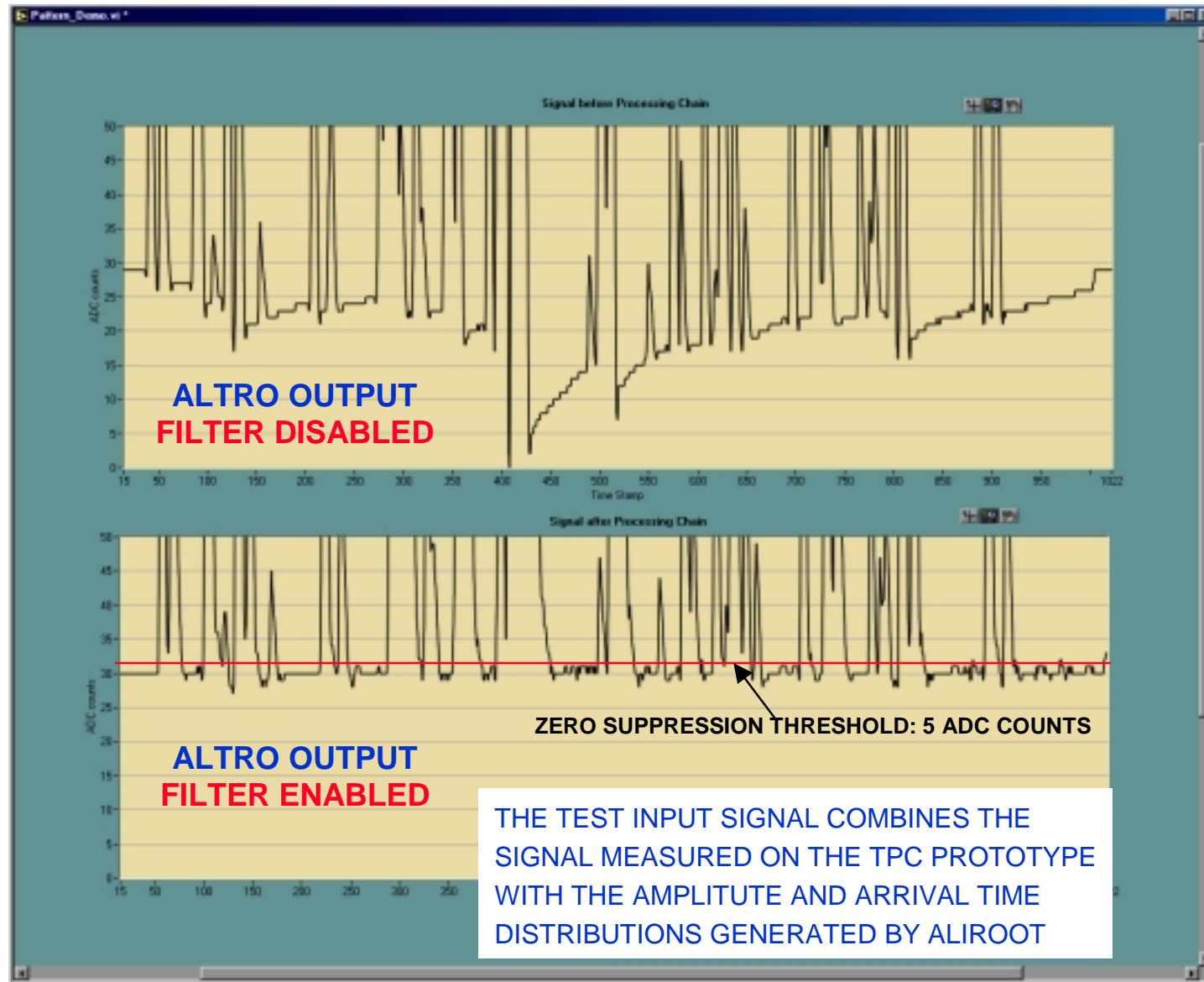
Status Bar

Channel: 0 Chip Address: 0

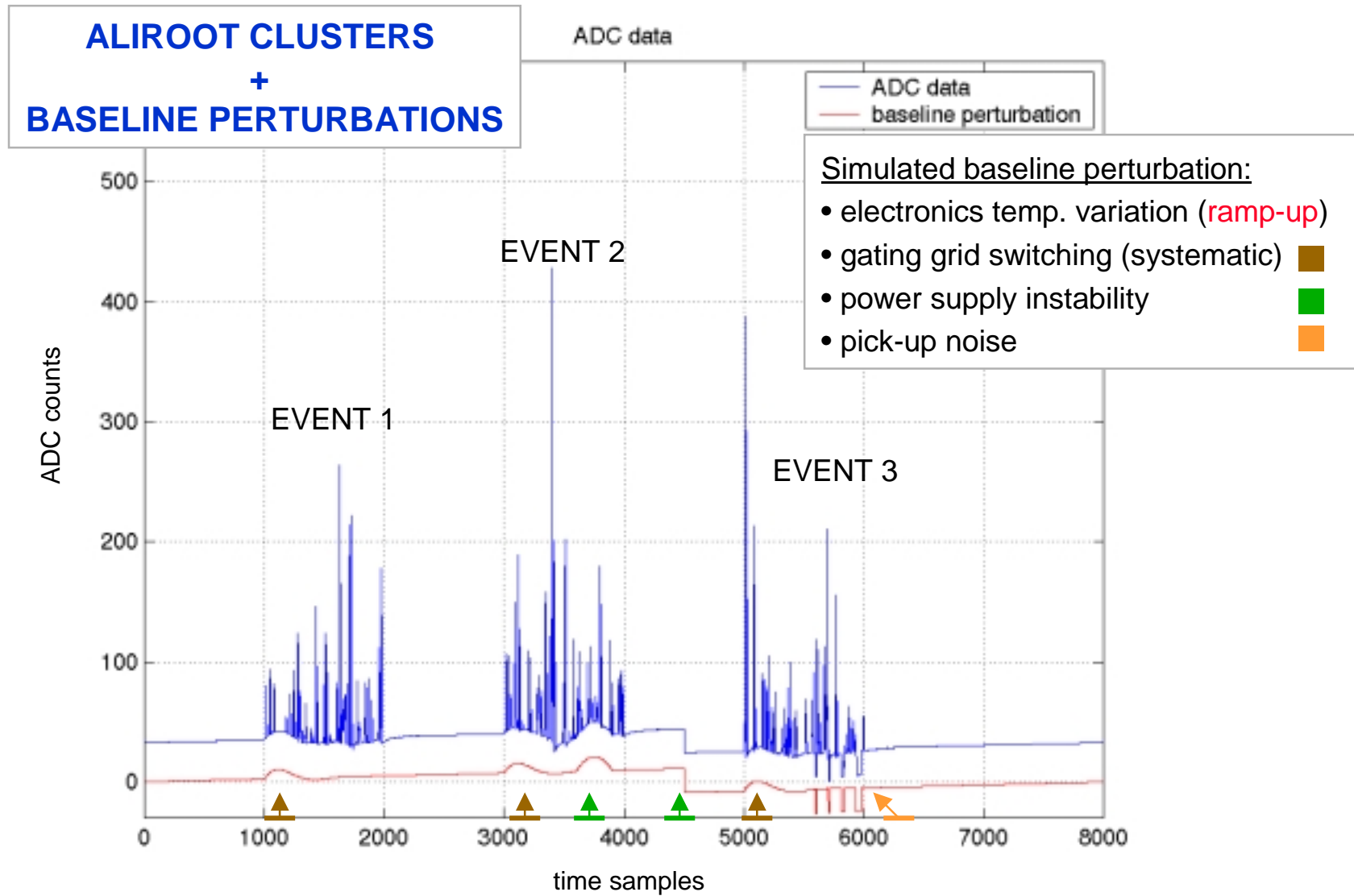
Read All Write All Verify on Write

Unwritten Changes Verification Error Tx/Rx Error

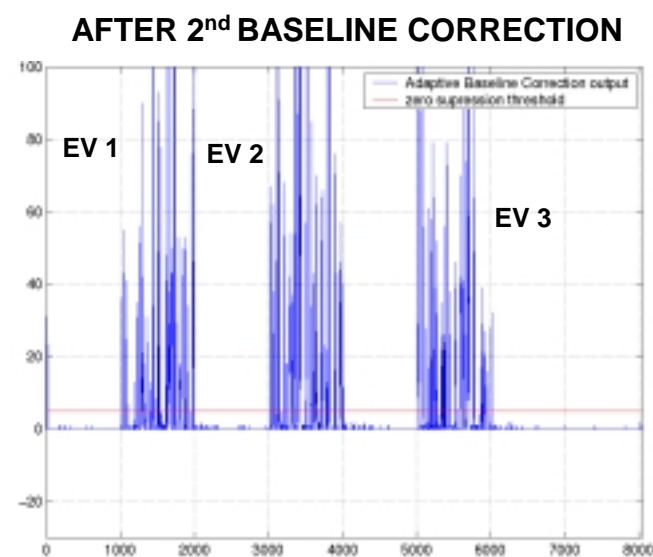
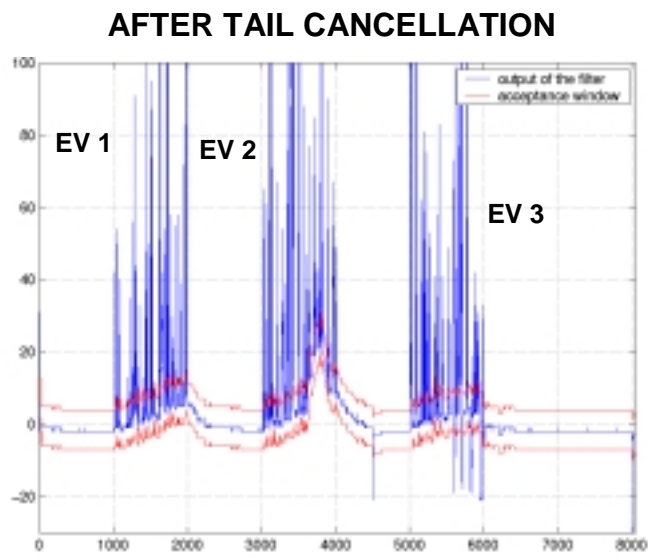
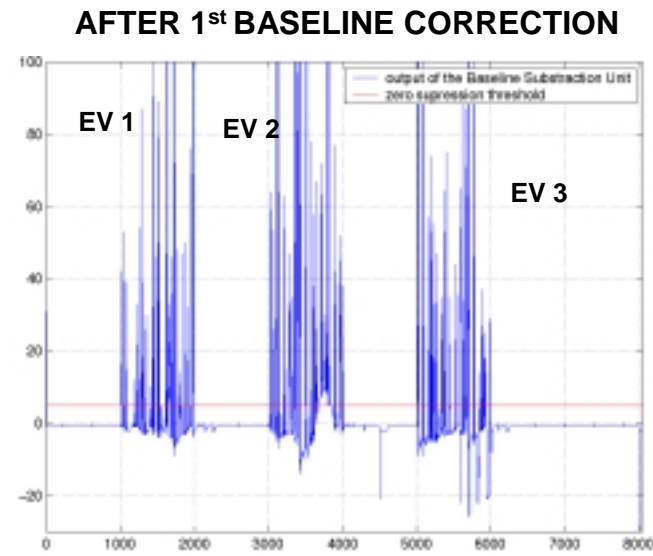
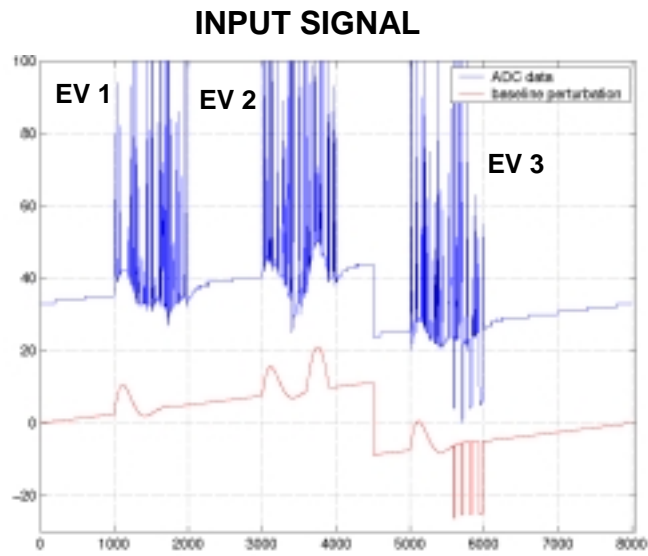
Functional Validation: Realistic Input Pattern



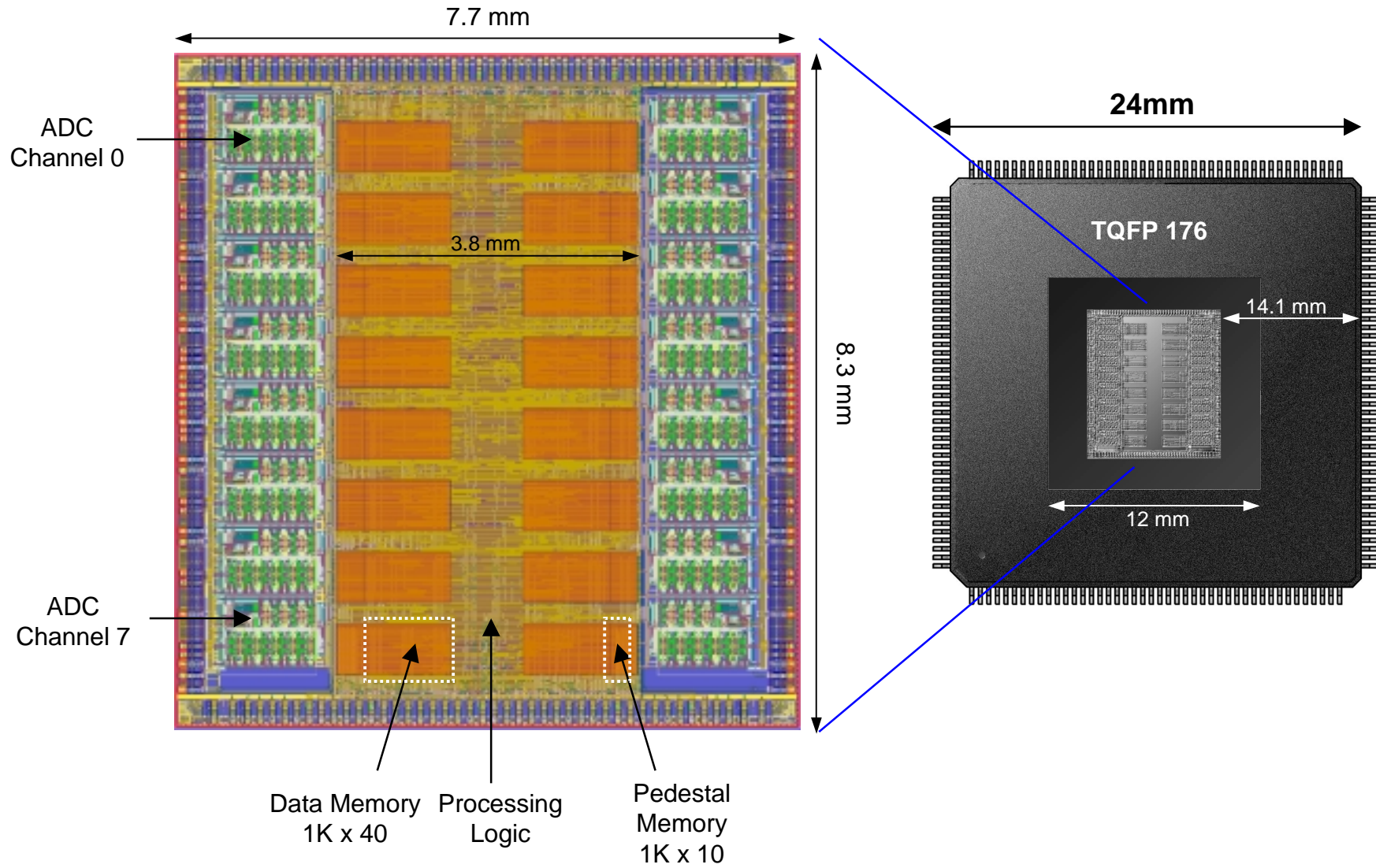
FRONT-END SIGNAL PROCESSING



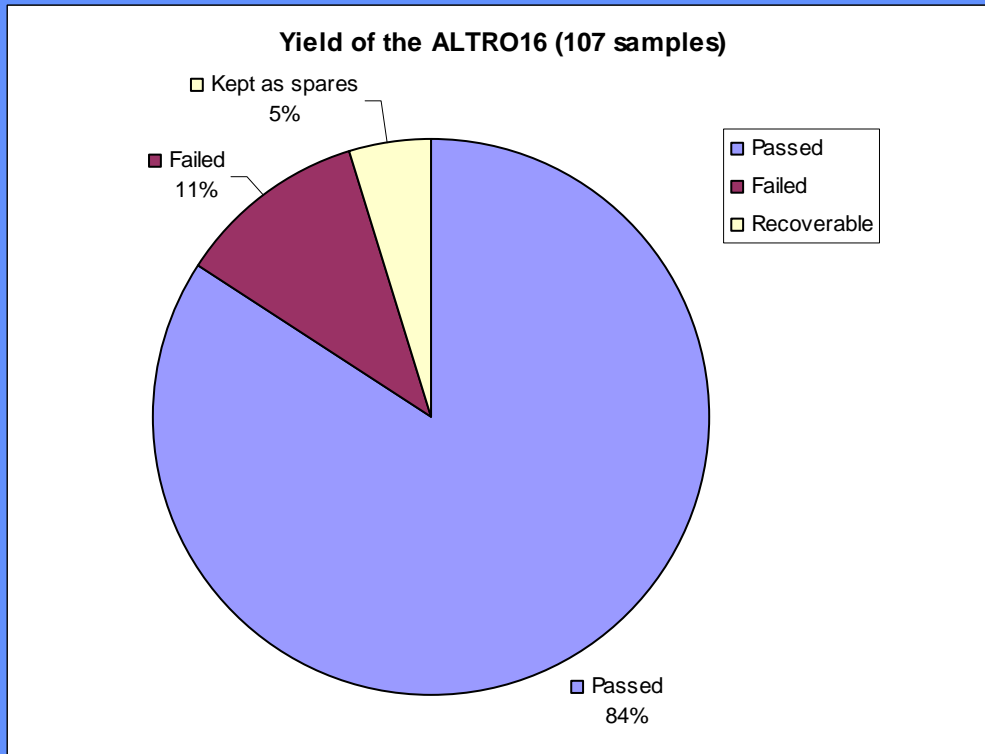
FRONT-END SIGNAL PROCESSING



Layout and Package



YIELD



Recoverable chips correspond to single and double bit stuck in the Memories

The Specific location of single bit stuck can be known, and the error can be corrected while de-formatting the data packet.

Failure Analysis

