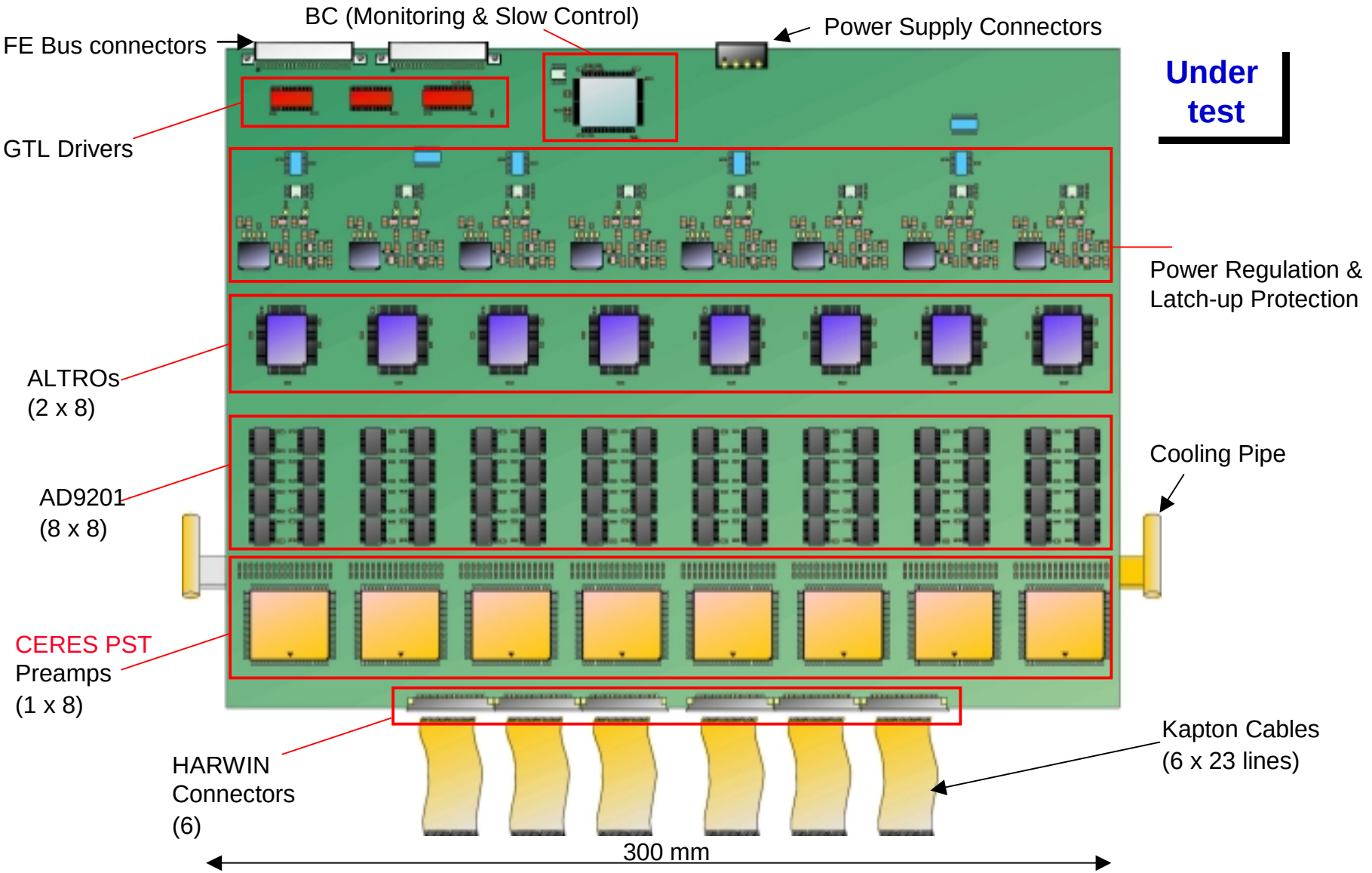
FRONT END CARD

ALICE TPC Meeting

GSI (Darmstadt), December 11, 2001

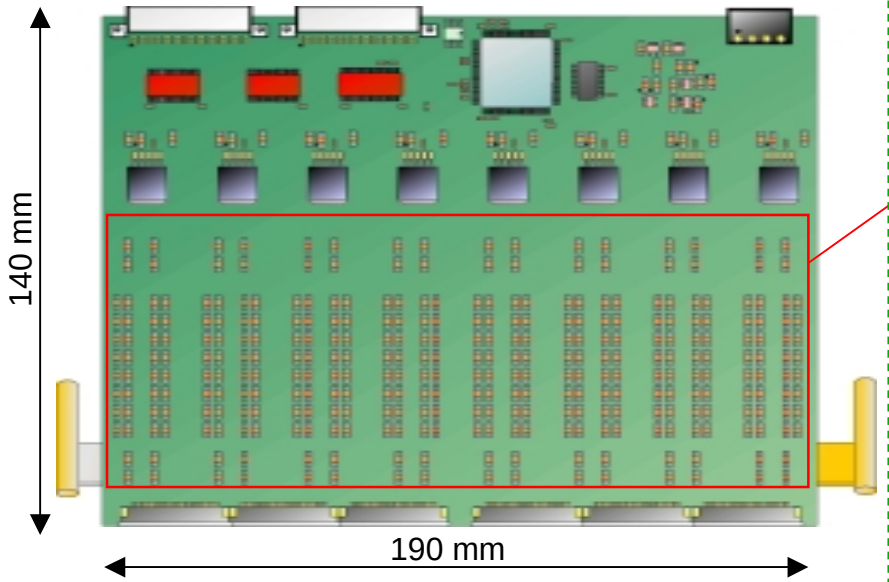
OUTLINE

- **Summary of the prototyping activities**
- **New FEC design**
- **Future work**


FE Bus connectors
BC (Monitoring & Slow Control)
Power Supply Connectors
Under test
GTL Drivers
Power Regulation & Latch-up Protection
ALTROs (2 x 8)
AD9201 (8 x 8)
Cooling Pipe
CERES PST Preamps (1 x 8)
HARWIN Connectors (6)
Kapton Cables (6 x 23 lines)
300 mm

Under test

Size of Functional Prototype

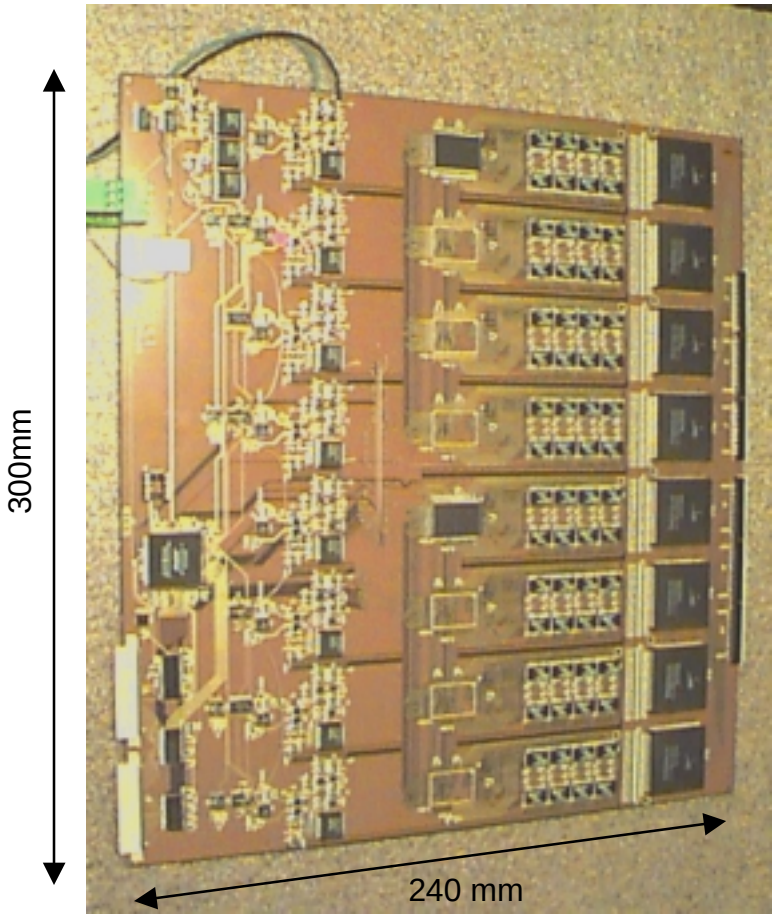


Resistors to emulate power dissipation of:

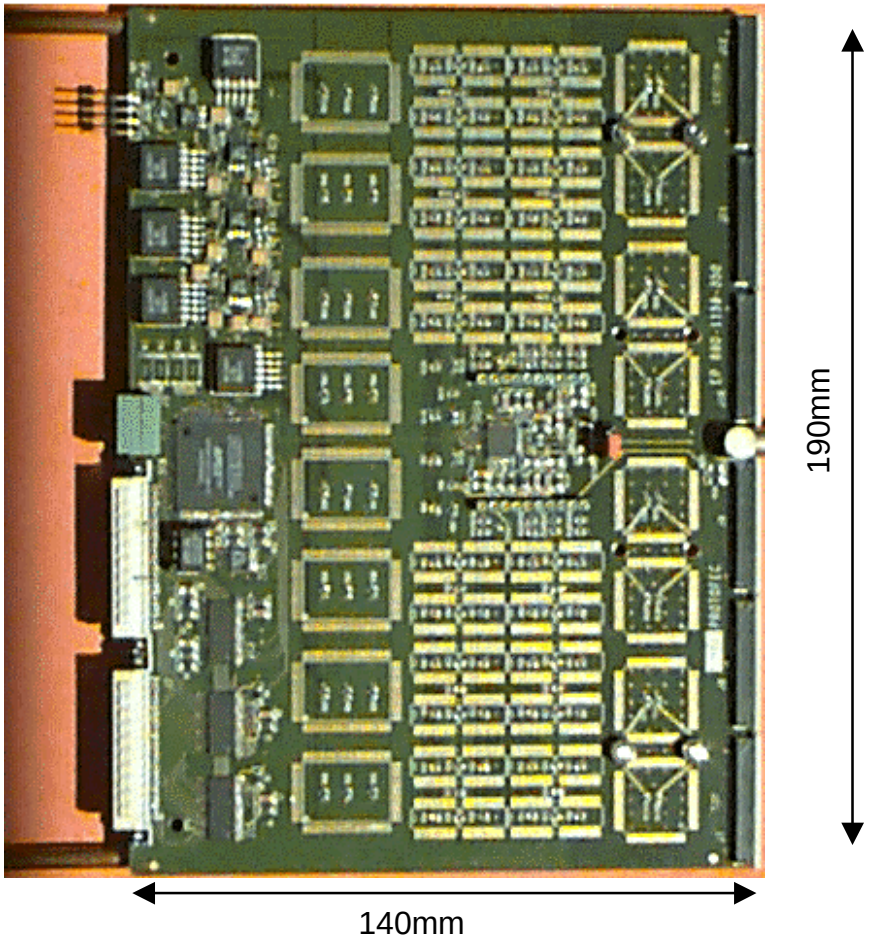
- ALTROs
- ADCs
- PASAs

FRONT-END CARD PROTOTYPES (2001)

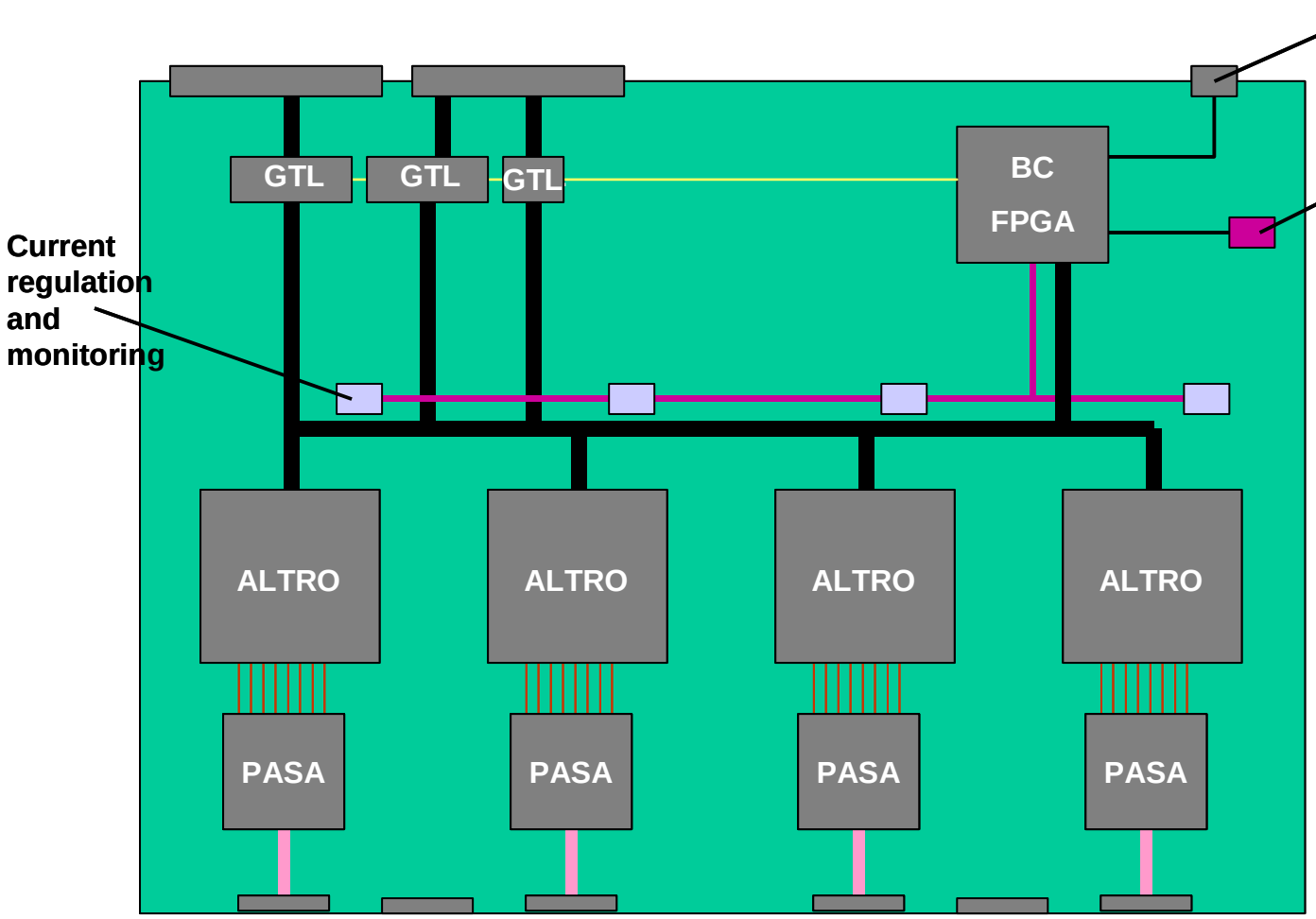
FUNCTIONAL PROTOTYPE



LIGHT PROTOTYPE



NEW FRONT-END CARD PROTOTYPE (FEB 2002)

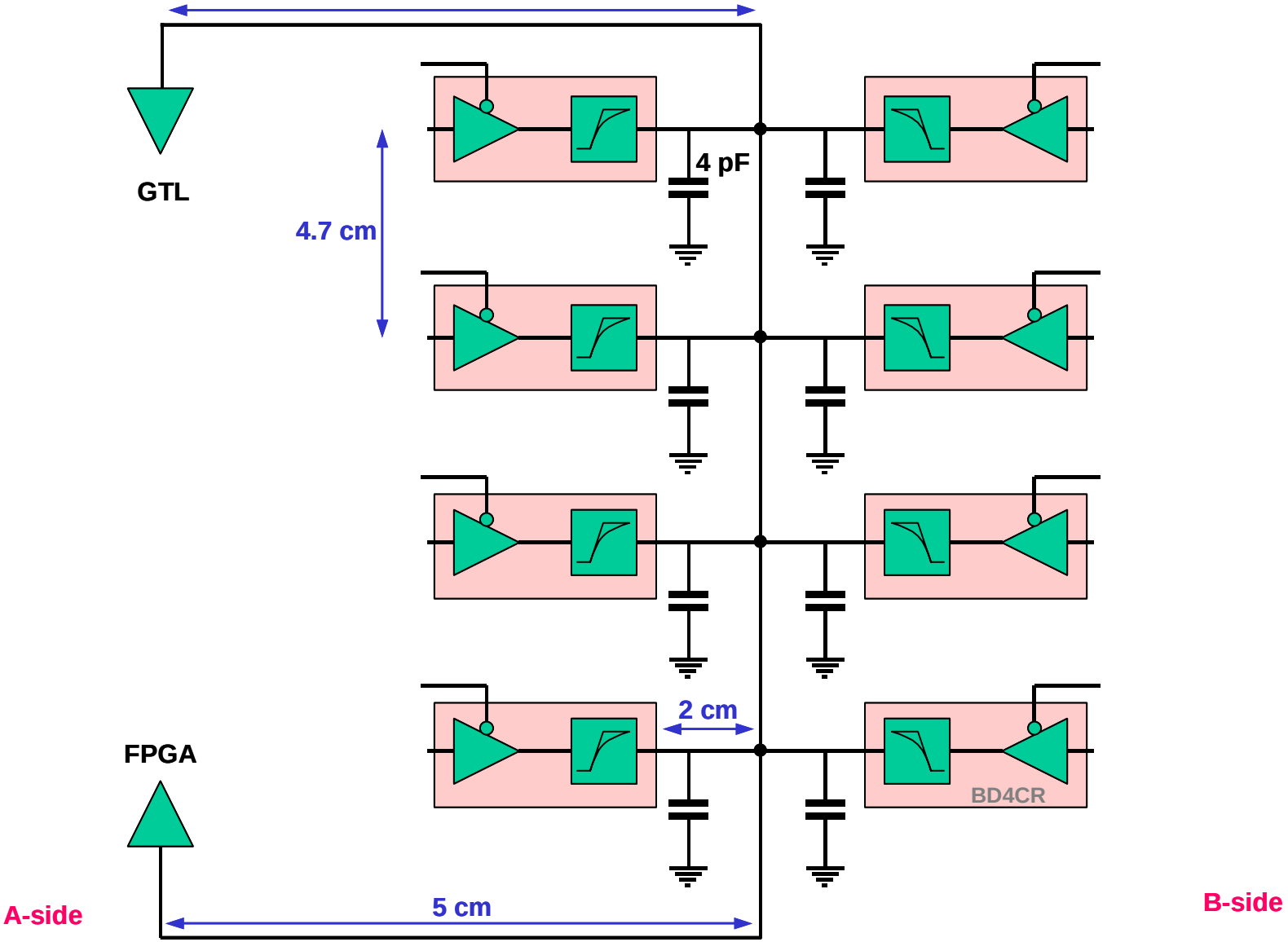


Another 4 on the back side

8 layers PCB

- 4 wires layers
- 1 digital gnd
- 1 analogue gnd
- 1 digital vdd
- 1 analogue vcc

FEC INTERNAL BUS



FUTURE WORK

- Optimization of the FEC internal data bus
- Selection of the technology for the implementation of the board controller:
  - SRAM FPGA (ALTERA) vs. anti-fuse FPGA (ACTEL)
  - Hardcopy FPGA (ALTERA)
  - Hardwired gate array (two masks technology)
- Design, implementation and test of the local slow control bus
- Test of the distribution of the clock signals (sampling clock and readout clock) and write a proposal:
  - Bus line vs. point-to-point connection
  - distribution of a single clock line (40 MHz) and generation of the sampling clock in the RCU by the use of PLL, or distribution of two independent clock lines?
- Define a scheme for a bulky electrical connection of the FEC ground to the ROC frame