ALTRO CHIP

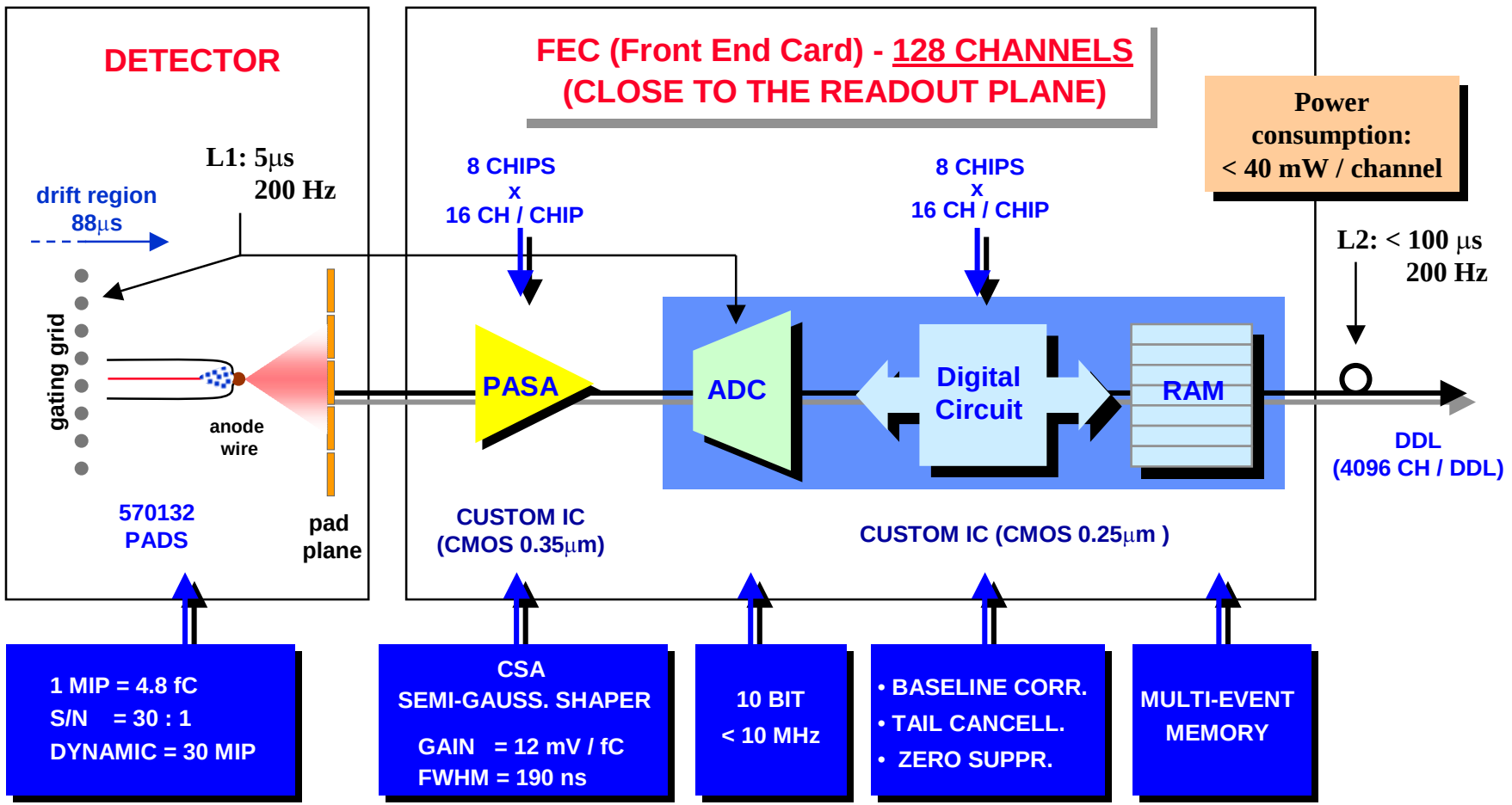
ALICE TPC Meeting

GSI (Darmstadt), December 11, 2001

OUTLINE

- **Summary of the prototyping activities**
- **Chip main features**
- **System for the chip characterization**
- **Documentation**

FEE ARCHITECTURE

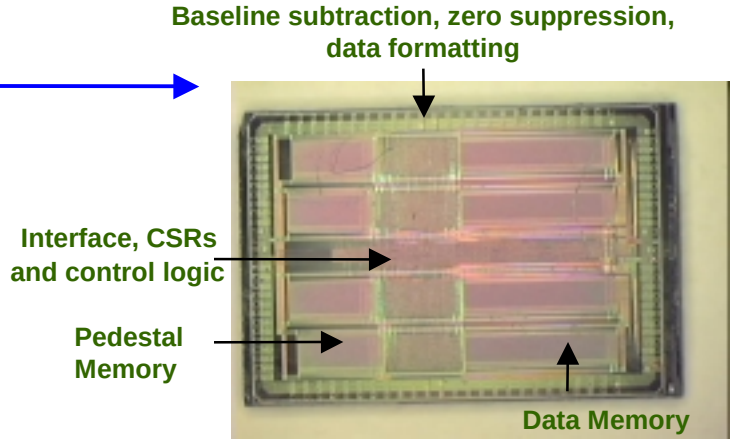


1st prototype ('98):

- Digital circuit: pedestal subtraction, zero suppression, data formatting, data memory (512 x 10-bit words)
- implementation with FPGAs (1ch / FPGA) for the readout of FTPC (NA49)

2nd prototype ('99):

- Digital circuit: pedestal subtraction, zero suppression, data format, data memory (768 x 10-bit words)
- 4 channels: (6 x 9 mm2)
- AMS CMOS 0.6 um
- fully working

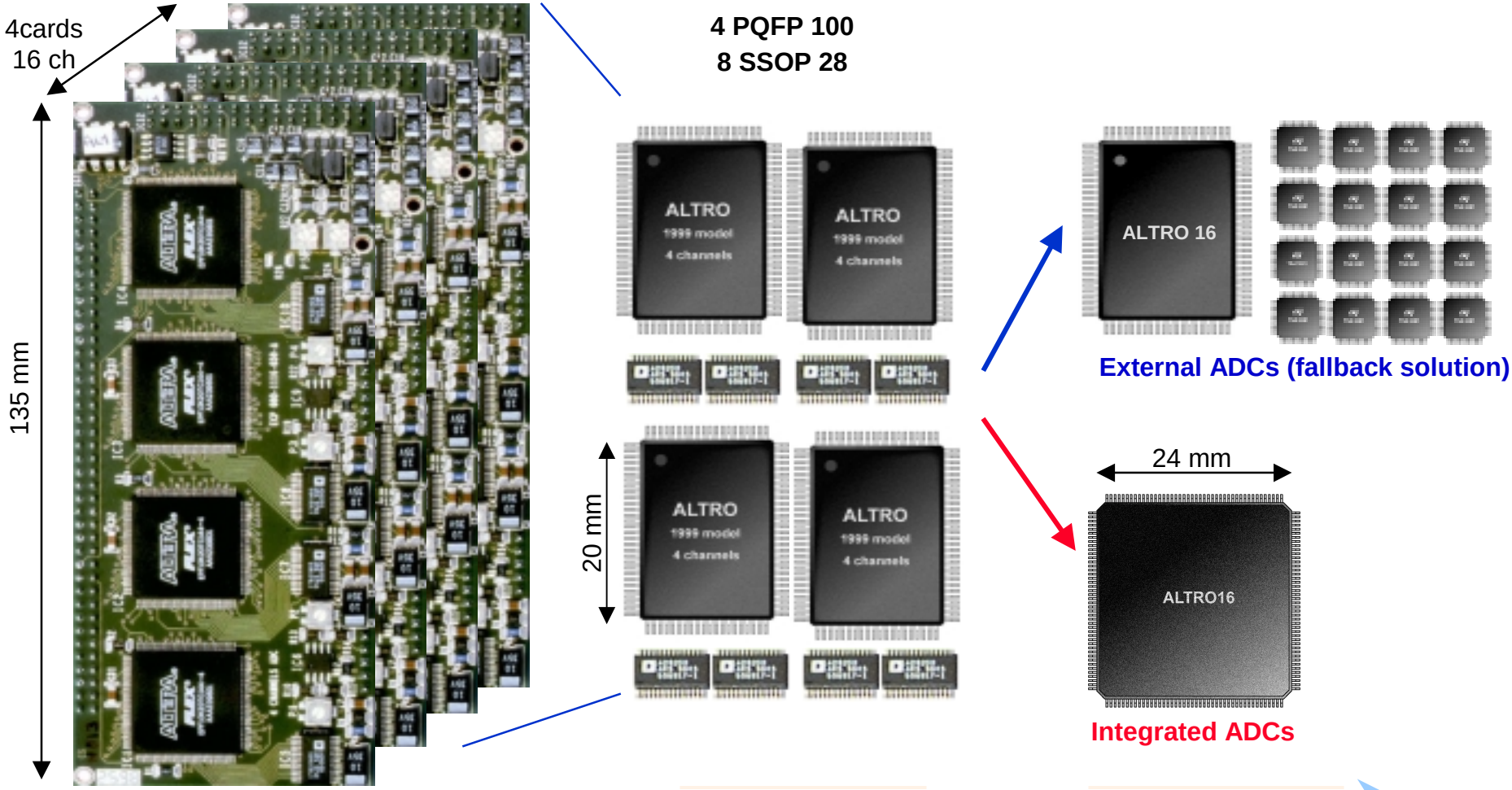


CHIP LAYOUT

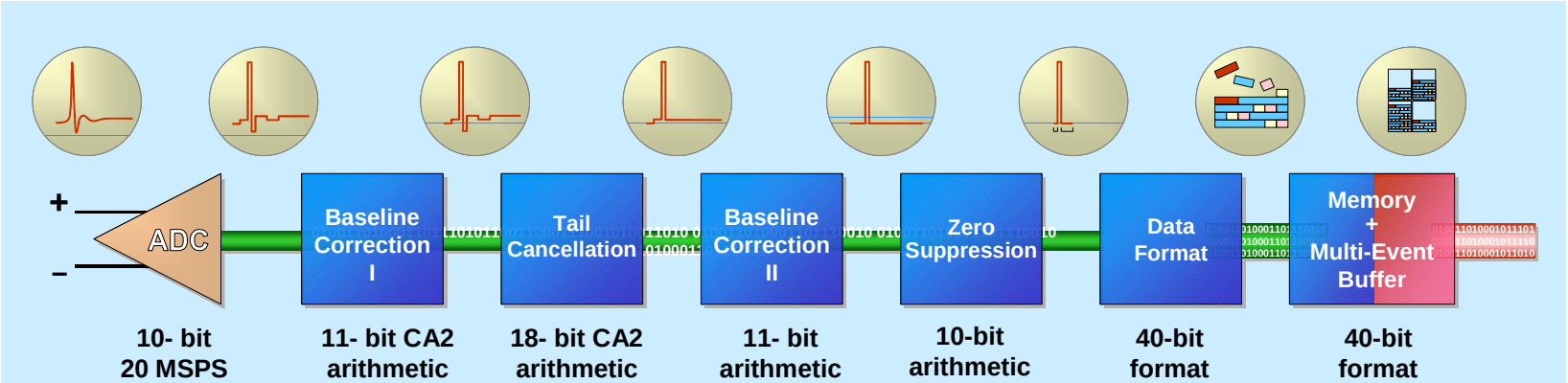
3rd prototype ('01):

- Mixed analogue-digital circuit: ADC, pedestal correction and subtraction, tail cancellation, zero suppression, data formatting, data memory (4K x10-bit words)
- 16 channels - ST CMOS 0.25um
- Contract procurement: Jul '01
- Submission: Sep '01
- Delivery (50 packaged samples): Jan '02
- Testing: Jan – Feb '02

ALTRO CHIP – SUMMARY OF THE PROTOTYPING ACTIVITIES



ALICE TPCE READOUT CHIP (ALTRO-16)

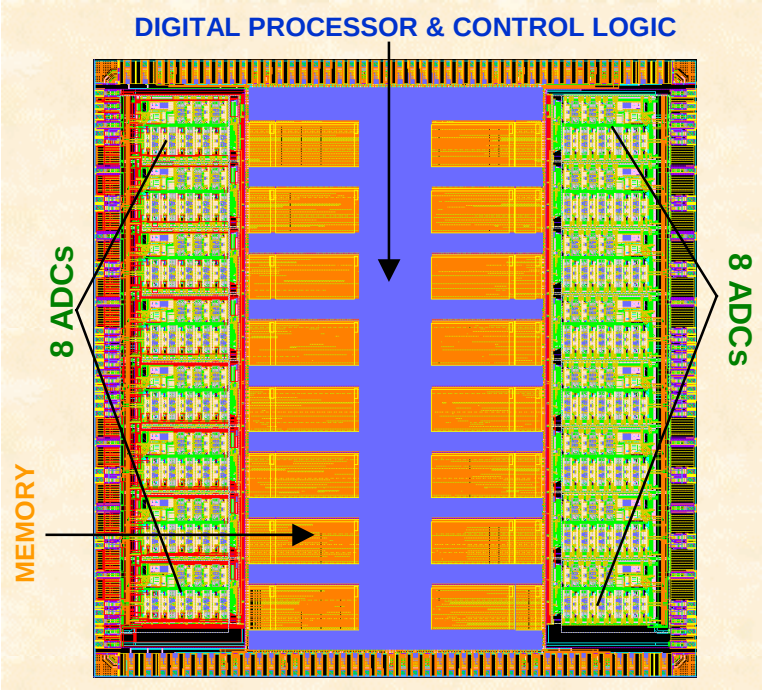


SAMPLING CLOCK 20 MHz

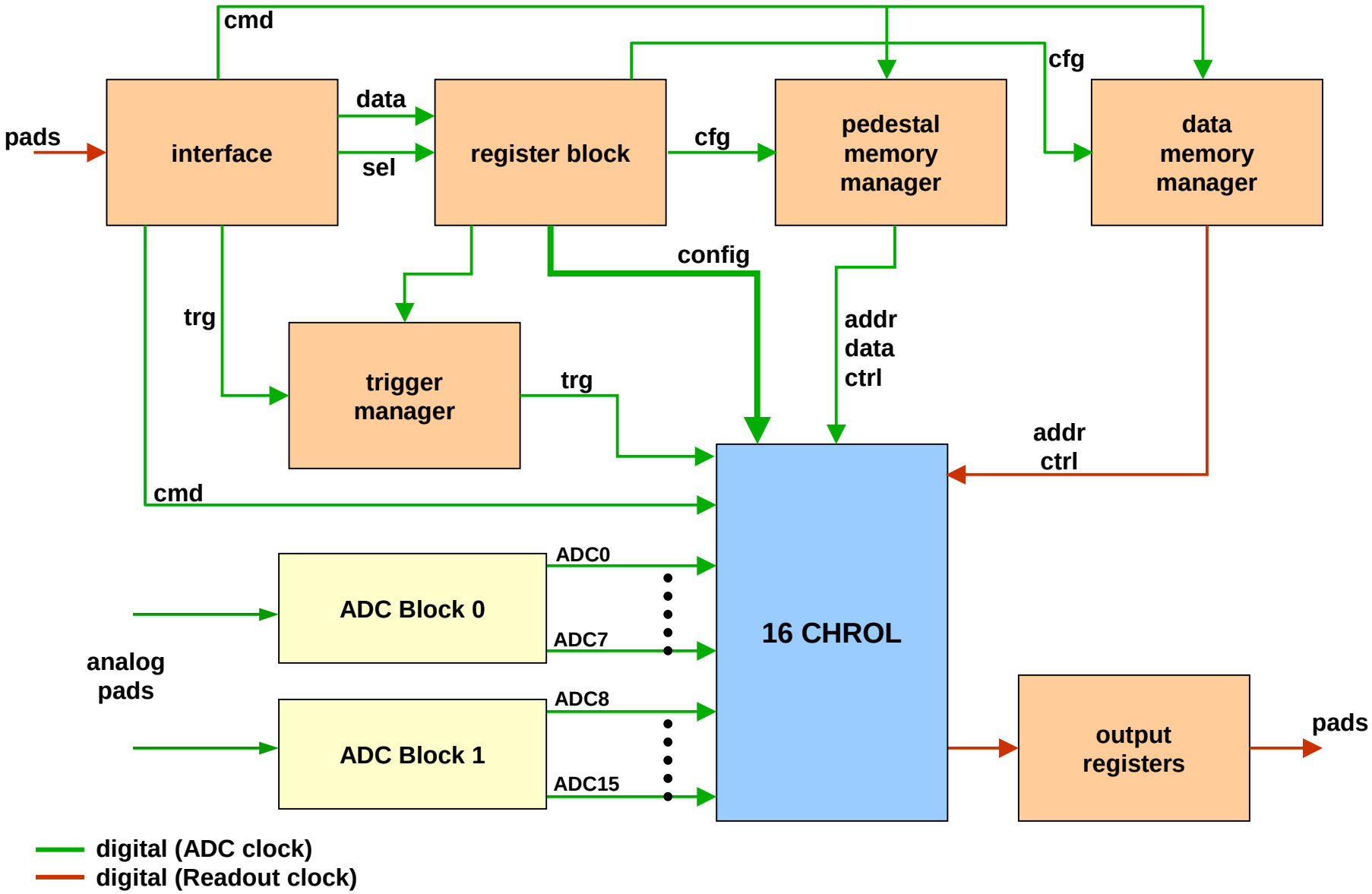
READOUT CLOCK 40 MHz

16-ch signal digitizer and processor

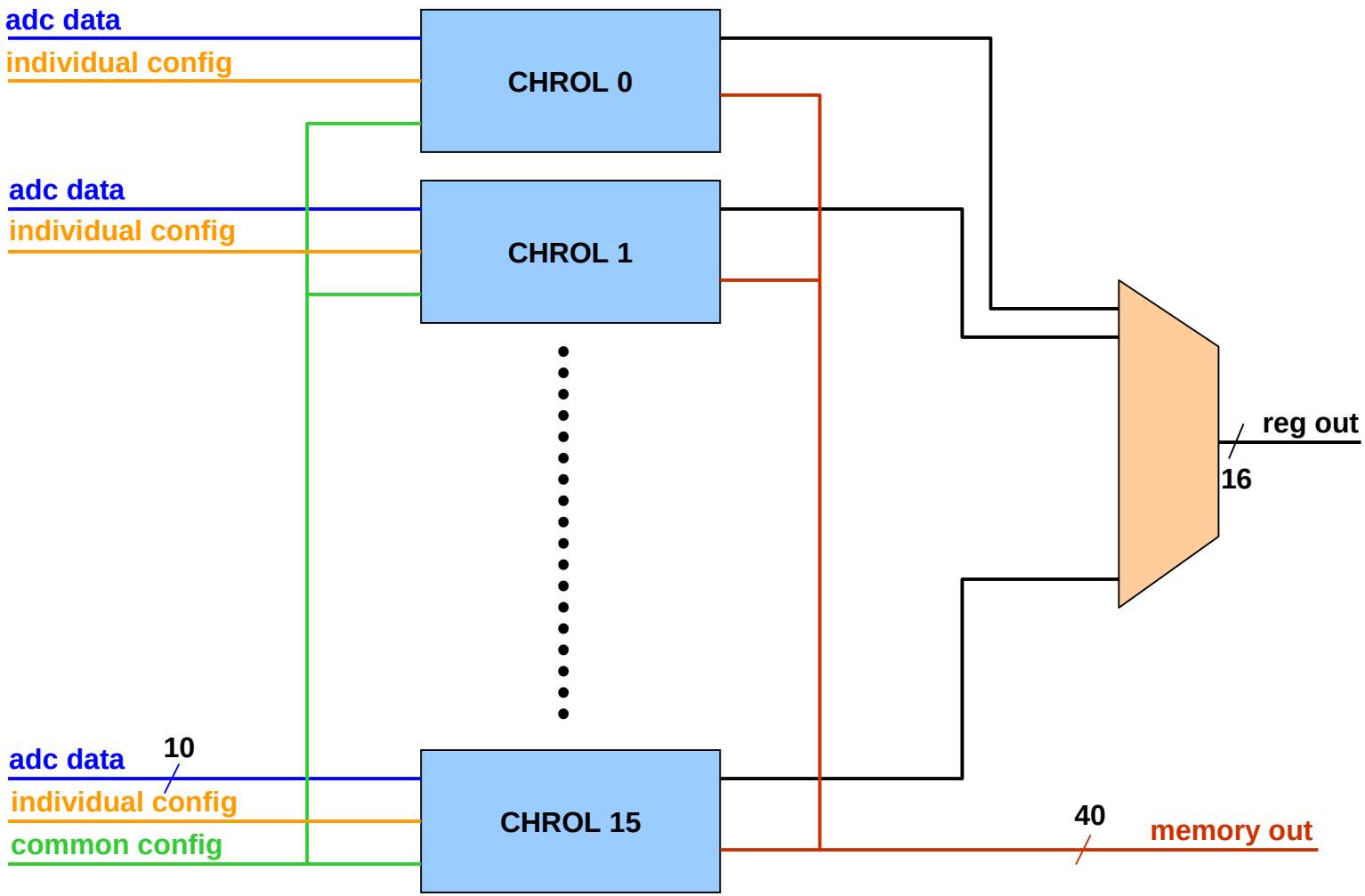
- HCMOS7 0.25 μm (ST)
- area: 64 mm^2
- power: 29 mW / ch
- PACKAGE: TQFP176
- SEU protection (Hamming)



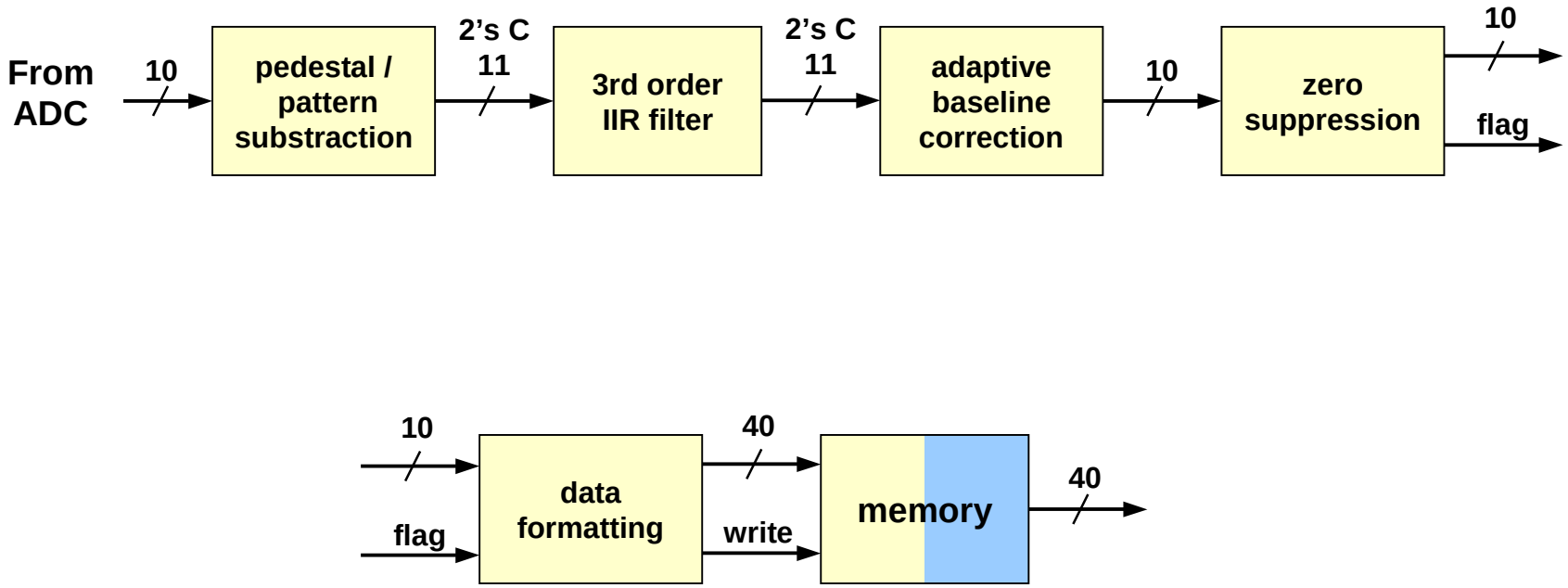
CORE BUILD-UP



CHANNEL BUILD-UP

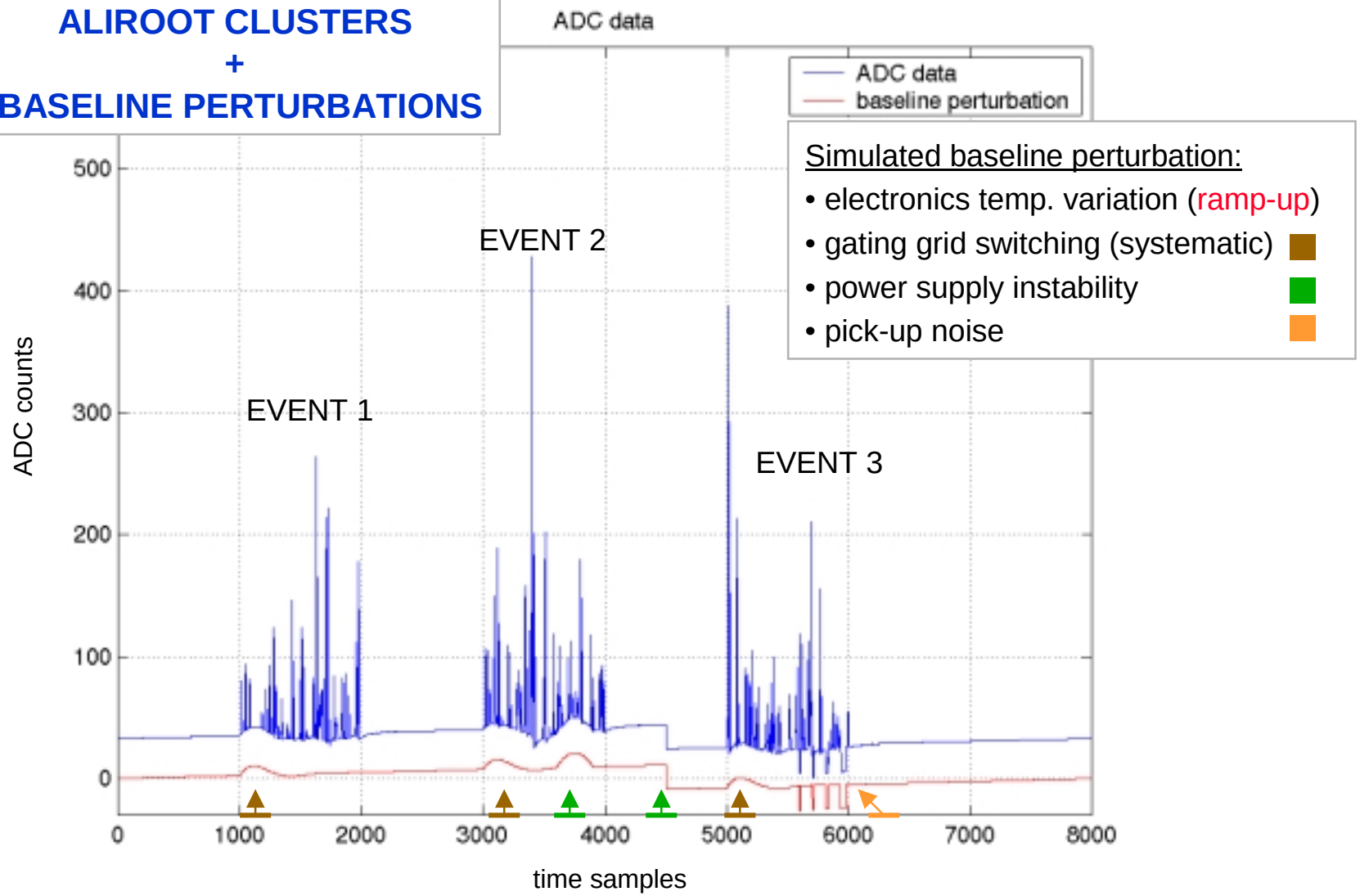


CHANNEL DATA PATH



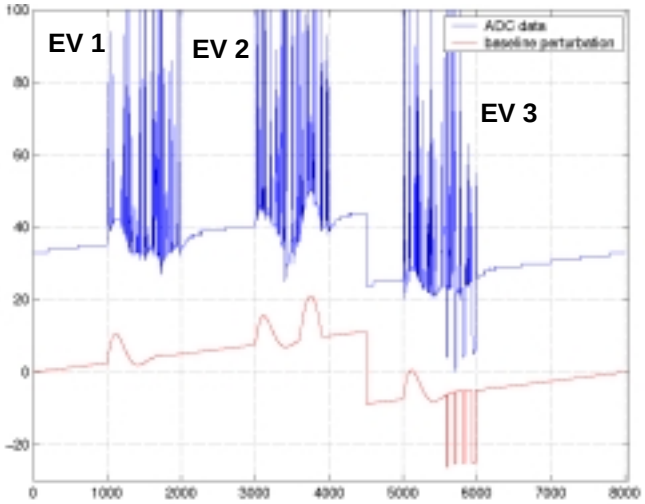
FRONT-END SIGNAL PROCESSING

ALIROOT CLUSTERS
+
BASELINE PERTURBATIONS

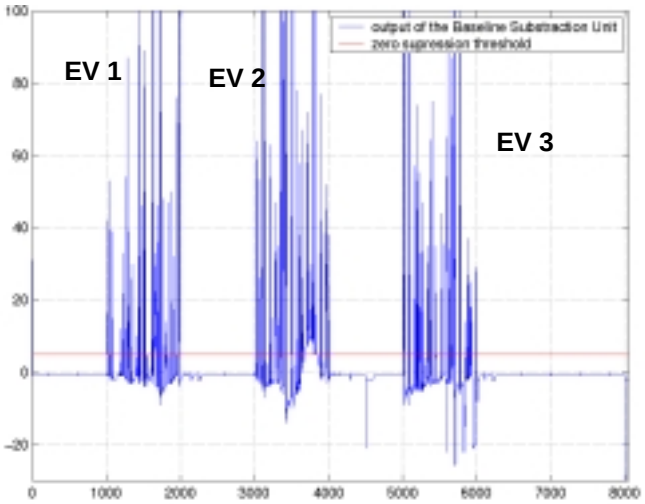


FRONT-END SIGNAL PROCESSING

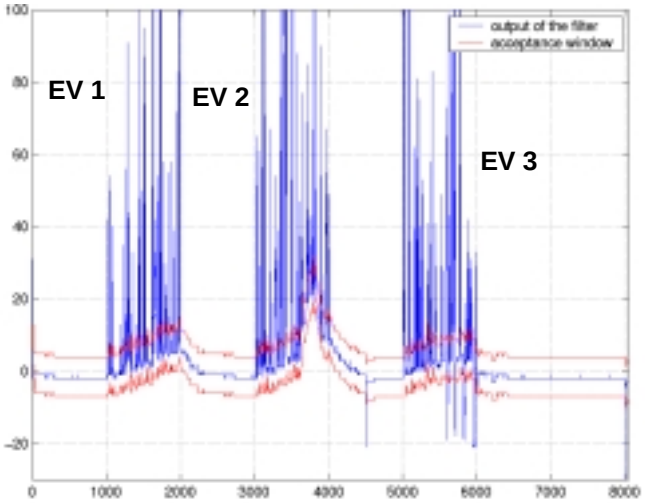
INPUT SIGNAL



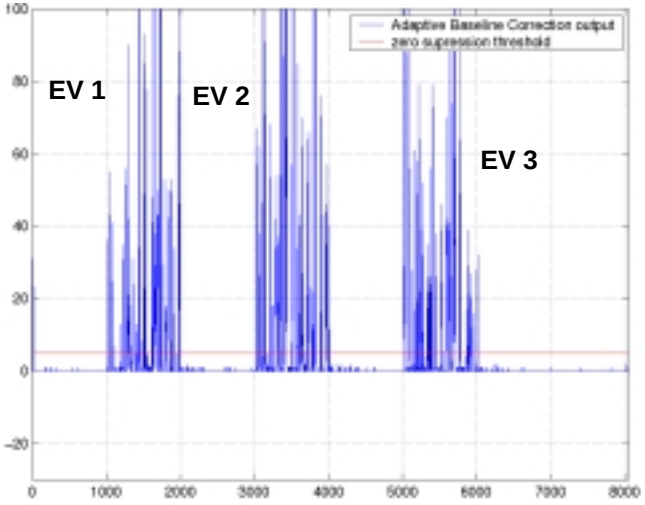
AFTER 1st BASELINE CORRECTION



AFTER TAIL CANCELLATION

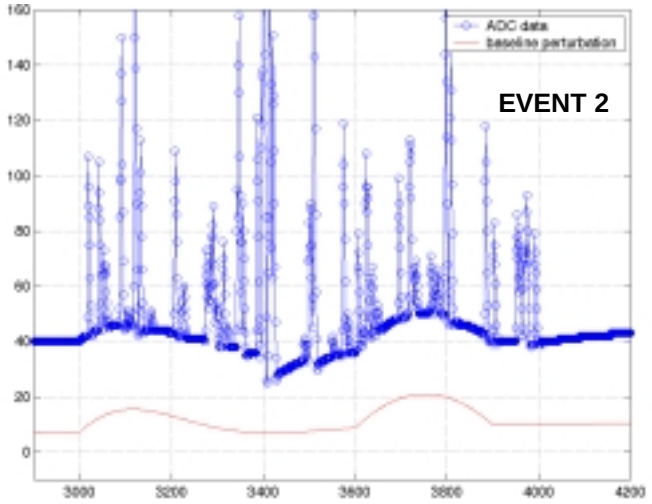


AFTER 2nd BASELINE CORRECTION

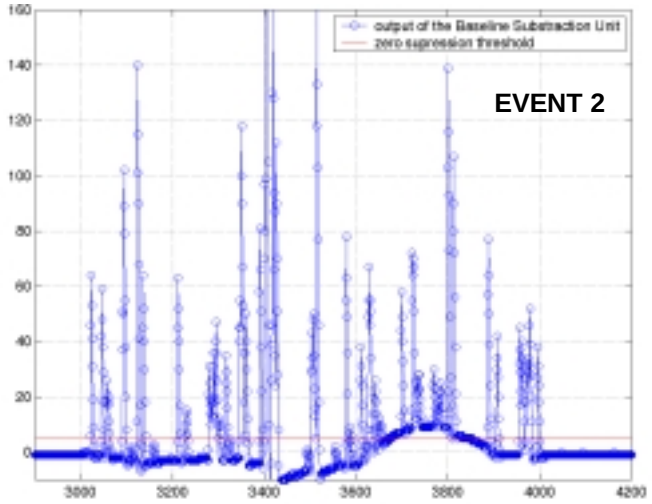


FRONT-END SIGNAL PROCESSING

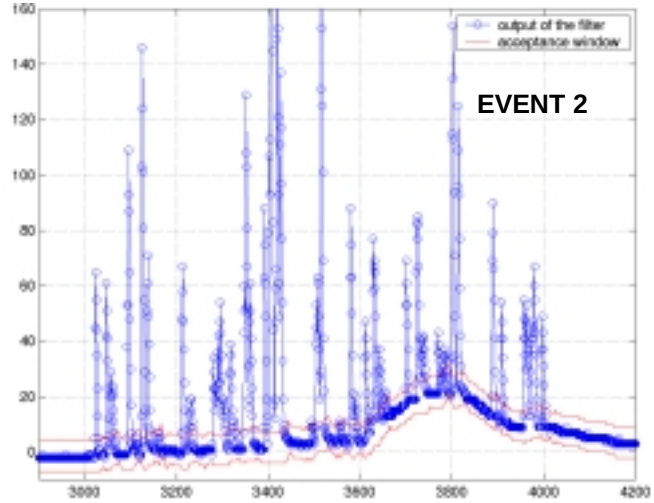
INPUT SIGNAL



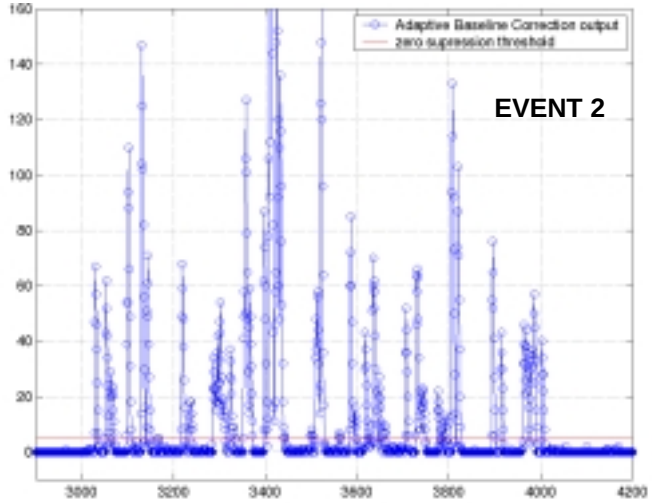
AFTER 1st BASELINE CORRECTION



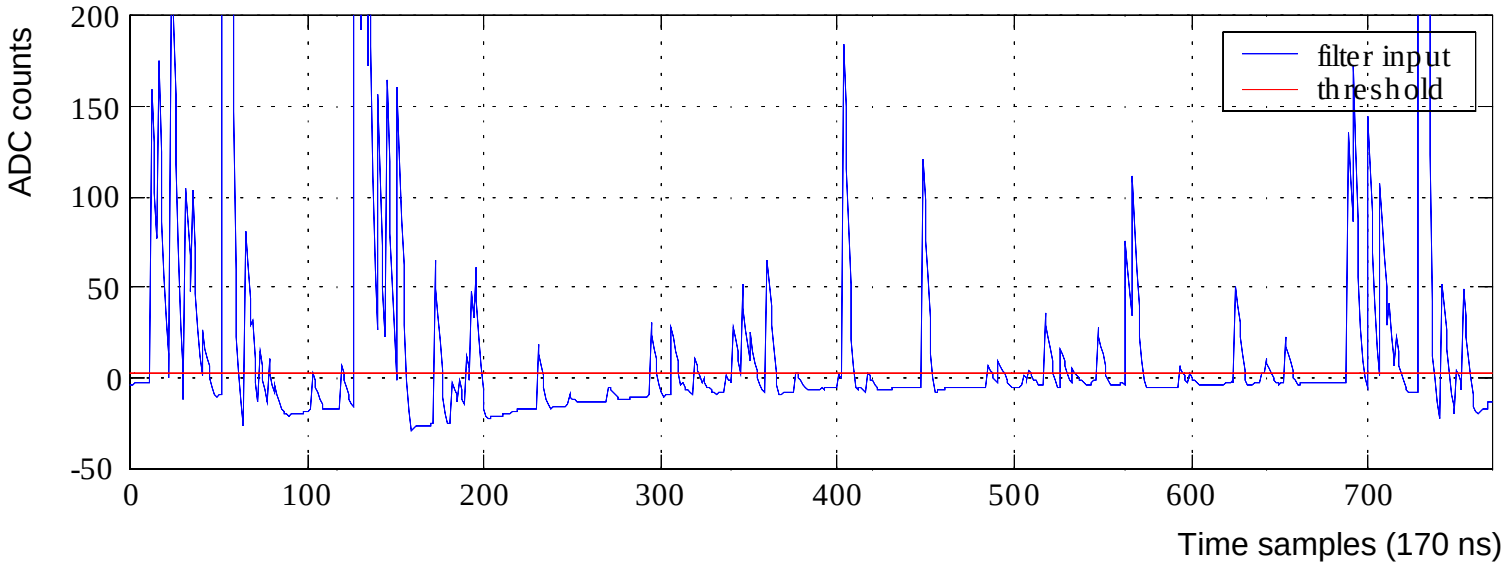
AFTER TAIL CANCELLATION



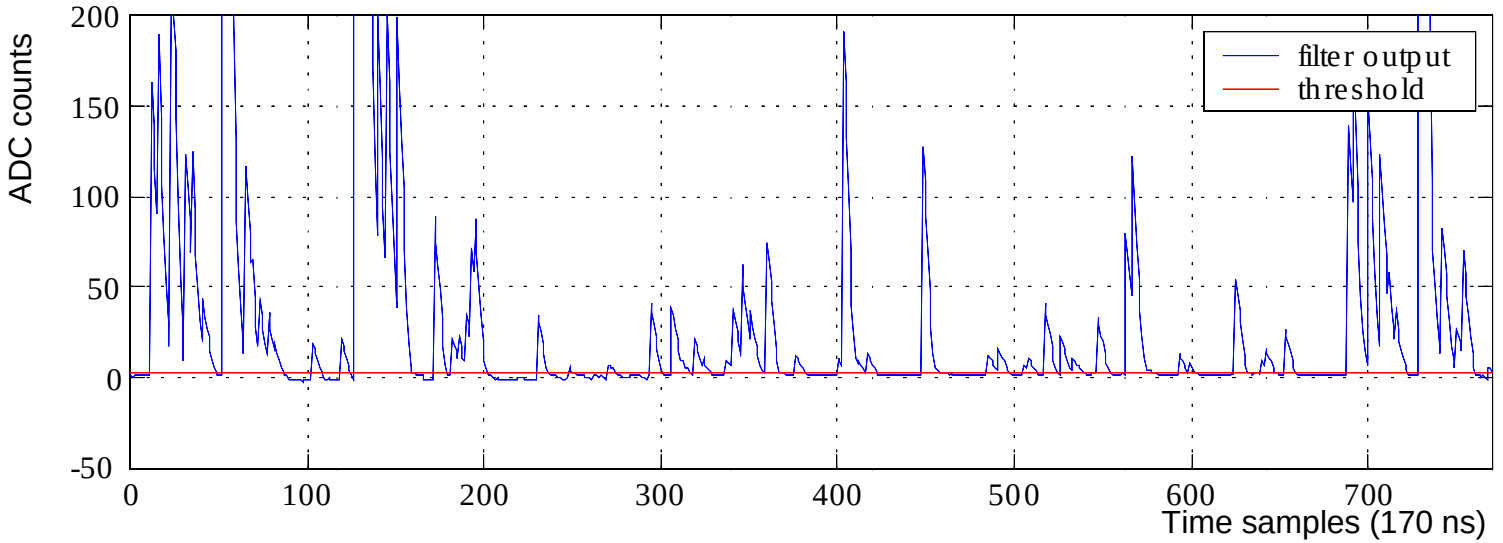
AFTER 2nd BASELINE CORRECTION



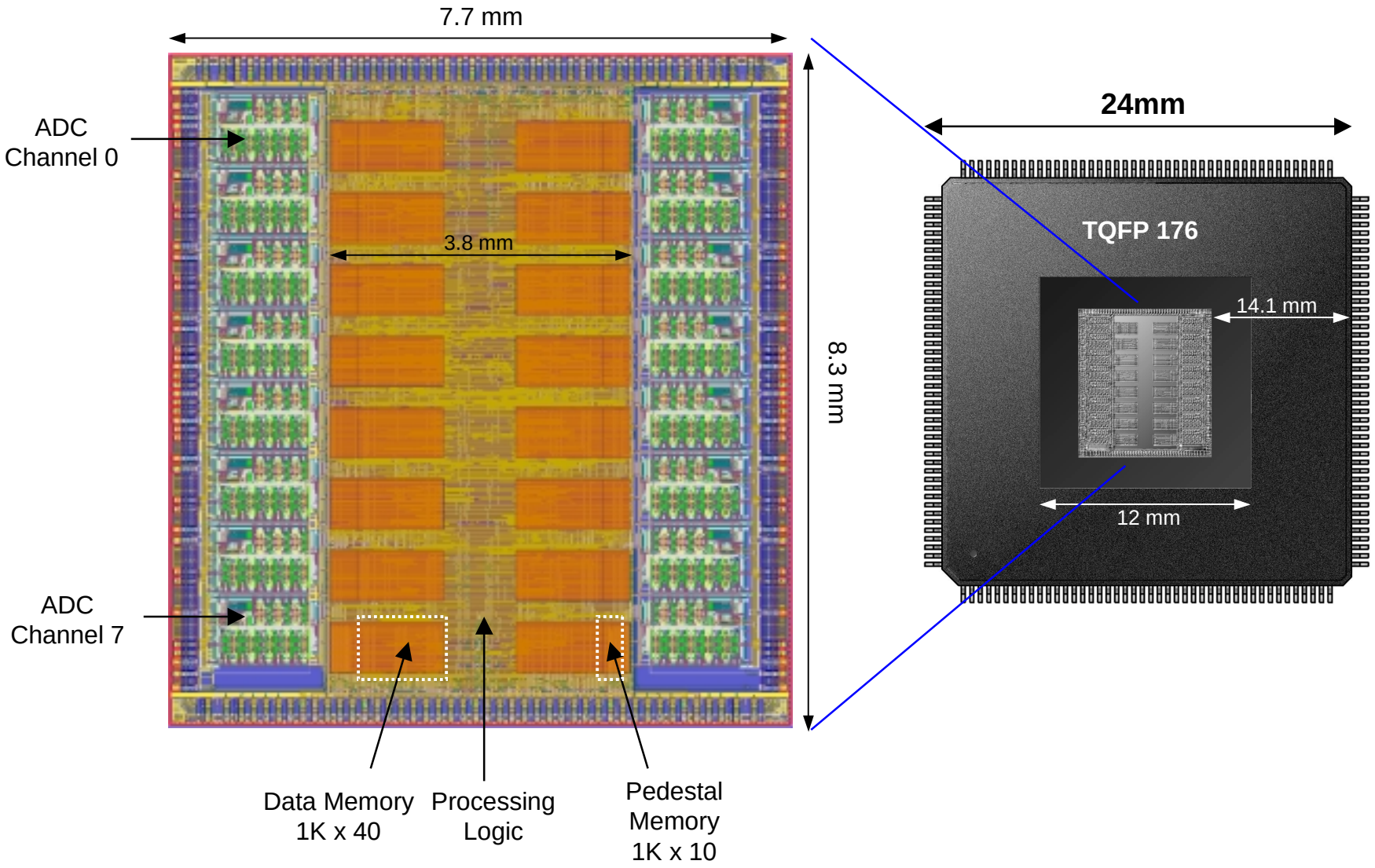
DIGITAL TAIL CANCELLATION PERFORMANCE



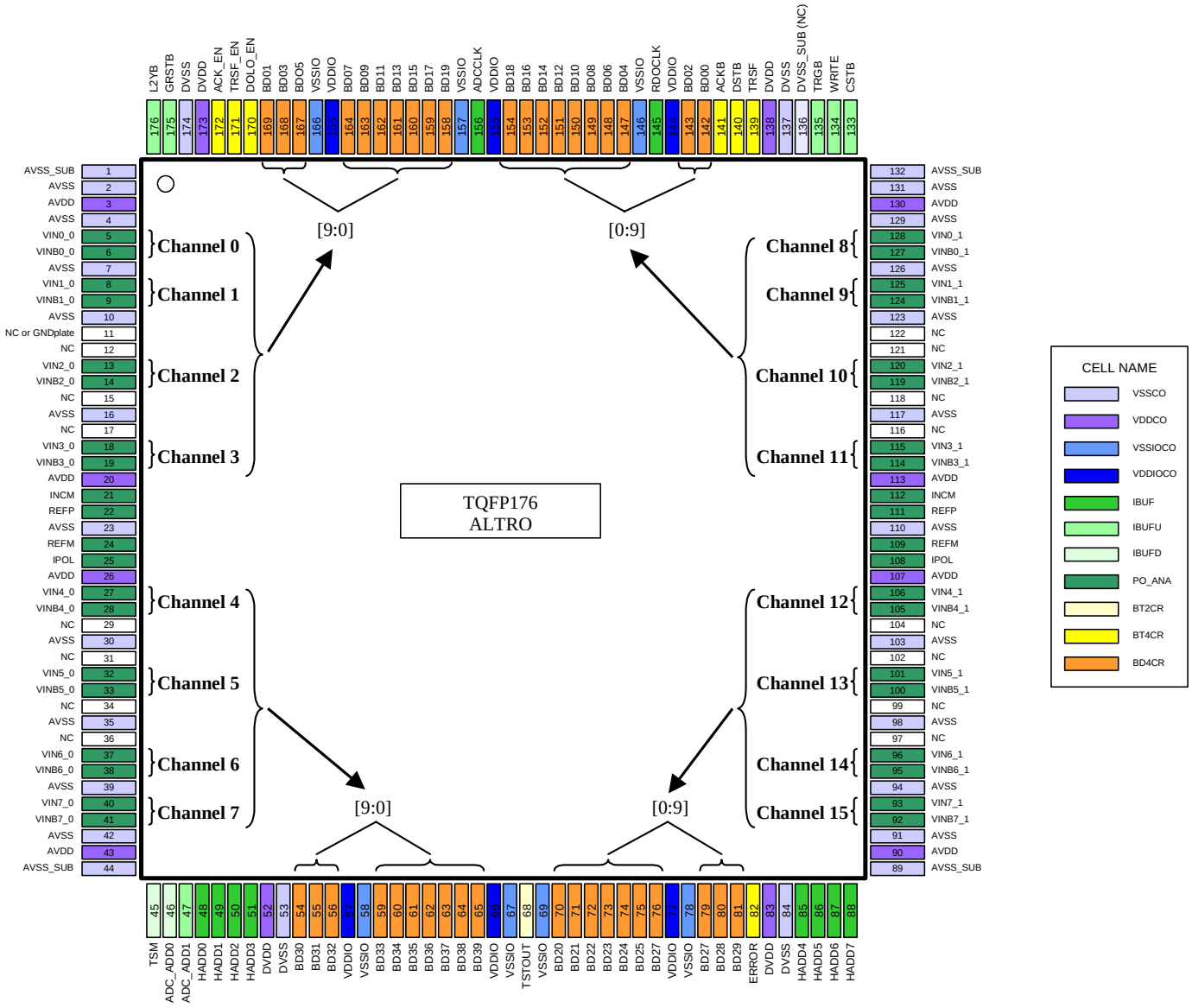
Filtered data and fixed threshold



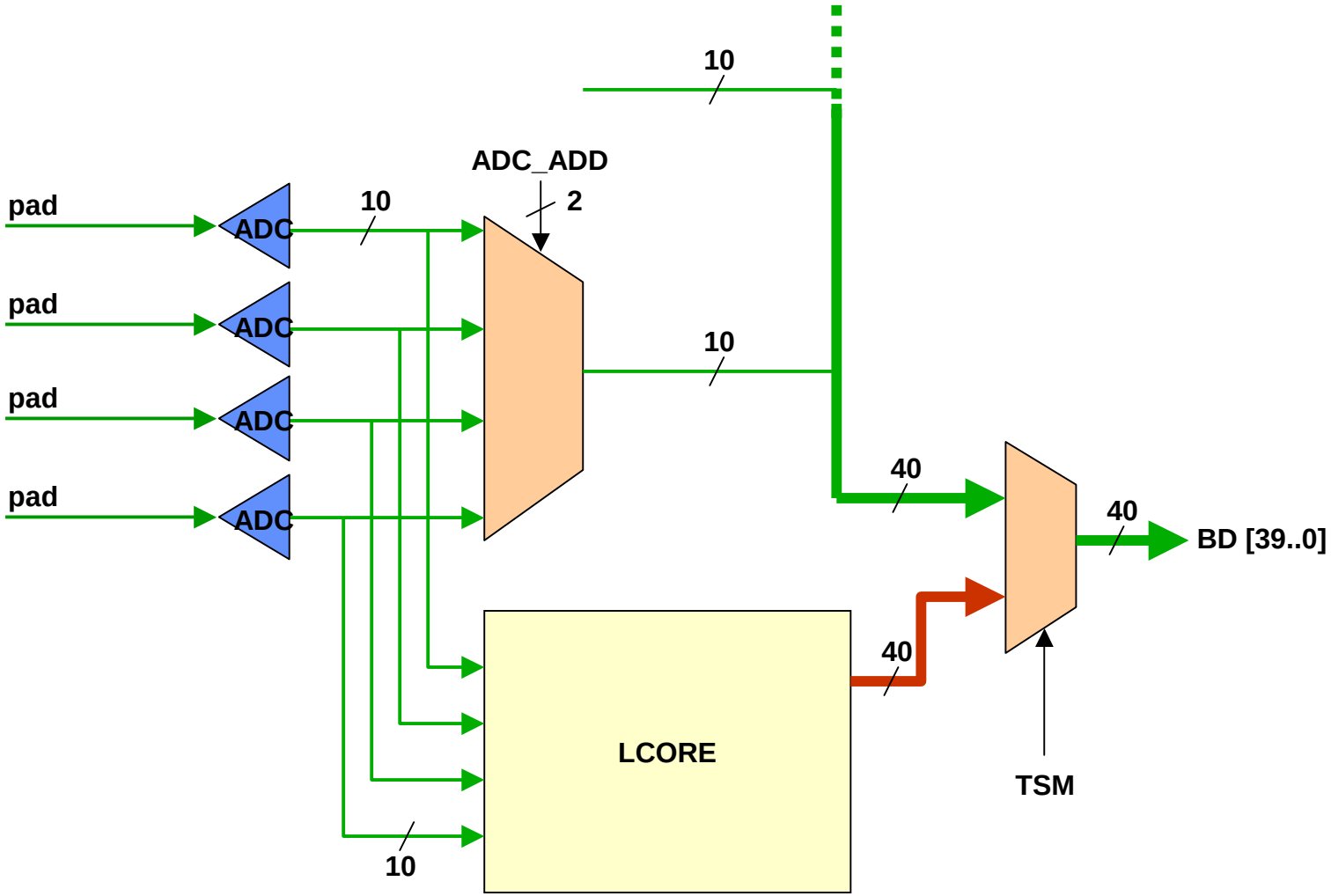
LAYOUT AND PACKAGE



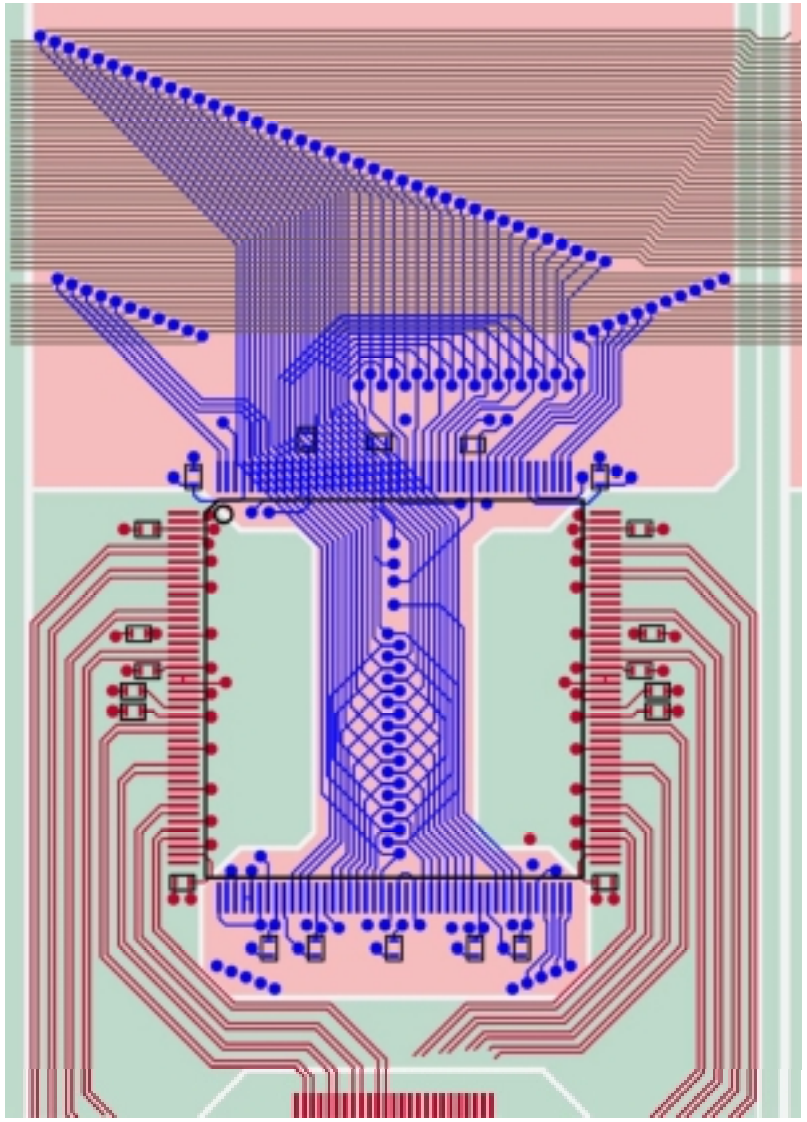
PACKAGE AND PINOUT



ADC TEST FEATURE



PCB DESIGN



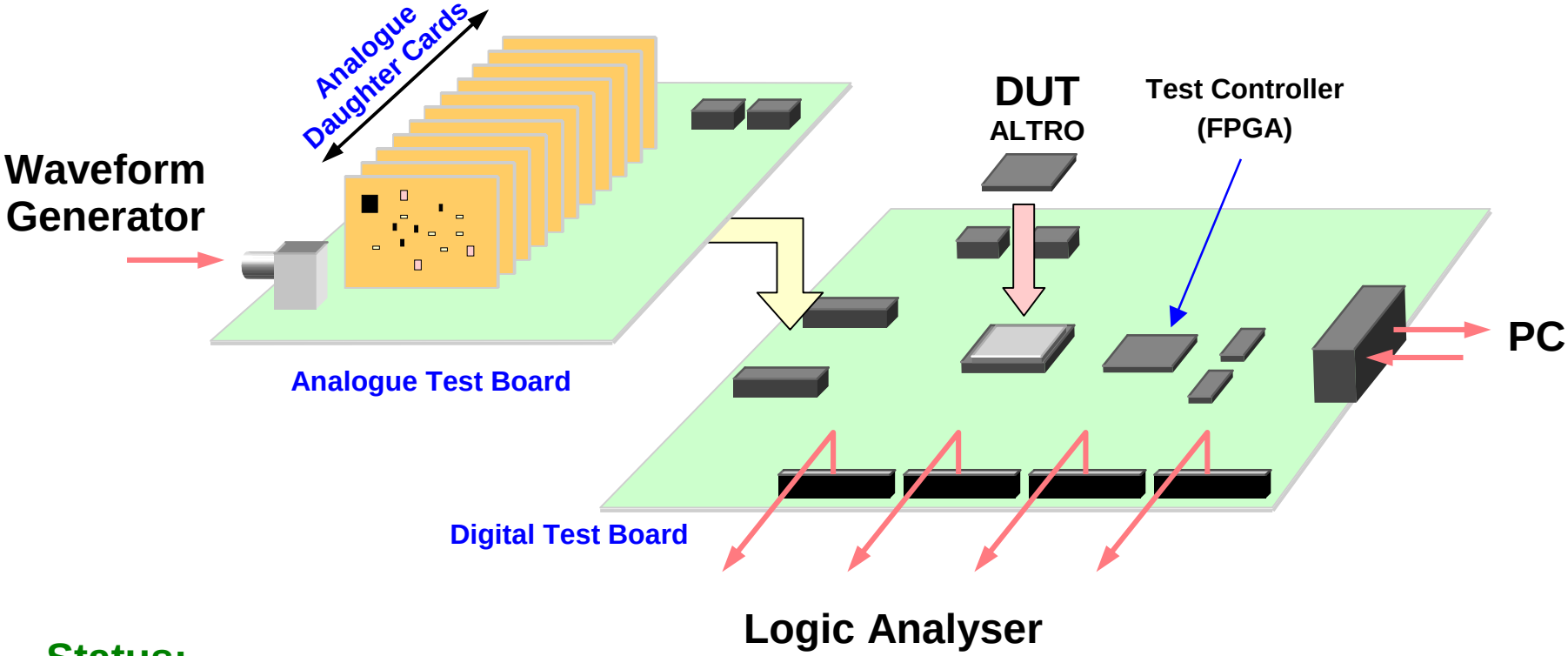
The layout of the chip has been optimised to minimise the influence of the digital circuitry on the integrated ADCs.

Supply (VCC / GND) for the digital core

Supply (VCC / GND) for the ADC

The supply voltages for the PASA are distributed on a different plane

Test set-up for the characterization of the ALTRO prototype



Status:

Analogue Daughter Cards: ready

Analogue Test Board: delivered in wk 49 - test in wk 50 and 51

Digital Test Board: delivery in wk 50 – test in wk 51

FPGA logic: ready

PC software: basic tests routines ready

DOCUMENTATION AVAILABLE ON THE WEB

http://cern.ch/ep-ed-alice-tpc

- ALTRO User Manual
- Interface Module (Verilog RTL description)
- Interface Driver (Verilog behavioral description)