

+4V0IN\I

PASAGND\I

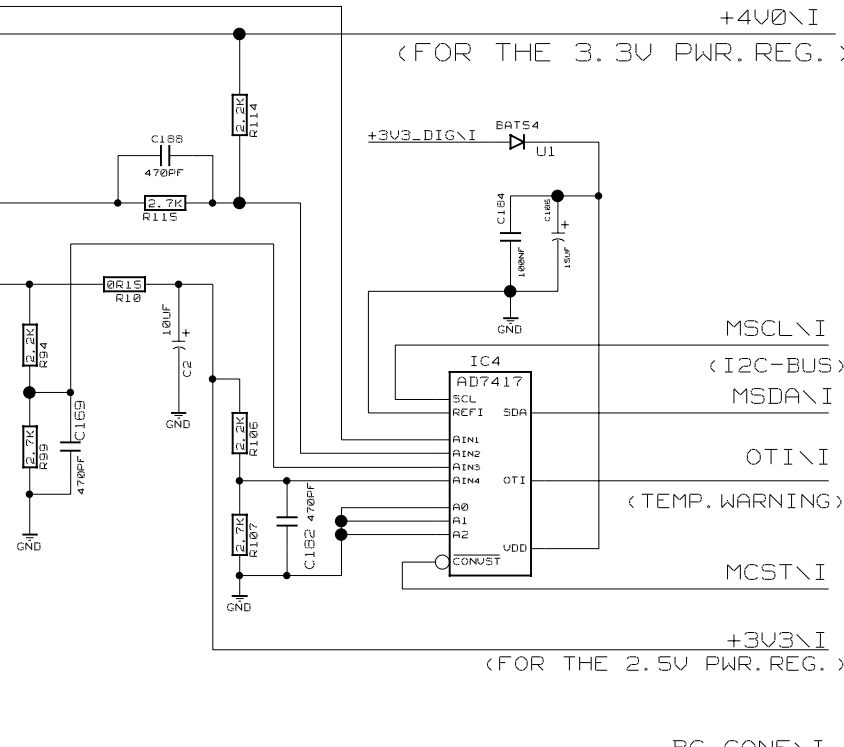
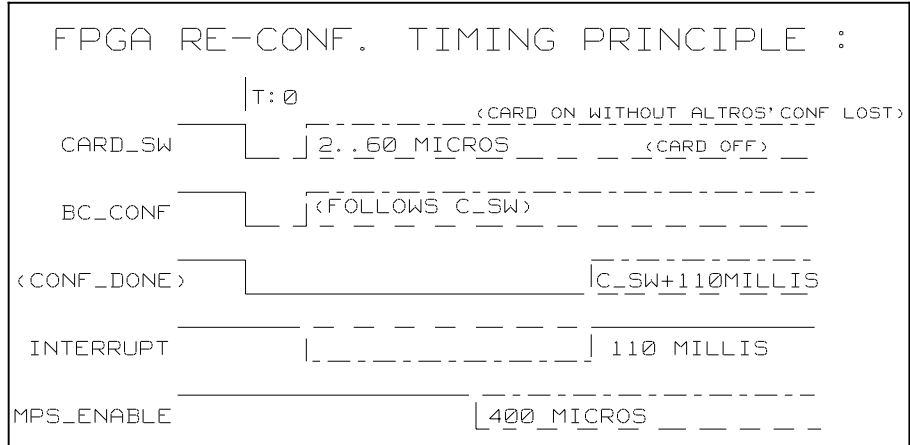
+3V3IN\I

+4V0\I

(FOR THE 3.3V PWR. REG.)

+3V3_DIG\I

+3V3\I
(FOR THE 2.5V PWR. REG.)



CARD_SW\I

(FROM BACKPLANE CONN)

CARD_SWAUX\I

(FROM I2C CONNECTOR)

BC_INT\I

(ACTIVE LOW)

MPS_ERROR\I

(OPEN DRAIN - ACTIVE LOW)

(240 MV FOR 39151 ERROR FLG / 40 MV FOR TC1173 ERROR FLG)

+4V0\I

BC_CONF\I

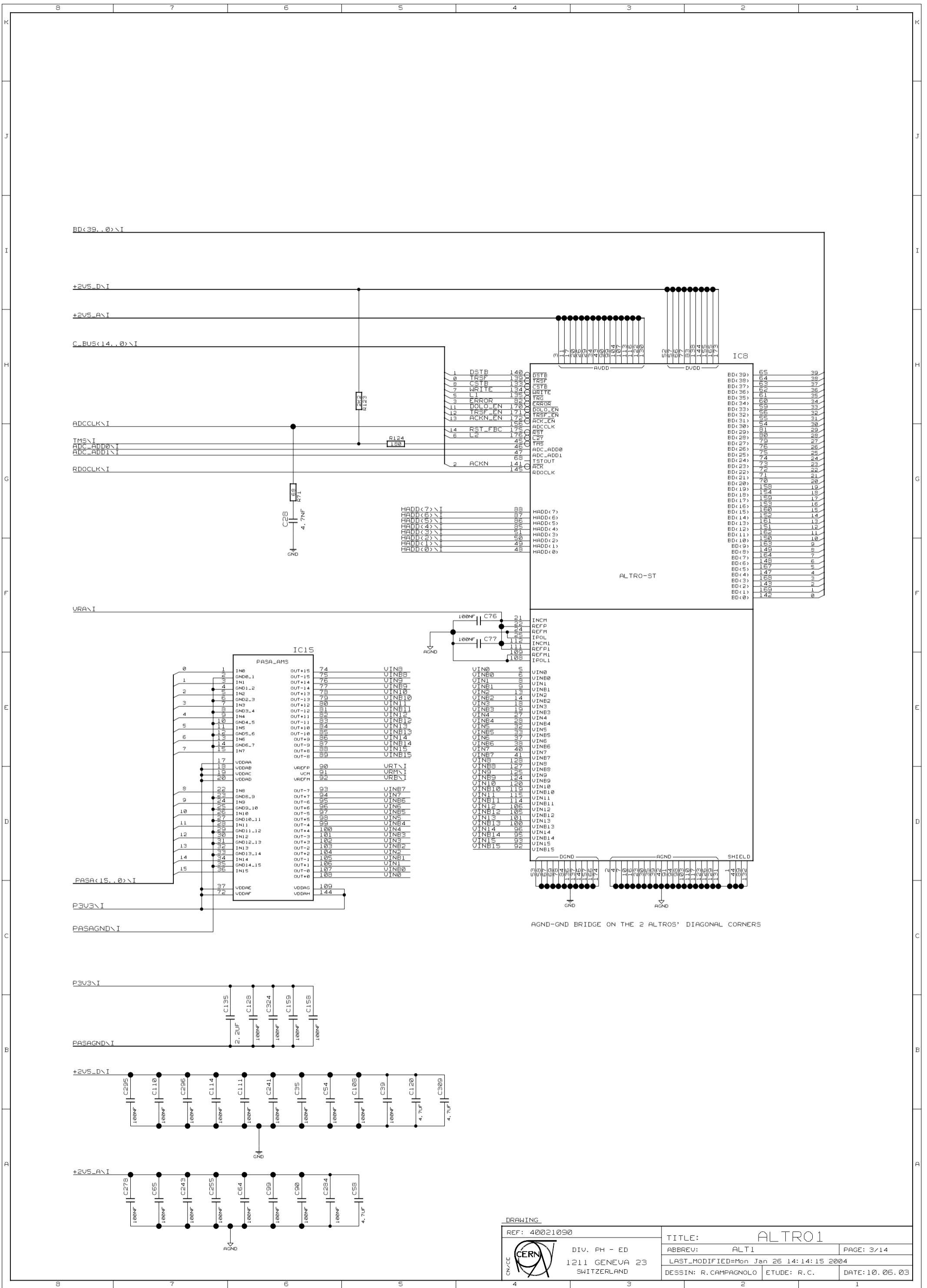
MPS_ENABLE\I

INTERRUPT\I

(OPEN COLLECTOR OUTPUT 'OR-WIRED' TO THE BUS WITH COMMON PULL-UP TERMINATION RESISTOR)

PULL-DOWN REQUIRED TO COMPENSATE DRIFTING CURRENTS WHEN FPGA IS NOT PROGRAMMED

EDMS REF: X		VERSION: X		PCB: X		SYSTEM: X	
REF: 40021090				TITLE: POWER_CTRL			
		DIV. PH - ED		ABBREV: PCTRL		PAGE: 2/14	
		1211 GENEVA 23 SWITZERLAND		LAST_MODIFIED=Mon Jan 26 14:10:30 2004			
		DESSIN: R. CAMPAGNOLO		ETUDE: R. C.		DATE: 10.05.03	



BD<39..0>\I

+2V5_D\I

+2V5_A\I

C_BUS<14..0>\I

ADCCLK\I

TMS\I

ADC_ADD0\I

ADC_ADD1\I

RDOCLK\I

URAV\I

PASA<15..0>\I

P3V3\I

PASAGND\I

P3V3\I

PASAGND\I

+2V5_D\I

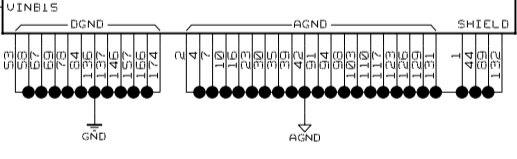
+2V5_A\I

1	DSTB	140	DSTB	55	39
0	TRSF	139	TRSF	54	38
8	CSTB	138	CSTB	53	37
7	WRITE	137	WRITE	52	36
6	LI	136	LI	51	35
5	ERROR	135	ERROR	50	34
11	DOLO_EN	170	DOLO_EN	49	33
12	TRSF_EN	171	TRSF_EN	48	32
13	ACKN_EN	172	ACKN_EN	47	31
14	RST_FBC	175	RST_FBC	46	30
E	LP	176	LP	45	29
4	ACKN	141	ACKN	44	28
148			ACKN	43	27
			ACKN	42	26
			ACKN	41	25
			ACKN	40	24
			ACKN	39	23
			ACKN	38	22
			ACKN	37	21
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			ACKN	33	17
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			ACKN	27	11
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			ACKN	25	9
			ACKN	24	8
			ACKN	23	7
			ACKN	22	6
			ACKN	21	5
			ACKN	20	4
			ACKN	19	3
			ACKN	18	2
			ACKN	17	1
			ACKN	16	0

HADD<7>\I	0	HADD<7>
HADD<6>\I	1	HADD<6>
HADD<5>\I	2	HADD<5>
HADD<4>\I	3	HADD<4>
HADD<3>\I	4	HADD<3>
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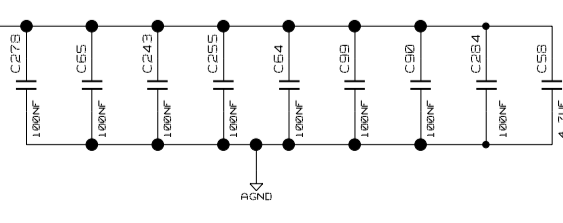
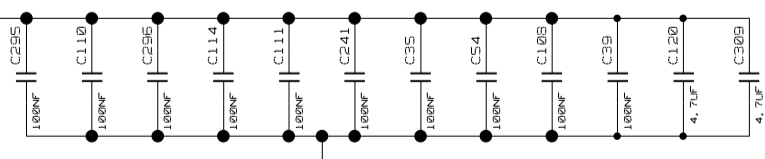
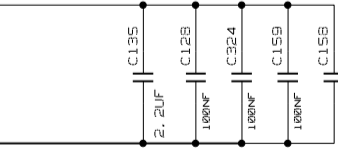


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REFP1	112	REFP1	112	VIN0
REFM1	113	REFM1	113	VIN0
IPOL1	114	IPOL1	114	VIN0
INC1	115	INC1	115	VIN0
REFP1	116	REFP1	116	VIN0
REFM1	117	REFM1	117	VIN0
IPOL1	118	IPOL1	118	VIN0
INC1	119	INC1	119	VIN0
REFP1	120	REFP1	120	VIN0
REFM1	121	REFM1	121	VIN0
IPOL1	122	IPOL1	122	VIN0
INC1	123	INC1	123	VIN0
REFP1	124	REFP1	124	VIN0
REFM1	125	REFM1	125	VIN0
IPOL1	126	IPOL1	126	VIN0
INC1	127	INC1	127	VIN0
REFP1	128	REFP1	128	VIN0
REFM1	129	REFM1	129	VIN0
IPOL1	130	IPOL1	130	VIN0
INC1	131	INC1	131	VIN0
REFP1	132	REFP1	132	VIN0
REFM1	133	REFM1	133	VIN0
IPOL1	134	IPOL1	134	VIN0
INC1	135	INC1	135	VIN0
REFP1	136	REFP1	136	VIN0
REFM1	137	REFM1	137	VIN0
IPOL1	138	IPOL1	138	VIN0
INC1	139	INC1	139	VIN0
REFP1	140	REFP1	140	VIN0
REFM1	141	REFM1	141	VIN0
IPOL1	142	IPOL1	142	VIN0



AGND-GND BRIDGE ON THE 2 ALTROS' DIAGONAL CORNERS

IN0	74	VIN0
OUT+15	75	VIN0
OUT+14	76	VIN0
OUT+13	77	VIN0
OUT+12	78	VIN0
OUT+11	79	VIN0
OUT+10	80	VIN0
OUT+9	81	VIN0
OUT+8	82	VIN0
OUT+7	83	VIN0
OUT+6	84	VIN0
OUT+5	85	VIN0
OUT+4	86	VIN0
OUT+3	87	VIN0
OUT+2	88	VIN0
OUT+1	89	VIN0
OUT+0	90	VIN0
OUT-15	91	VIN0
OUT-14	92	VIN0
OUT-13	93	VIN0
OUT-12	94	VIN0
OUT-11	95	VIN0
OUT-10	96	VIN0
OUT-9	97	VIN0
OUT-8	98	VIN0
OUT-7	99	VIN0
OUT-6	100	VIN0
OUT-5	101	VIN0
OUT-4	102	VIN0
OUT-3	103	VIN0
OUT-2	104	VIN0
OUT-1	105	VIN0
OUT+0	106	VIN0
OUT-0	107	VIN0
OUT+0	108	VIN0
OUT-0	109	VIN0
OUT+0	110	VIN0
OUT-0	111	VIN0
OUT+0	112	VIN0
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OUT-0	199	VIN0
OUT+0	200	VIN0



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CERN DIV. PH - ED 1211 GENEVA 23 SWITZERLAND

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ABBREU: ALT1

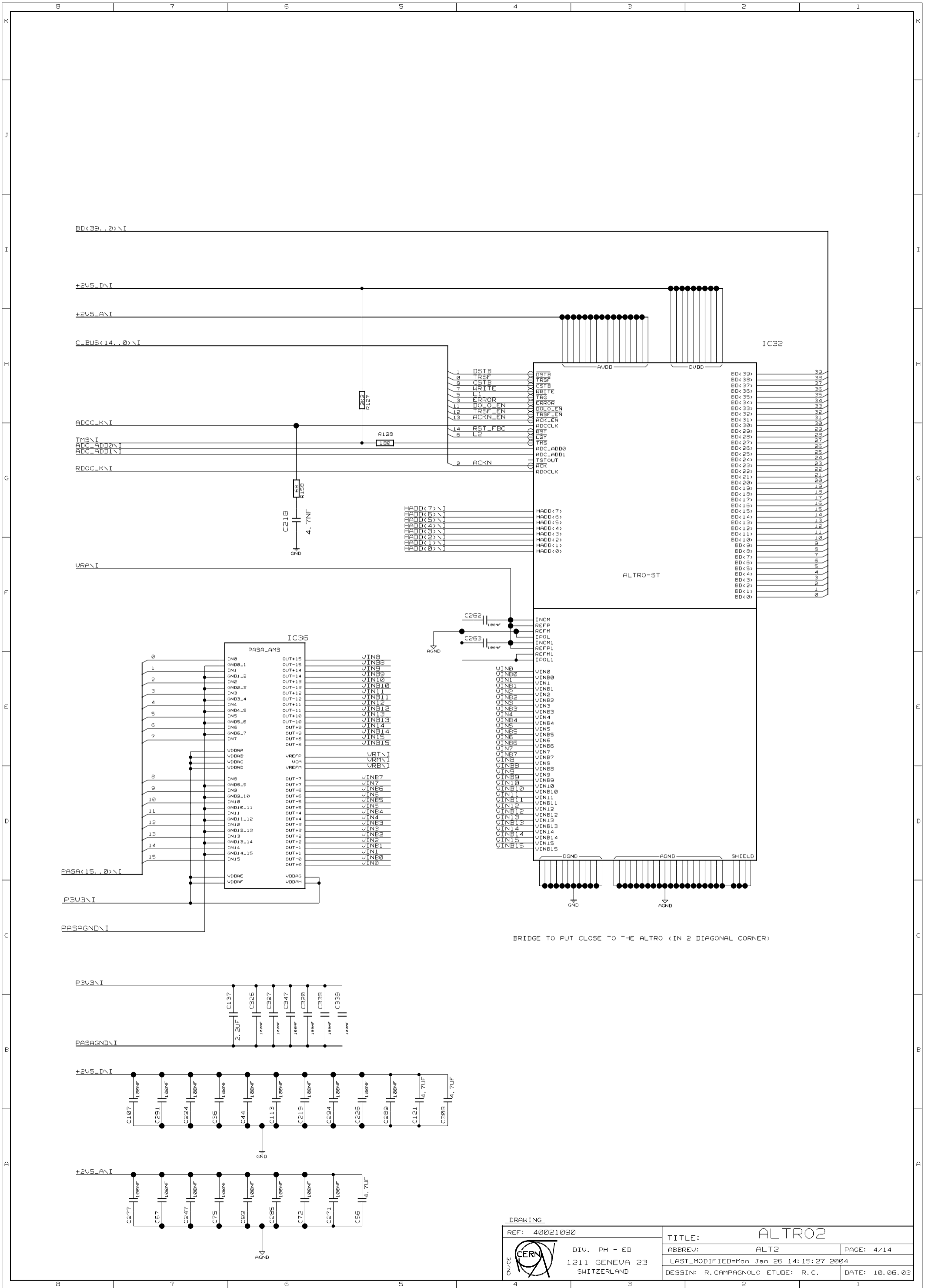
LAST_MODIFIED: Mon Jan 26 14:14:15 2004

DESSIN: R. CAMPANOLO

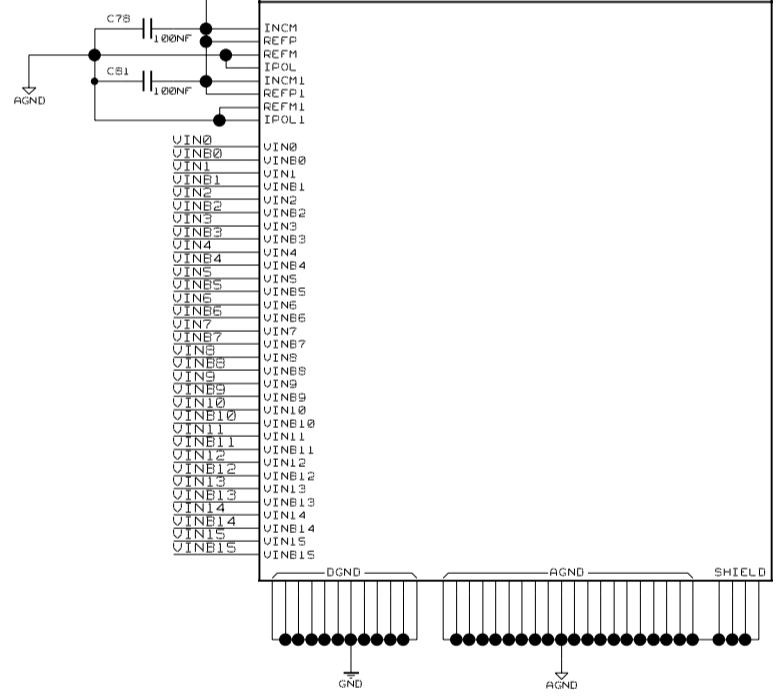
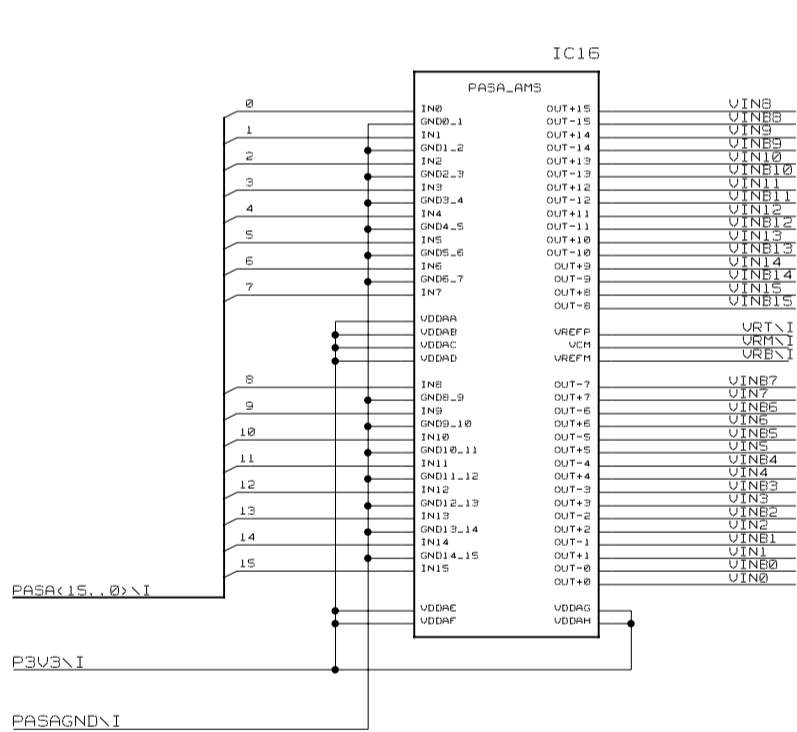
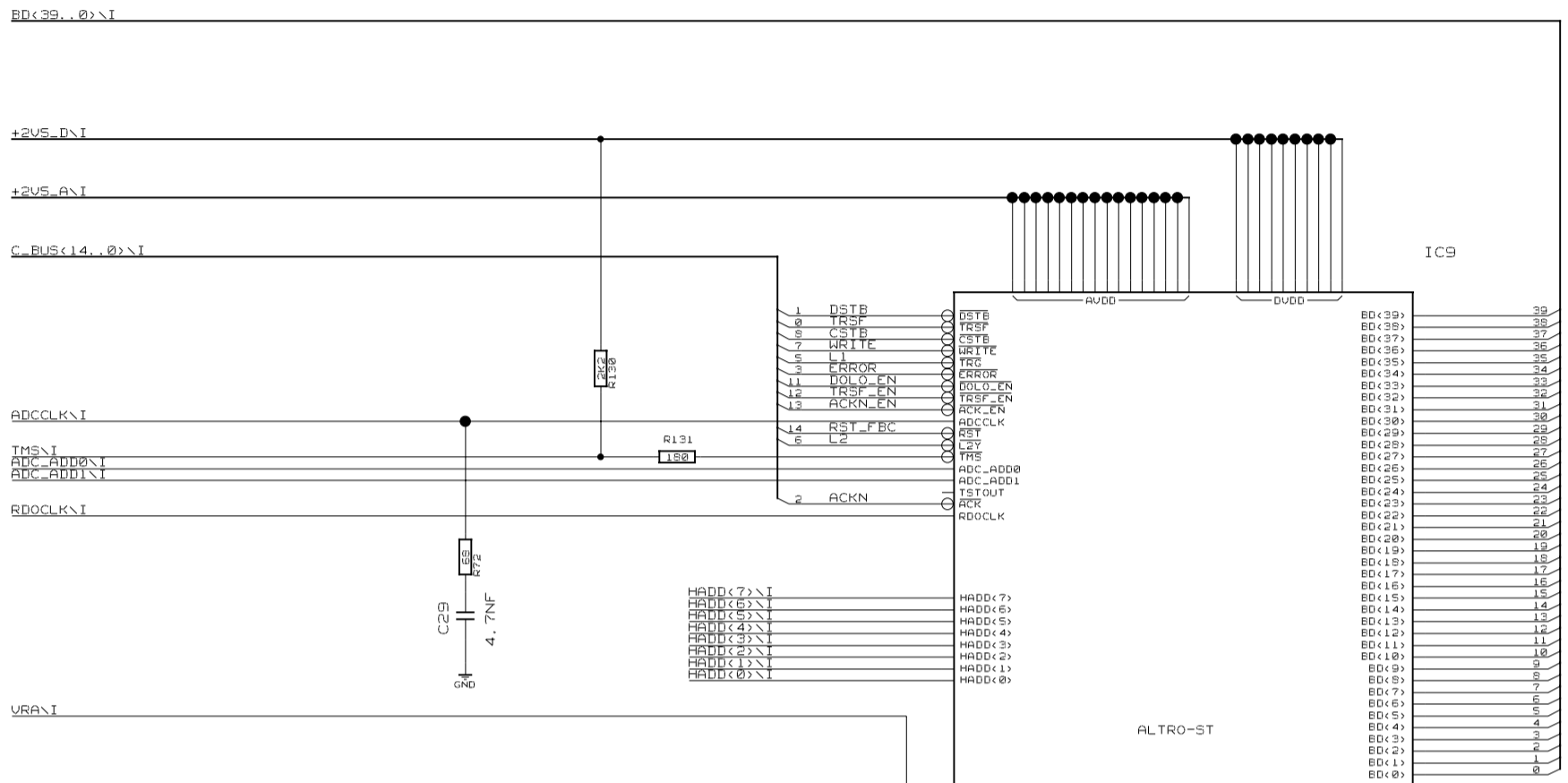
ETUDE: R. C.

PAGE: 3/14

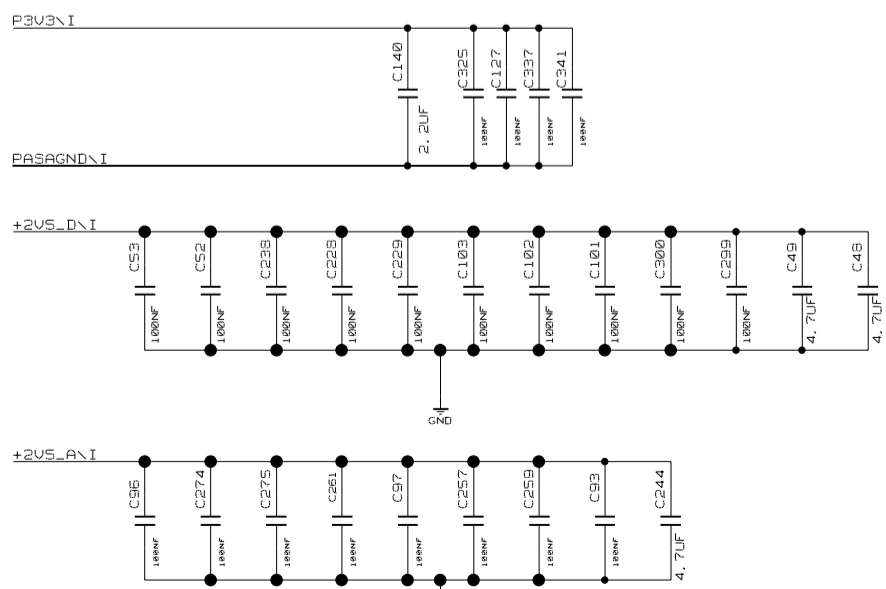
DATE: 10.06.03



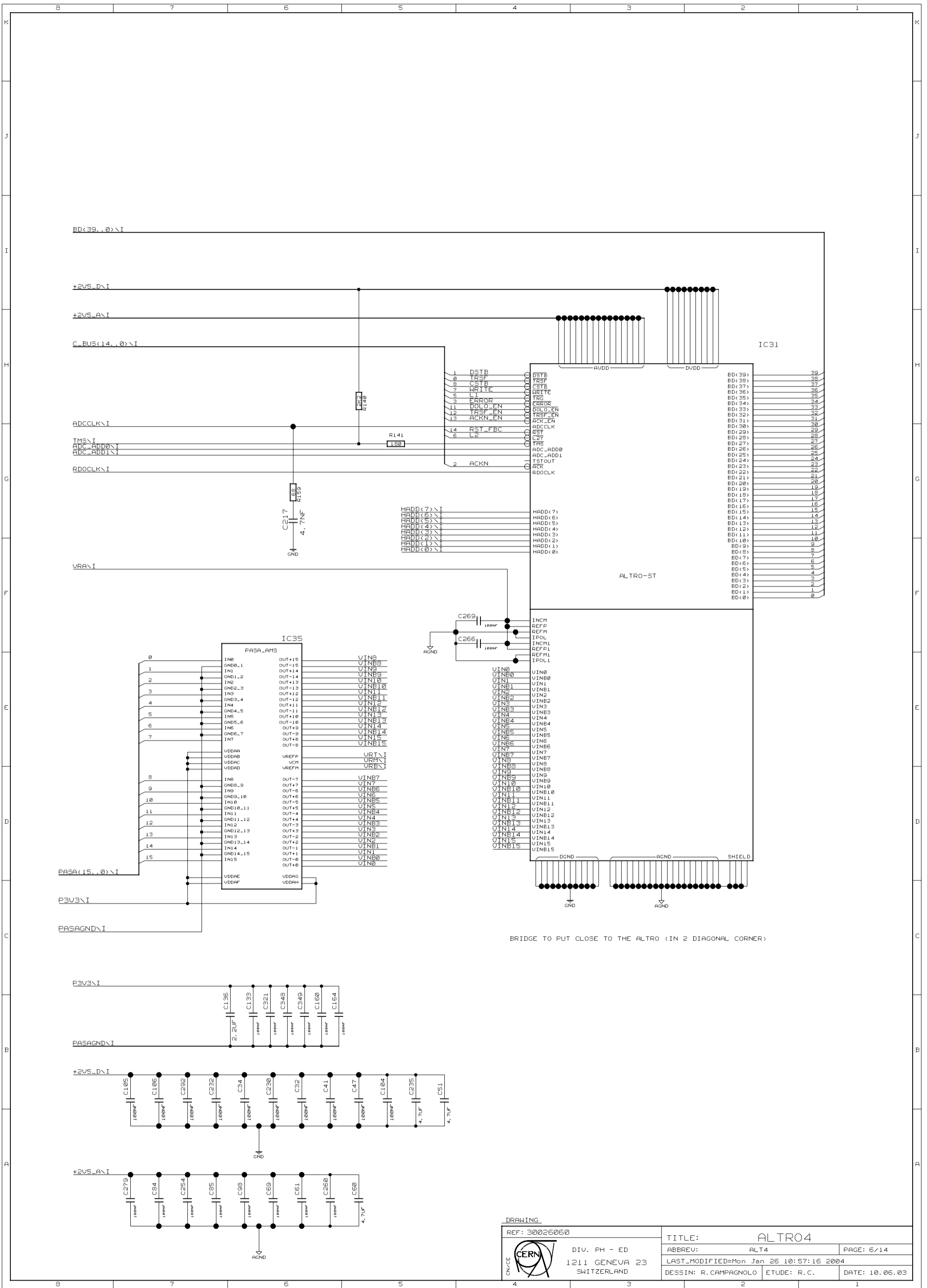
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1211 GENEVA 23		SWITZERLAND		PAGE: 4/14	
				LAST_MODIFIED=Mon Jan 26 14:15:27 2004	
				DESSIN: R. CAMPAGNOLO	
				ETUDE: R. C.	
				DATE: 10.05.03	



BRIDGE TO PUT CLOSE TO THE ALTRO (IN 2 DIAGONAL CORNER)

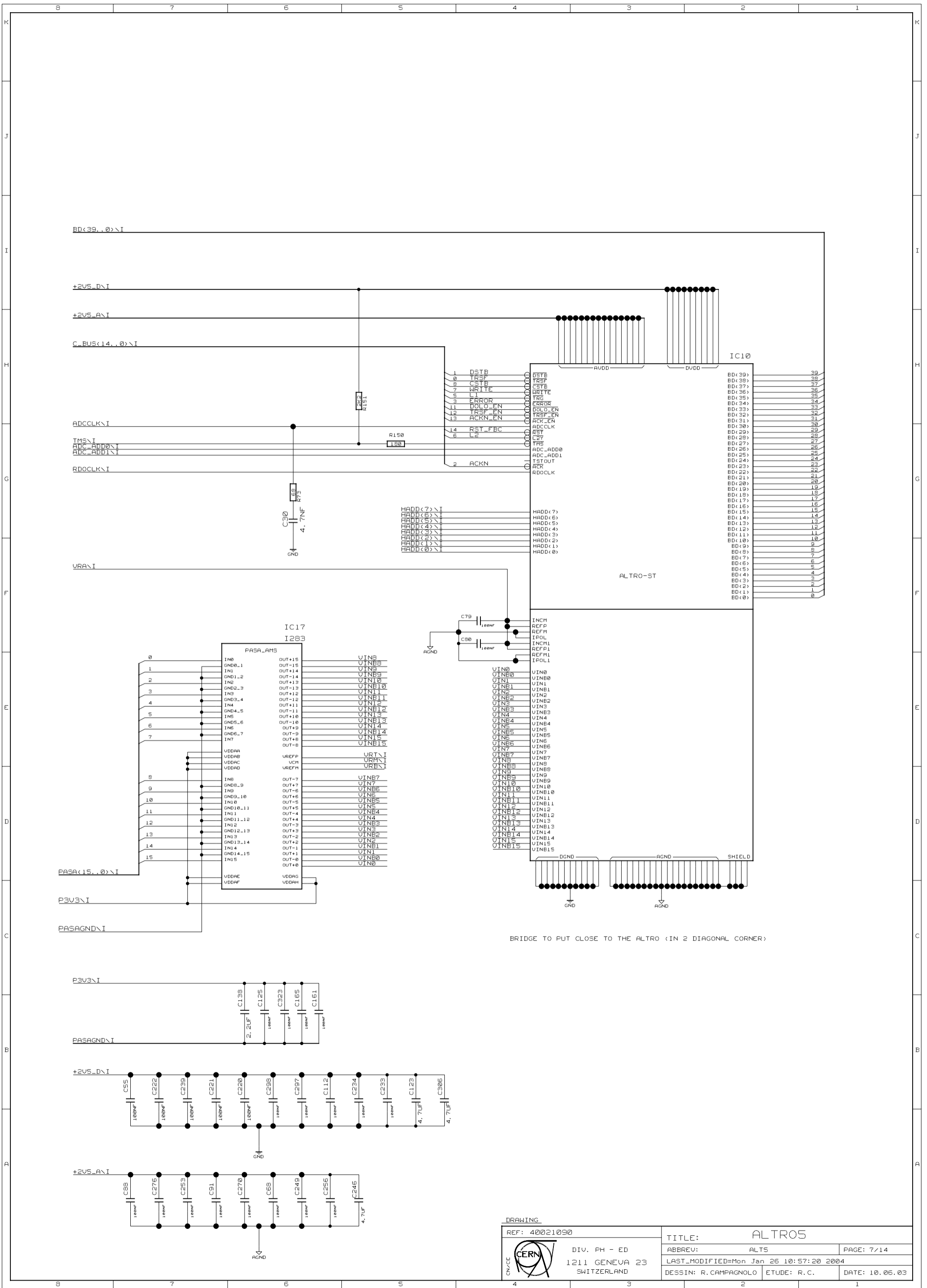


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		ETUDE: R.C.	DATE: 10.06.03

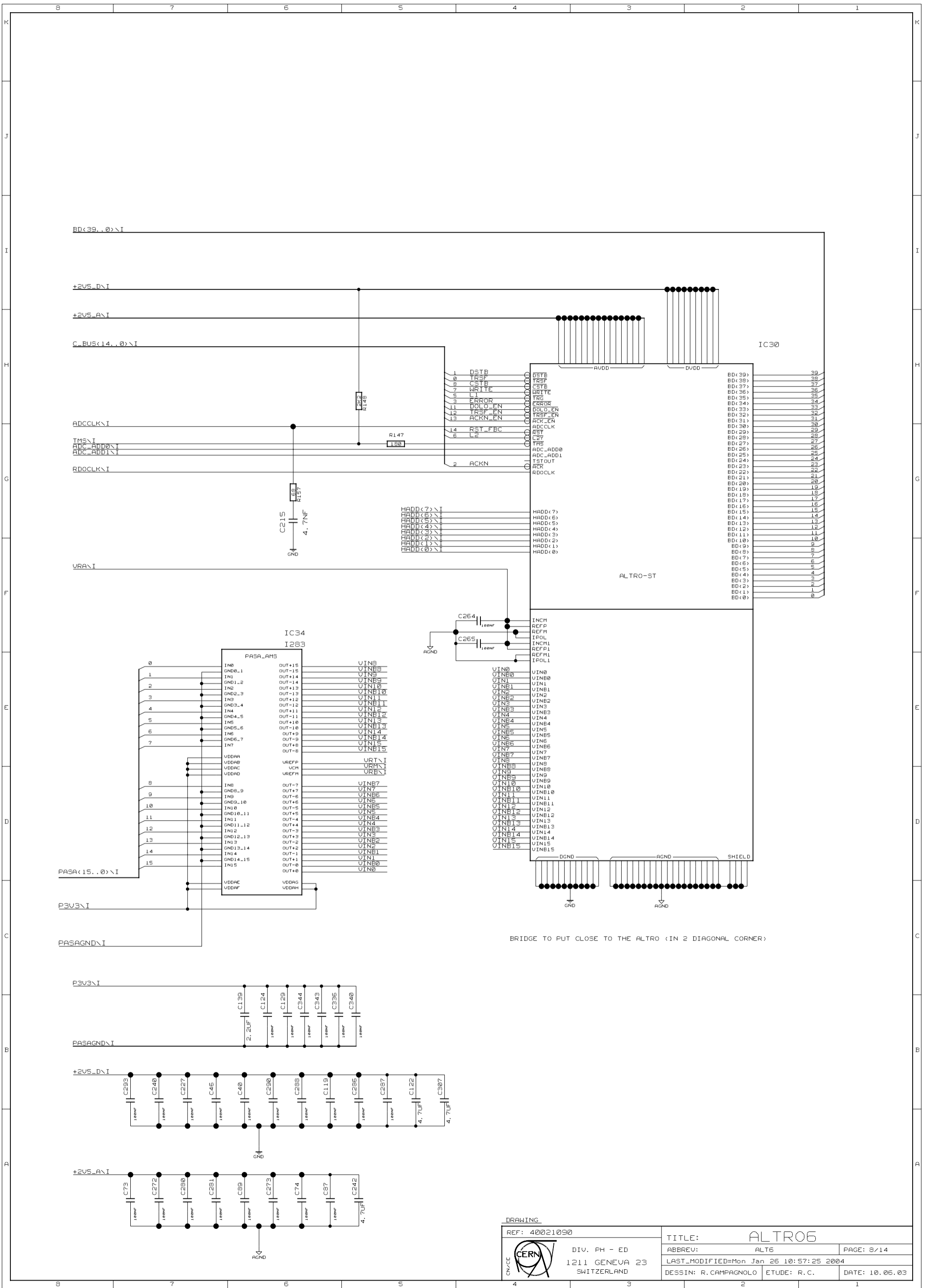


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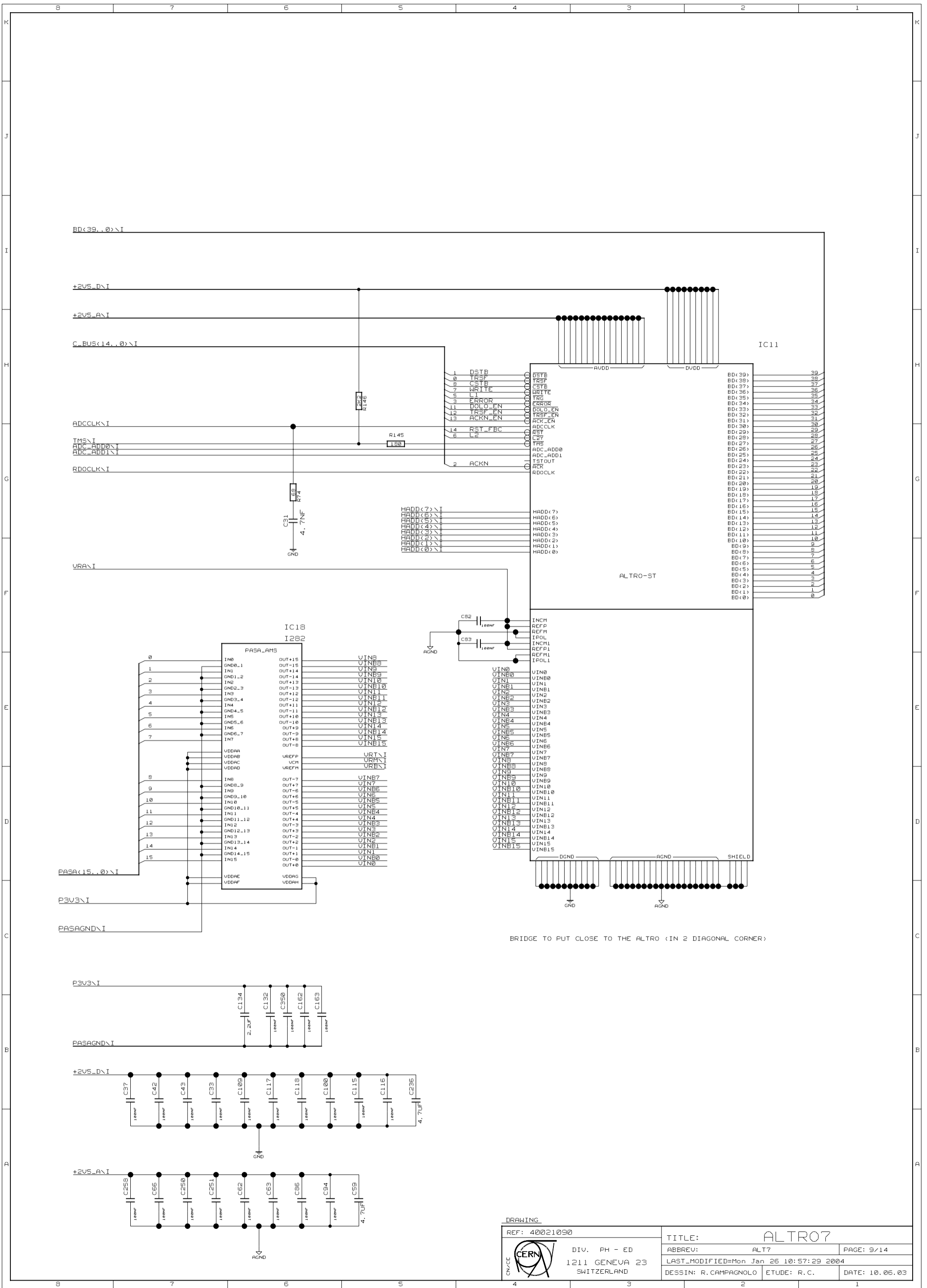
BRIDGE TO PUT CLOSE TO THE ALTRO (IN 2 DIAGONAL CORNER)



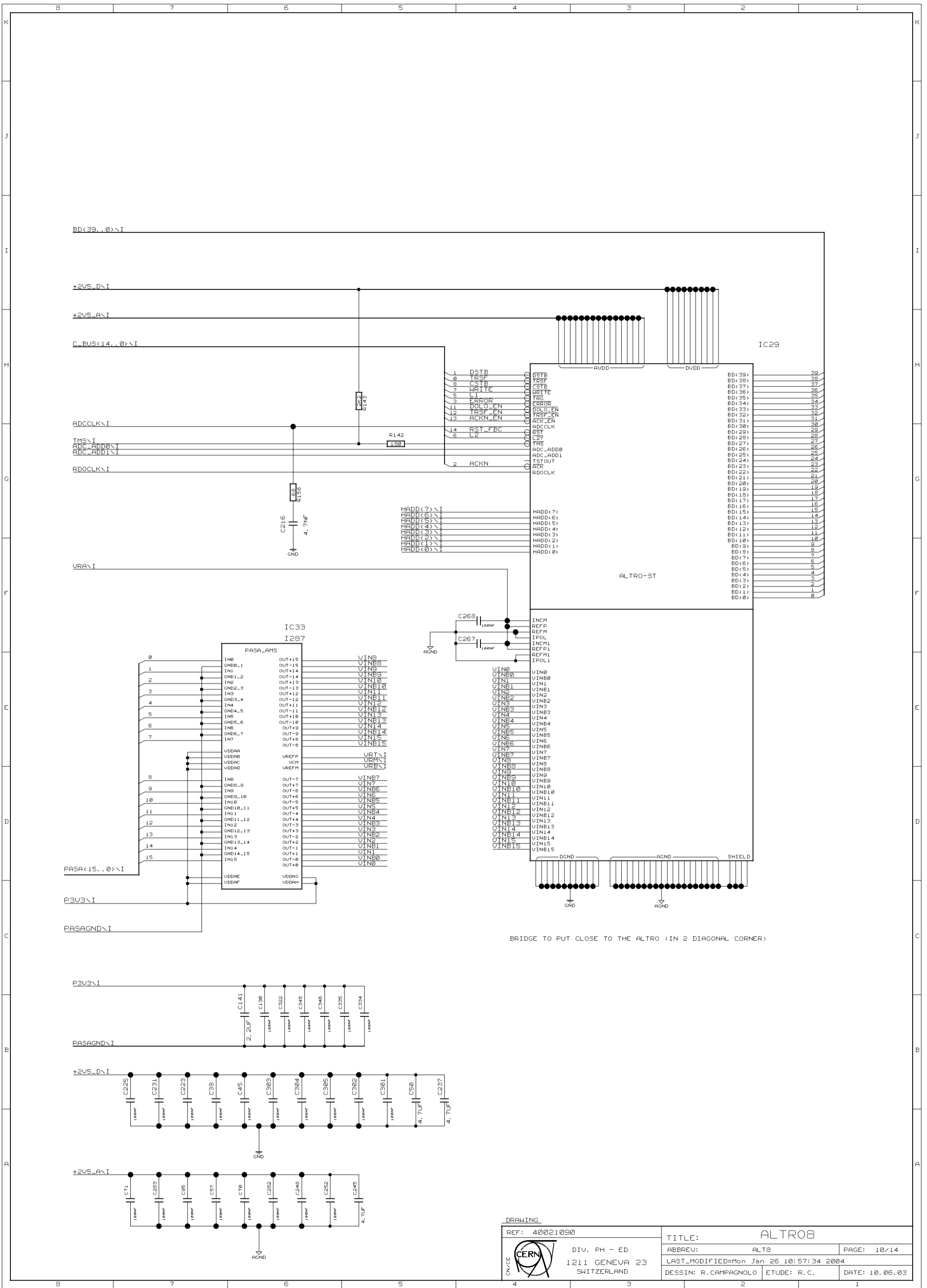
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		1211 GENEVA 23 SWITZERLAND	
DESSIN: R. CAMPAGNOLO		ETUDE: R. C.	DATE: 10.06.03



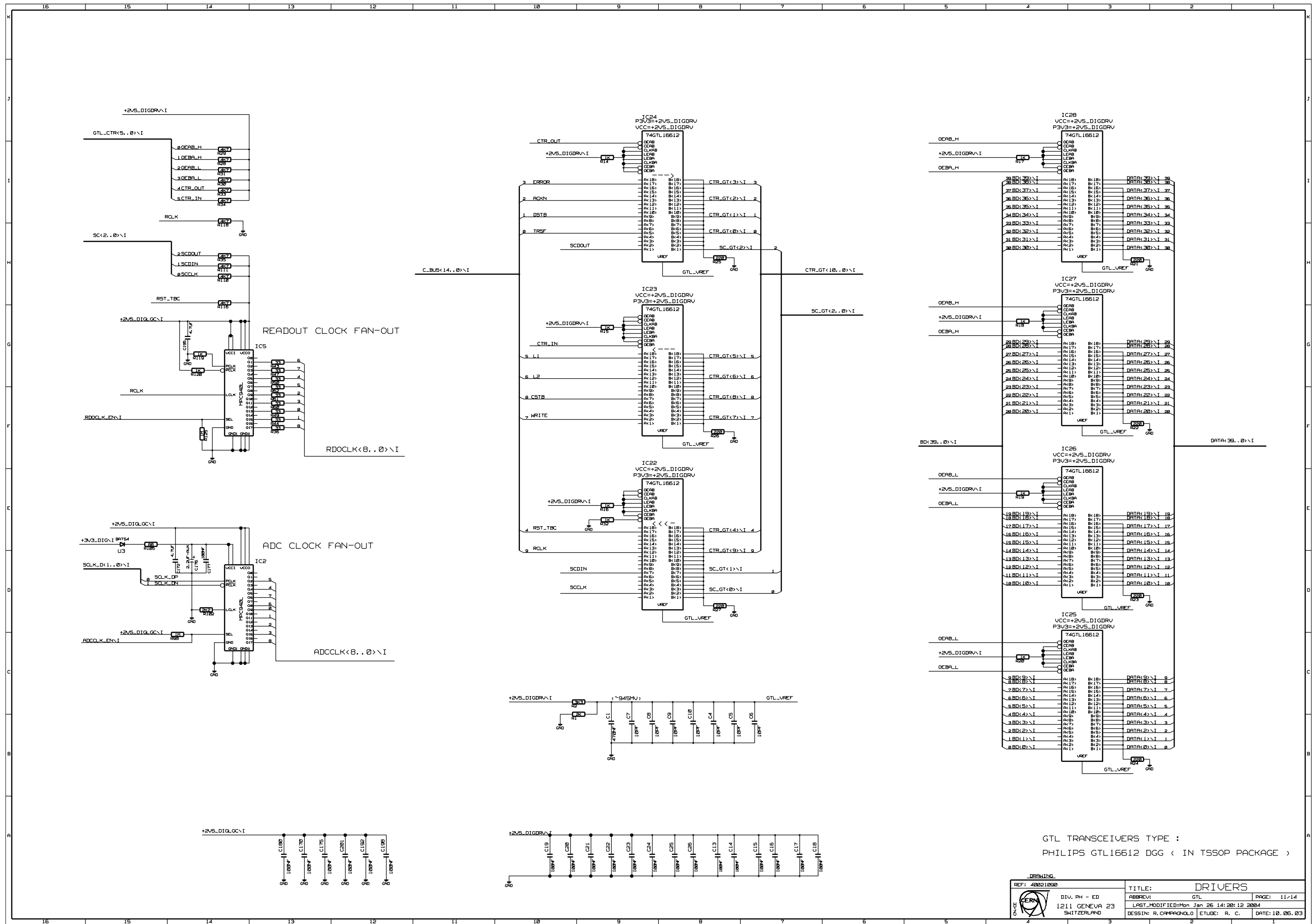
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	SWITZERLAND	DESSIN: R.CAMPAGNOLO	ETUDE: R.C.
			DATE: 10.06.03



DRAWING		REF: 40021090		TITLE: ALTRO7	
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DESSIN: R.CAMPAGNOLO		ETUDE: R.C.		DATE: 10.06.03	

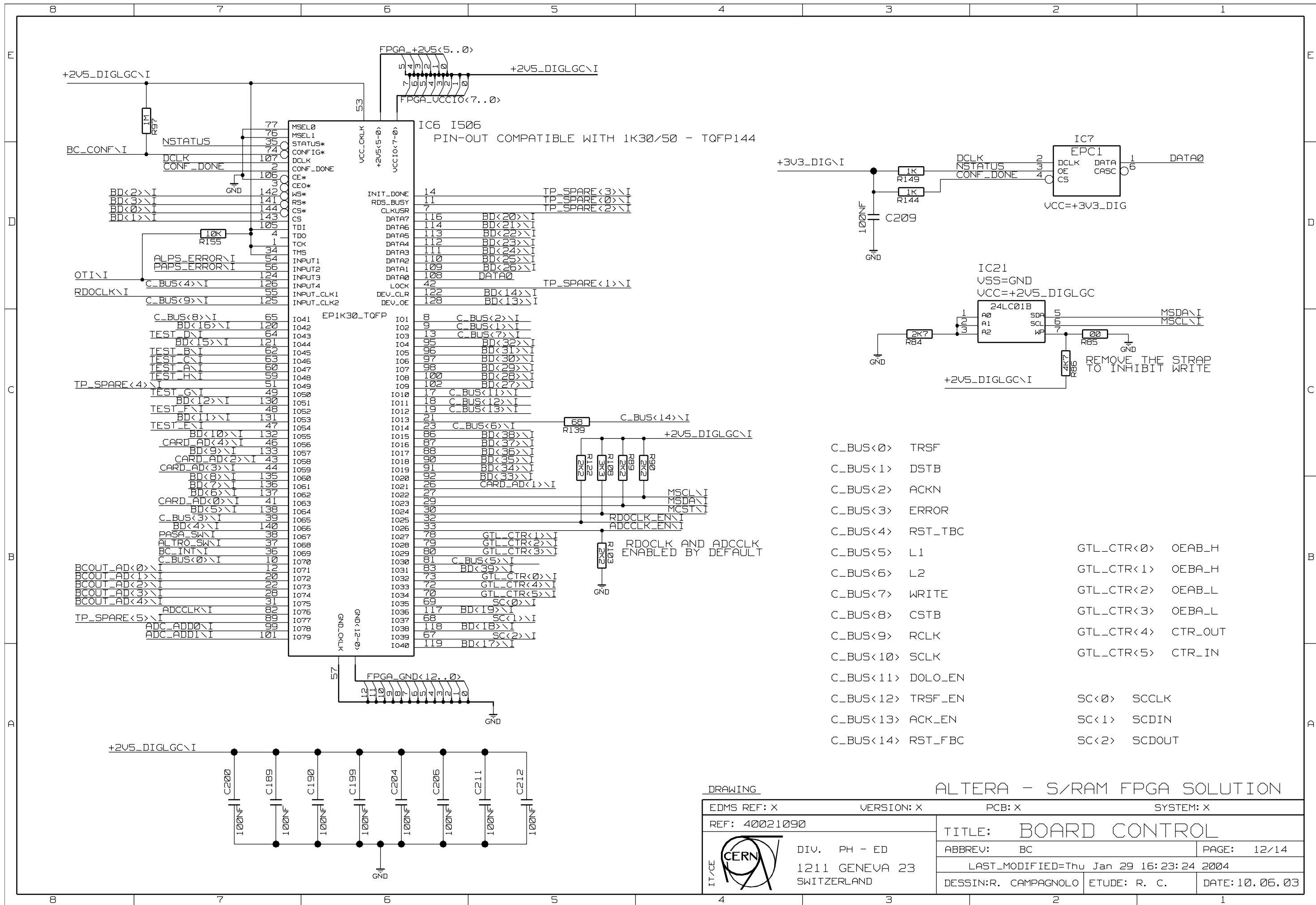


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	SWITZERLAND		DESSIN: R.CAMPAGNOLO		ETUDE: R.C.
				DATE: 10.06.03	



GTL TRANSCEIVERS TYPE :
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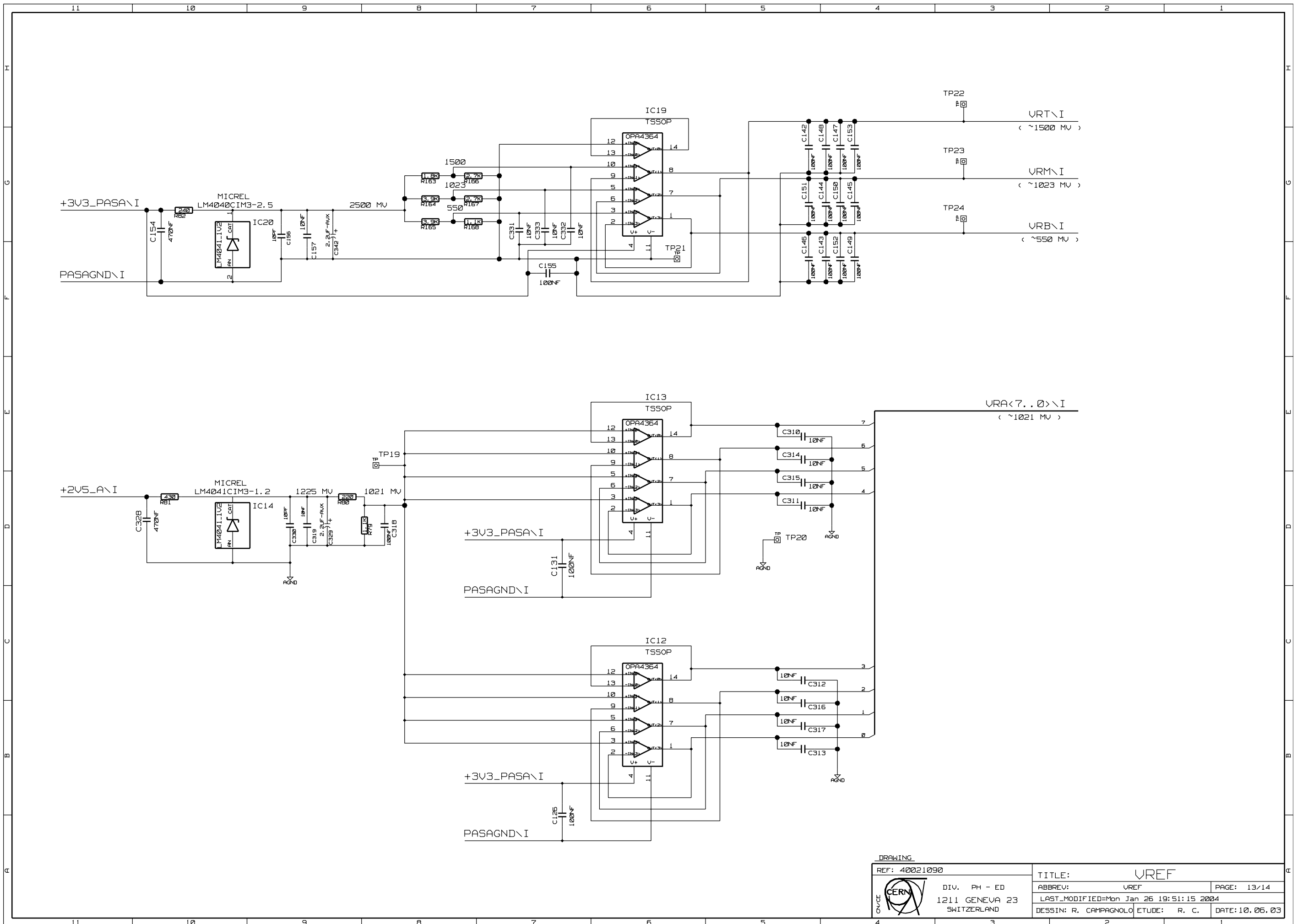
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SWITZERLAND		DESSIN: R. CAMPANOLO ETUDE: R. C. DATE: 10.05.03	




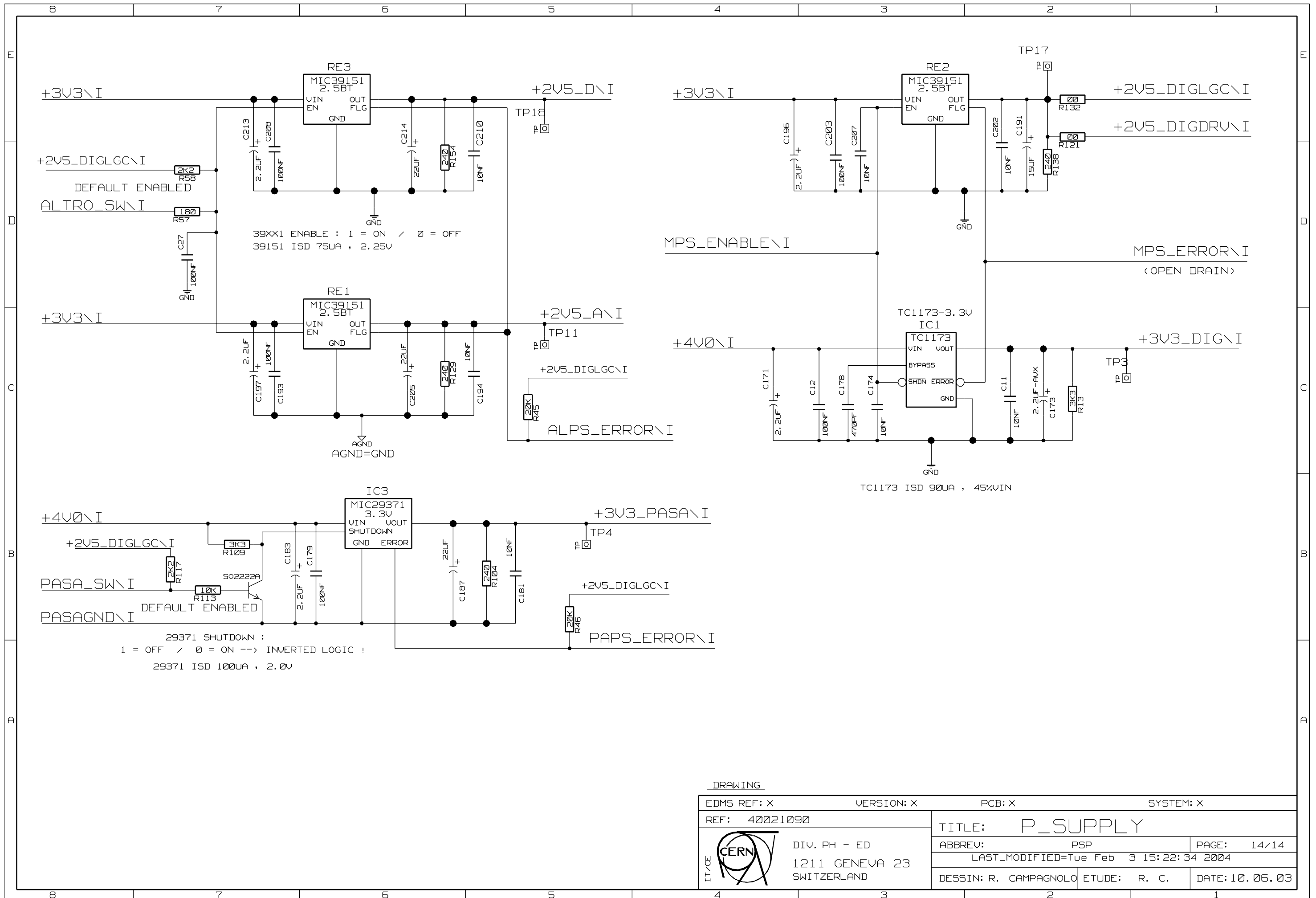
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- C_BUS<3> ERROR
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- C_BUS<6> L2
- C_BUS<7> WRITE
- C_BUS<8> CSTB
- C_BUS<9> RCLK
- C_BUS<10> SCLK
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- C_BUS<12> TRSF_EN
- C_BUS<13> ACK_EN
- C_BUS<14> RST_FBC
- GTL_CTR<0> OEAB_H
- GTL_CTR<1> OEBA_H
- GTL_CTR<2> OEAB_L
- GTL_CTR<3> OEBA_L
- GTL_CTR<4> CTR_OUT
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DRAWING ALTERA - S/DRAM FPGA SOLUTION


EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF: 40021090		TITLE: BOARD CONTROL	
 DIV. PH - ED 1211 GENEVA 23 SWITZERLAND	ABBREV: BC	PAGE: 12/14	
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DRAWING		TITLE: VREF	
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DRAWING

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