Front End Card - status report

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presentation available at http://cern.ch/ep-ed-alice-tpc/

OUTLINE

- The New Front End Card

- Related Interfaces
  - new 40-bit Mezzanine ,
  - Termination/ Service card ,
  - Analog Test card

- Test and Measurements

- Conclusions

Why a New Front End Card ?

The Old FEC Integrates :

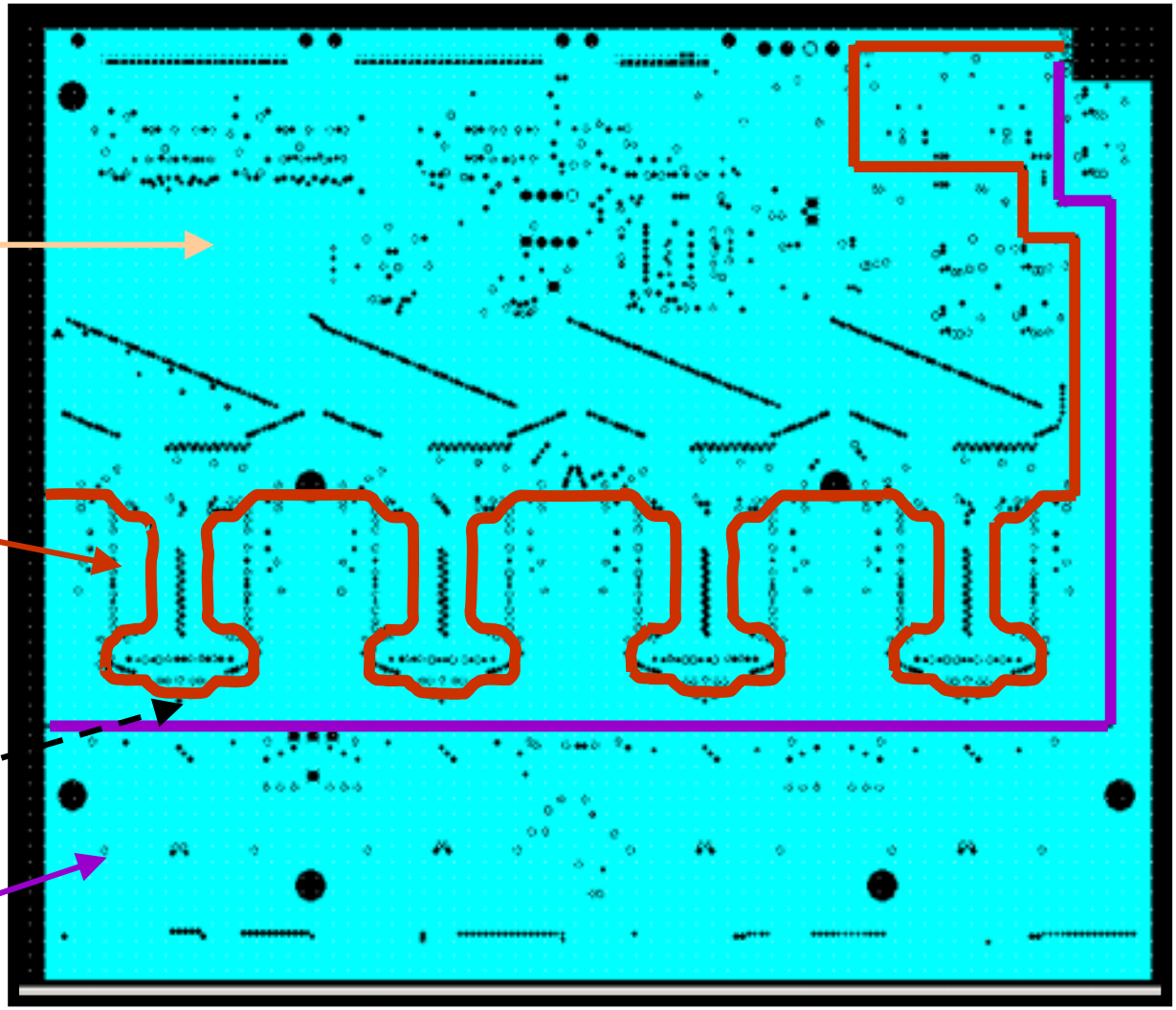
- 8 PASA from CERES
- 64 discrete dual-channel ADC
- 16 ALTRO chip (4 channels prototype)
- 32 bit Read Out BUS

The New FEC Integrates :

- 8 Newest PASA
- 8 ALTRO –16 channels each
- 40 bit Read Out BUS

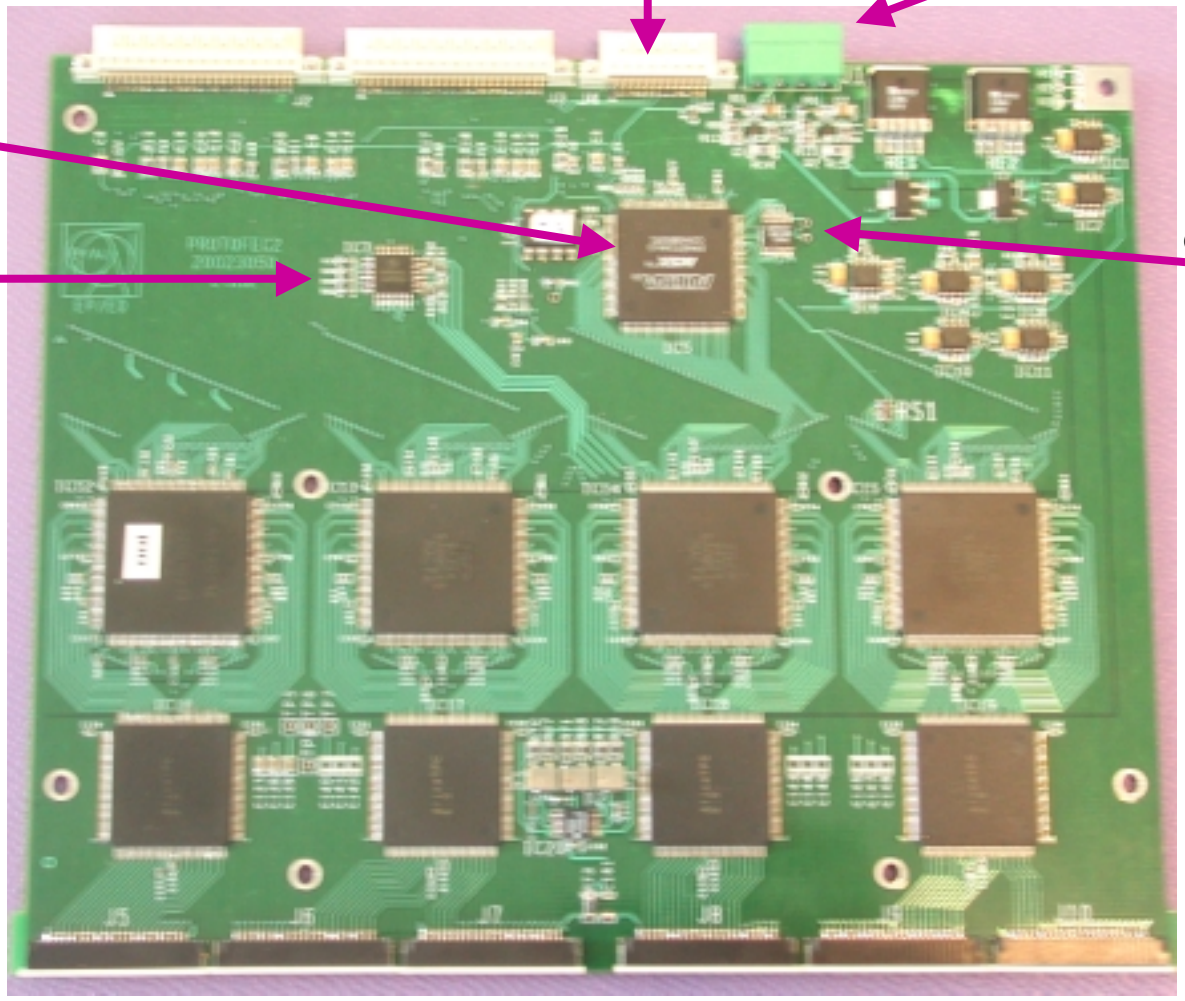
FEC - Circuit Board layout : The Ground plane

ALTRO bus - RCU side

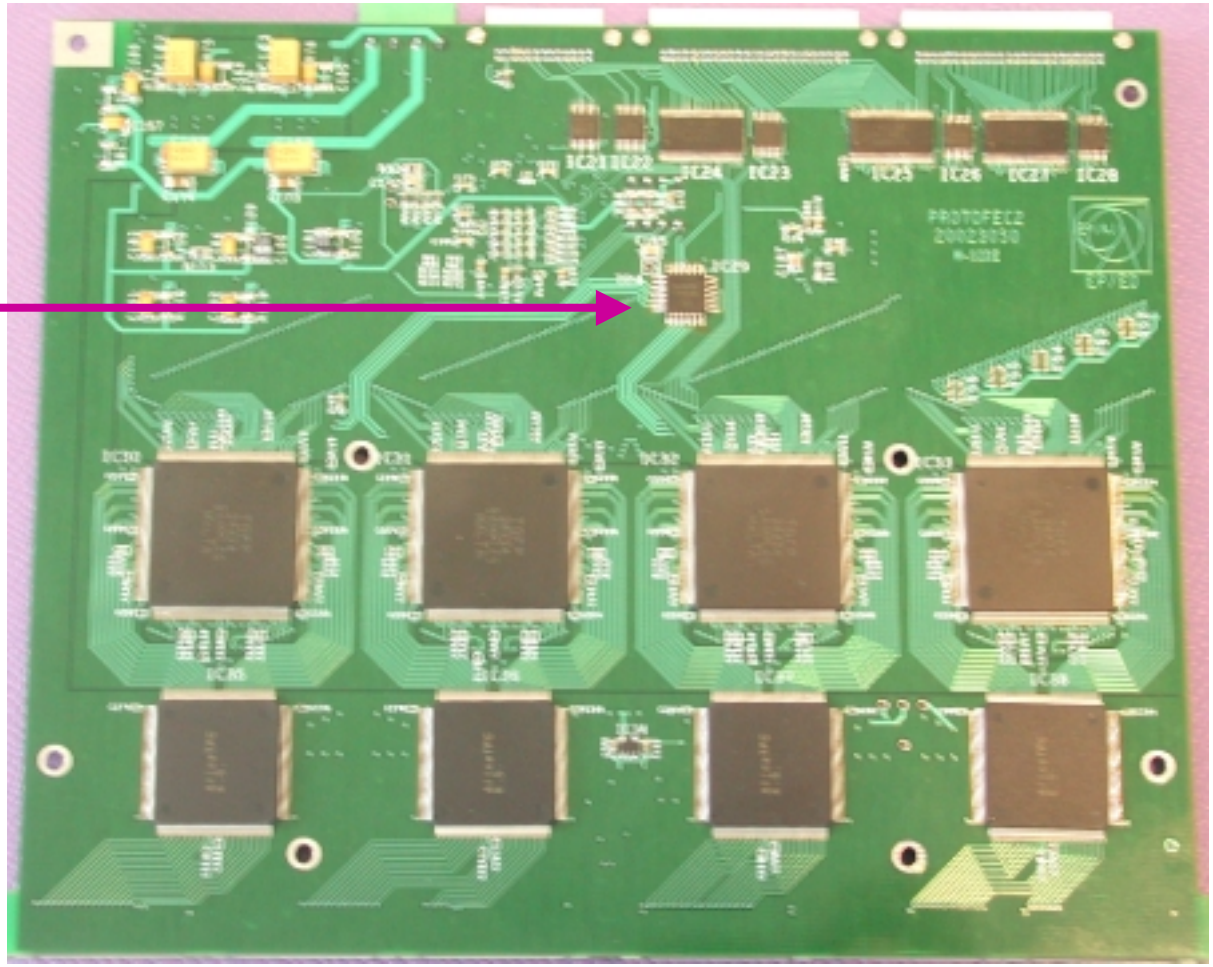


FRONT END CONNECTORS

The New Front End Card: TOP view



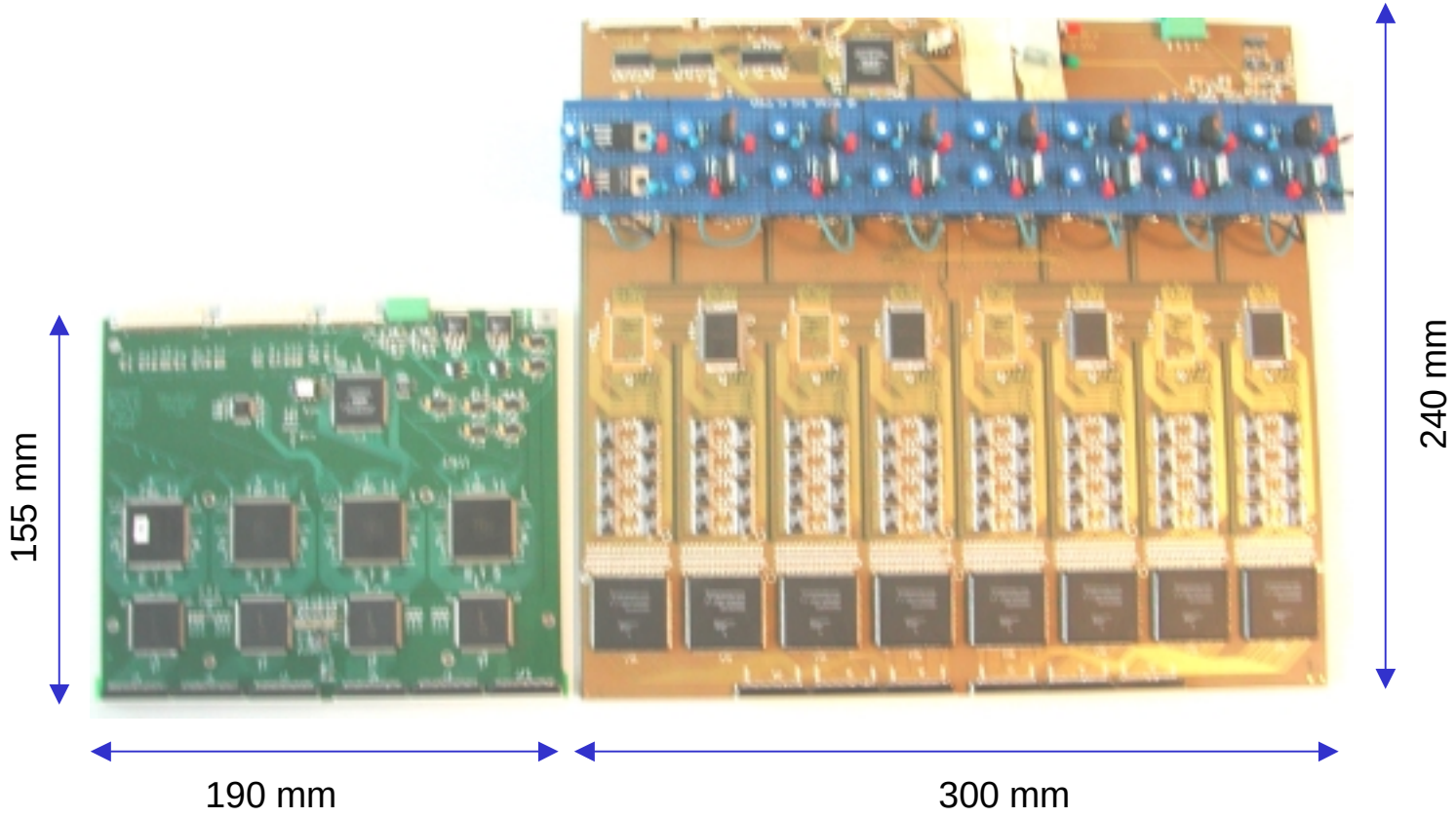
The New Front End Card:Bottom view



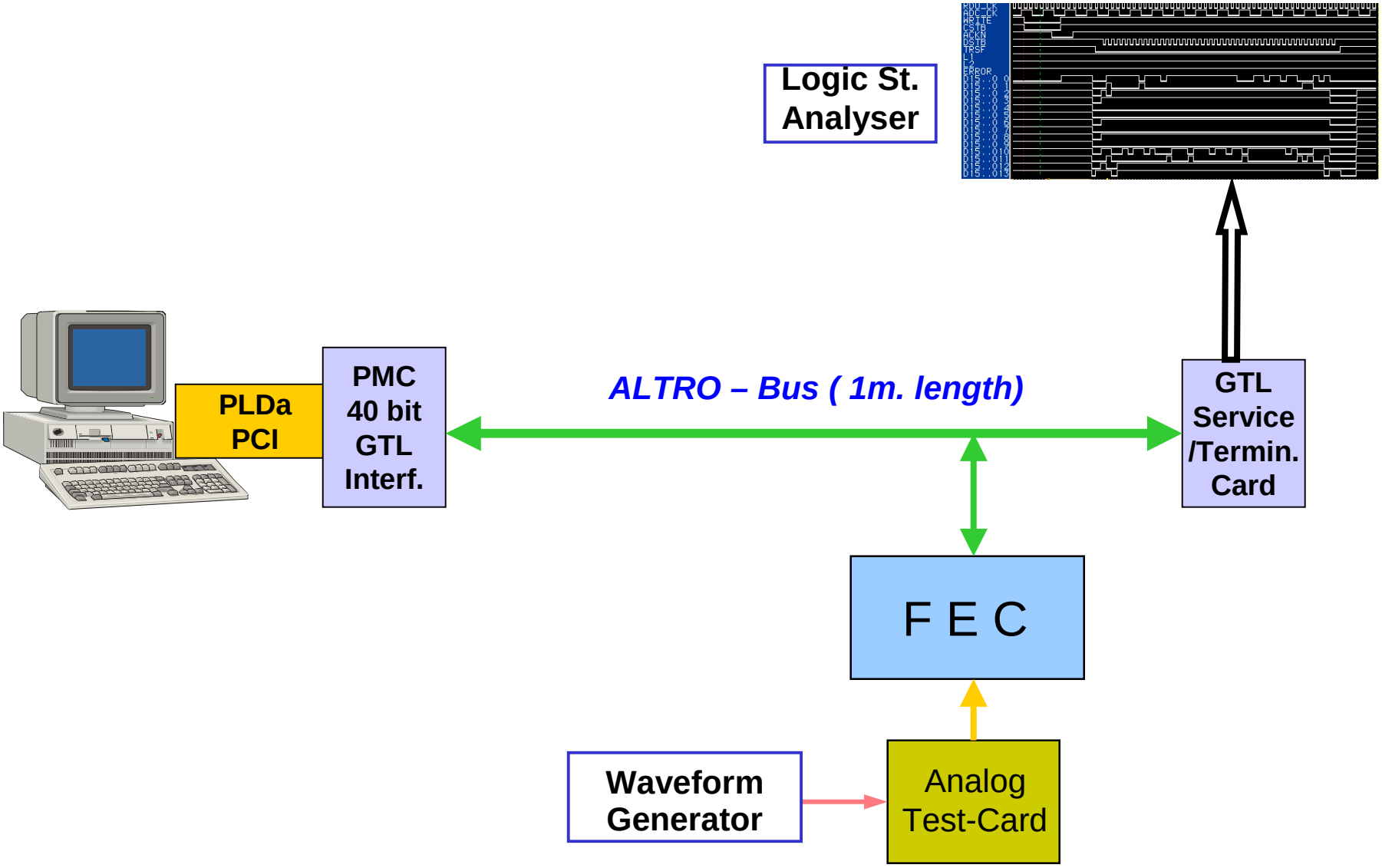
FECs – dimensional comparison

New Front End Card

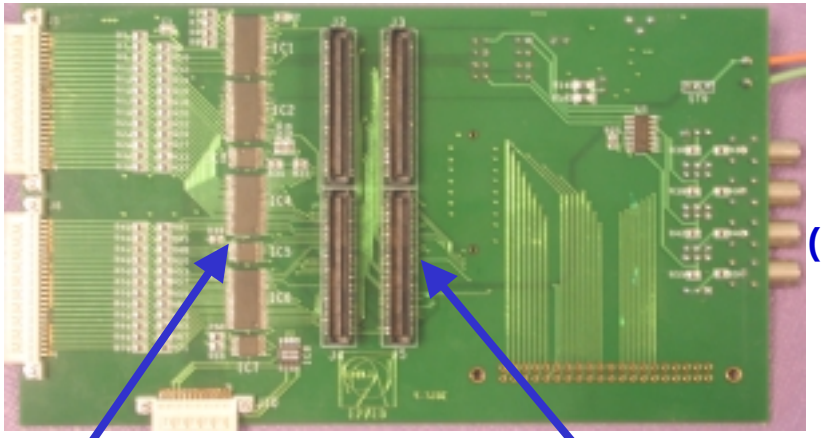
Previous functional prototype



Front End Card - Test Set Up



The new Mezzanine for PCI-based RCU



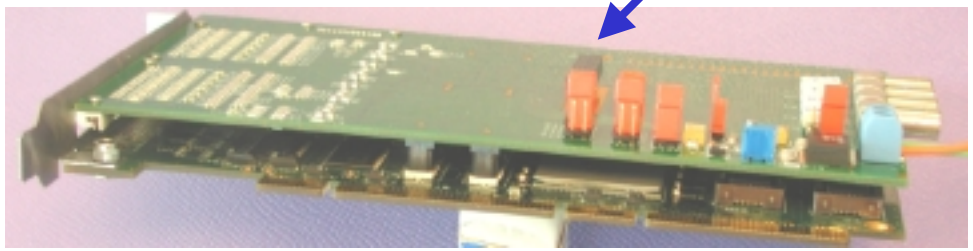
New 40-bit Mezzanine card

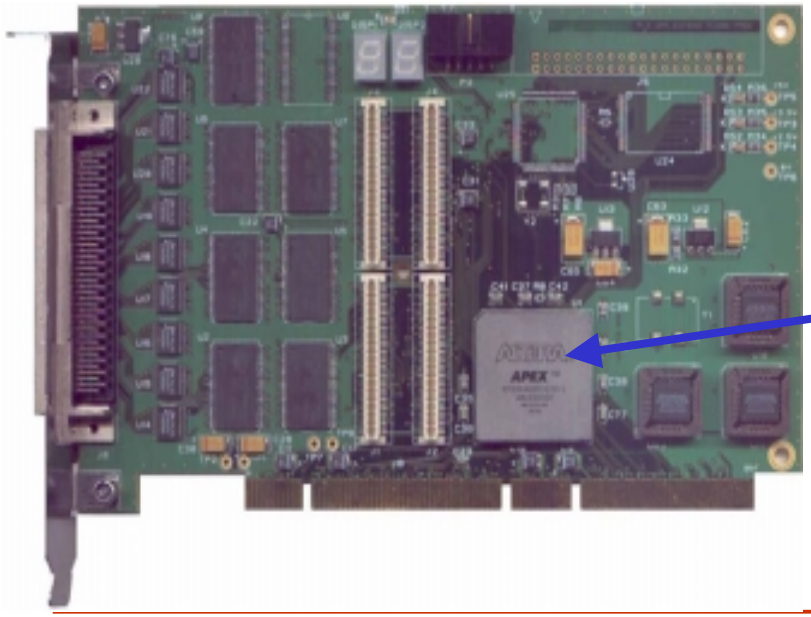
NIM CONNECTORs
(L1, L2, RDOCLK, ADCCLK)

DDL-SIU CONNECTOR

GTL Transceivers

PMC connectors





FPGA with PCI-core

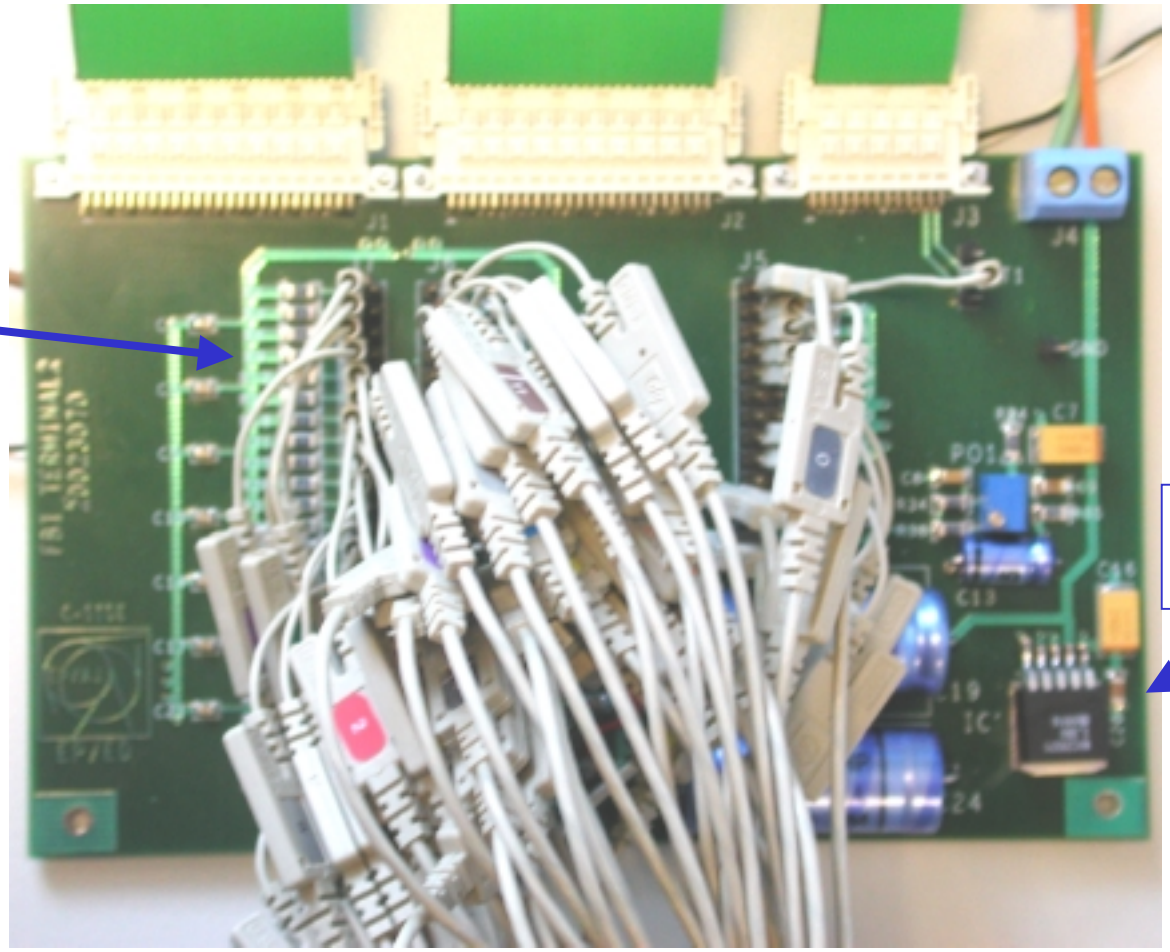
PCI CARD (PLDa)

The service card layout

ALTRO / GTL – bus

Power supply

Terminations Resistor

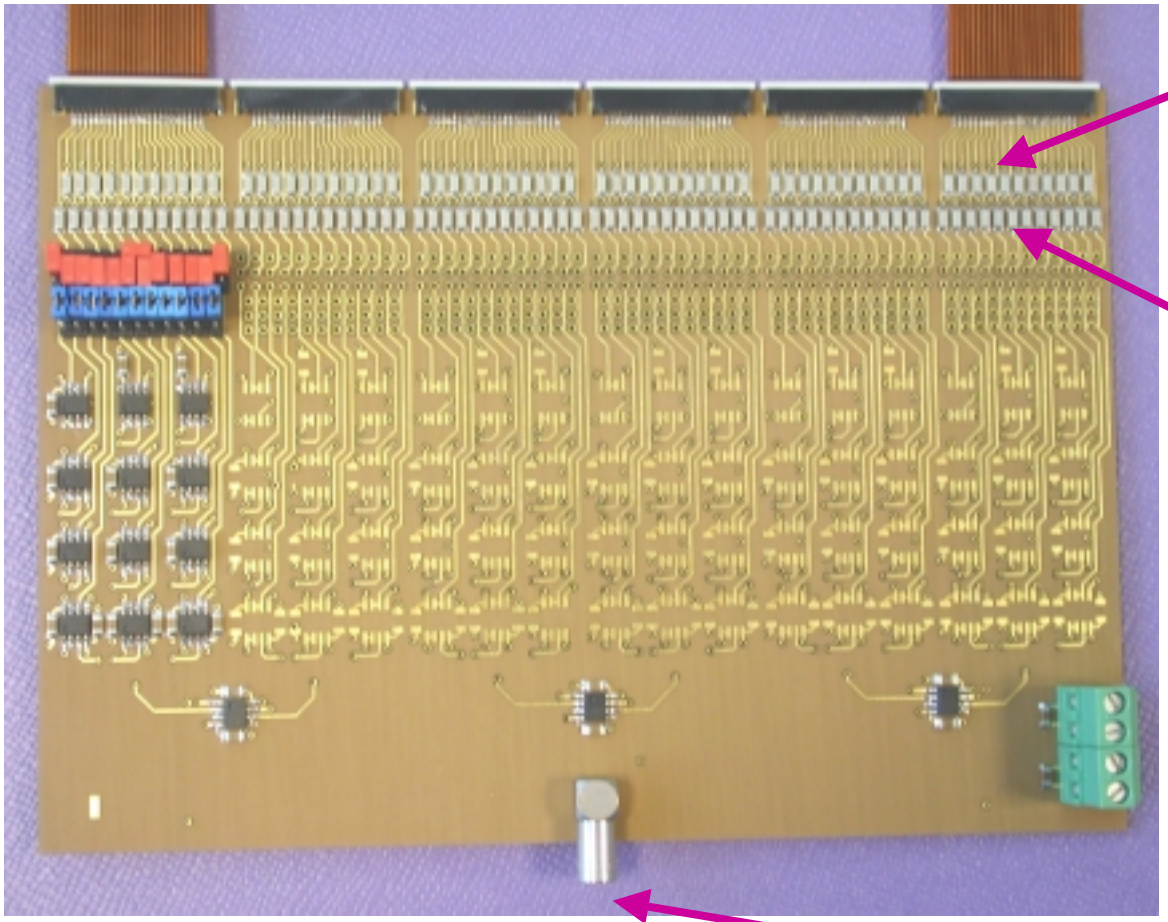


ALTRO-bus Power Supply

Logic State Analyzer probes

Analog Test Card layout

Kapton cables to the FEC



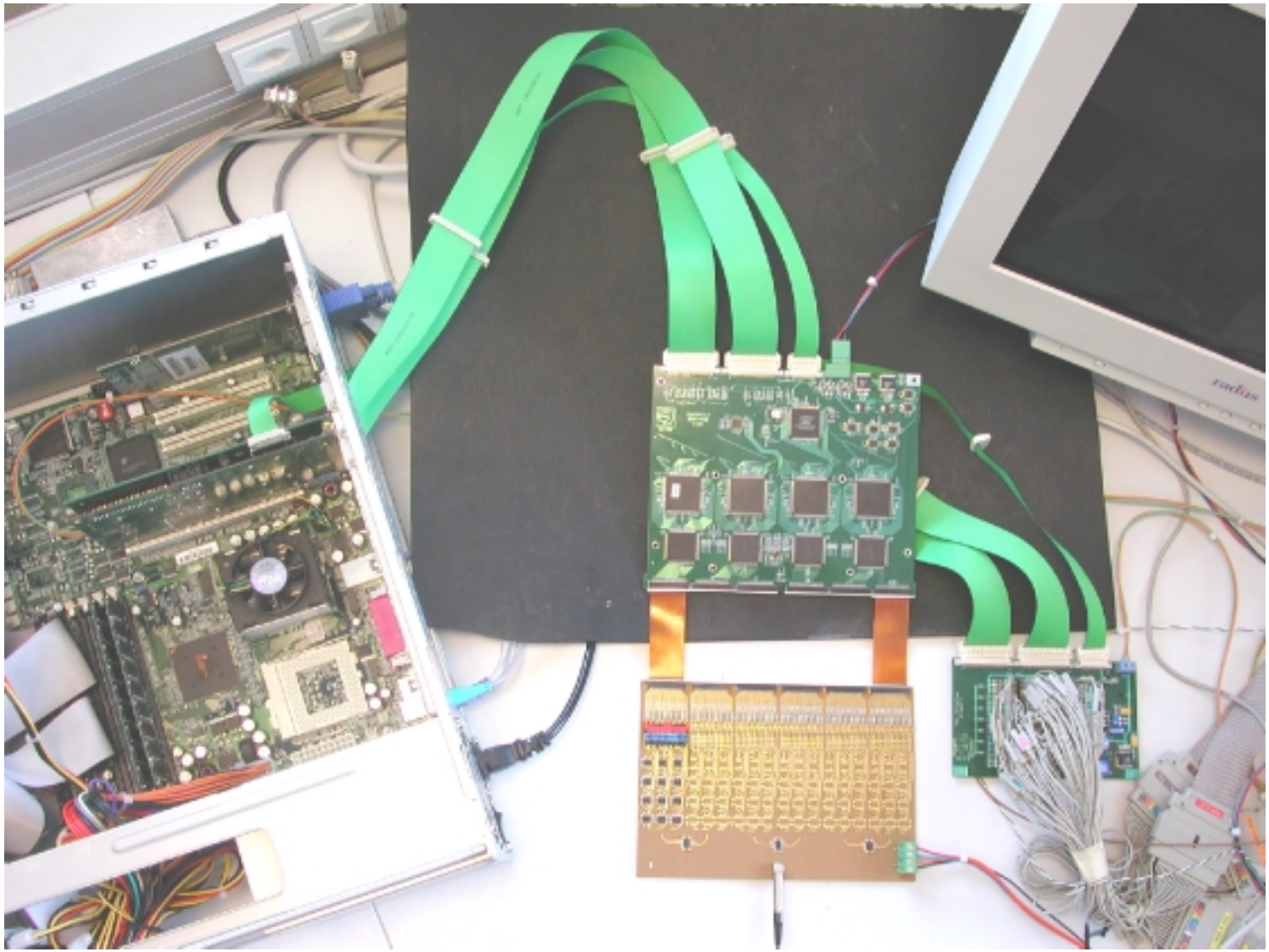
Capacitors for the injection of the charge into the PASA

Capacitors to simulate the detector Pad capacitance

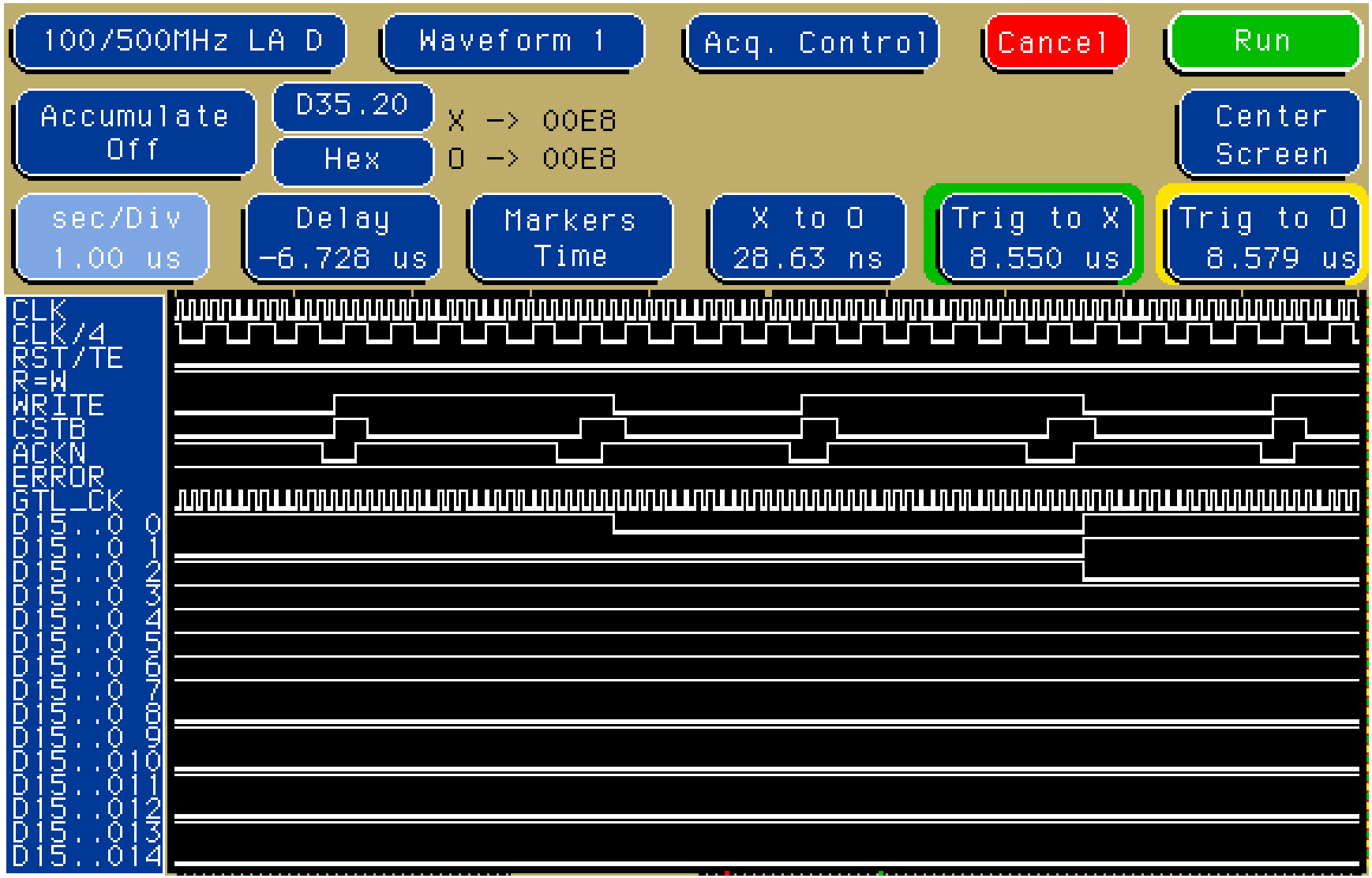
Power Supply

From the Waveform Generator

Complete system overview

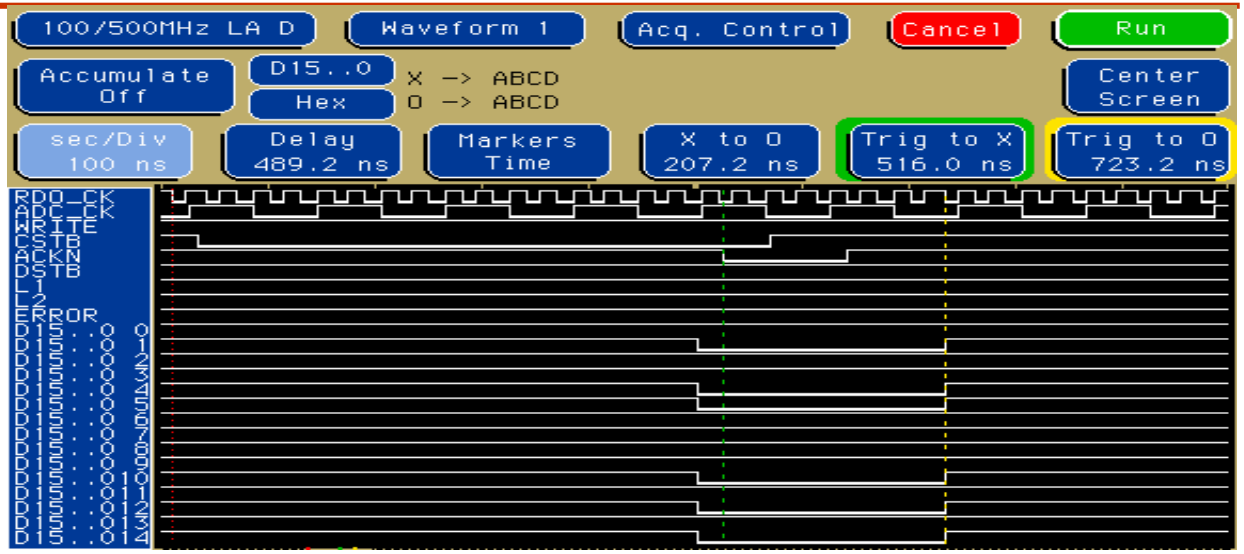


Self Test results : variable pattern on 128 channels

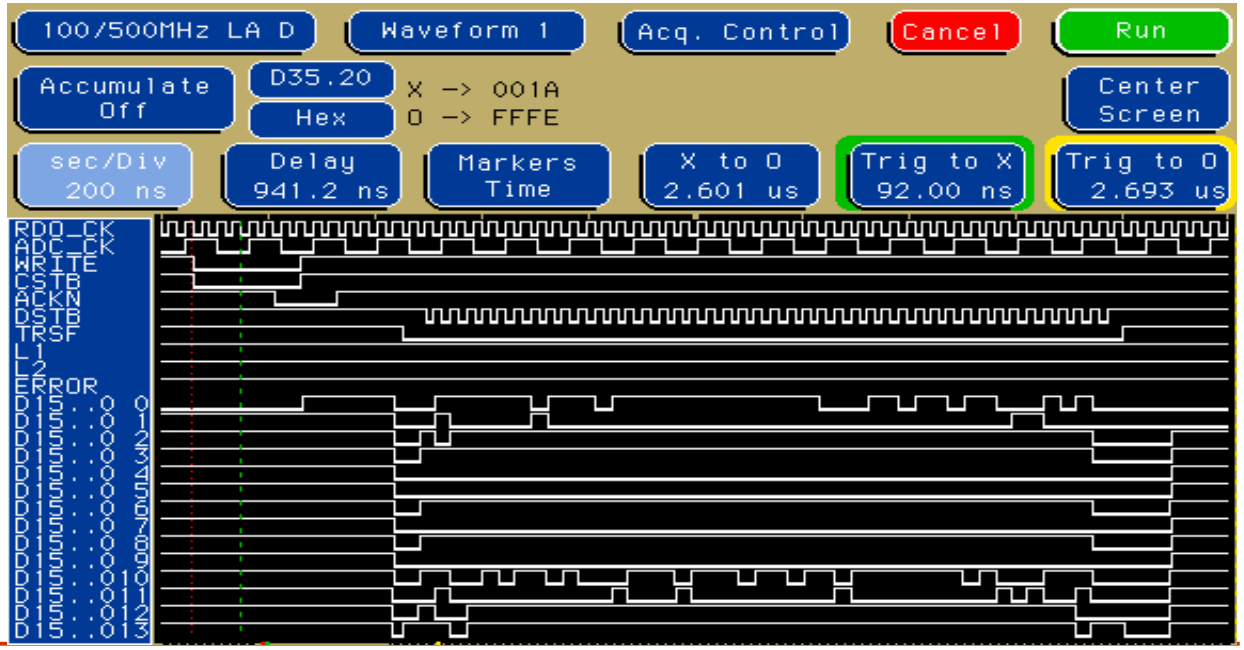


Communications with the FEC

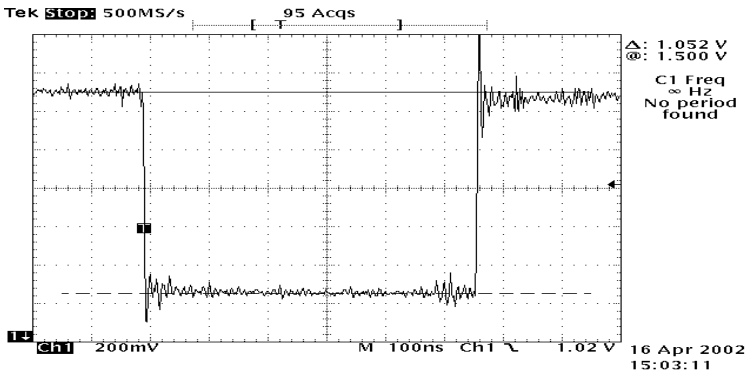
Access to an Altro Register (Write and Read)



Event download (Transfer)

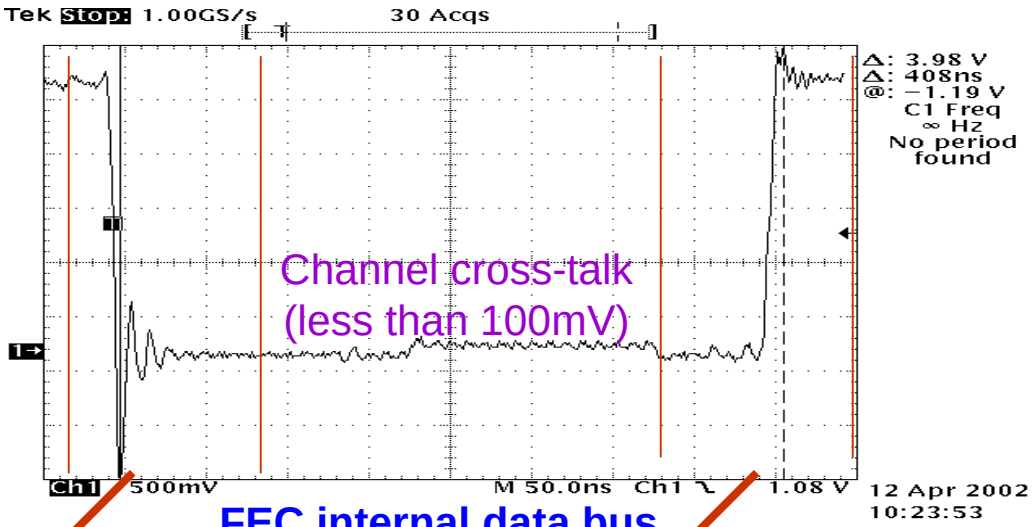


GTL and internal bus Overall signal quality

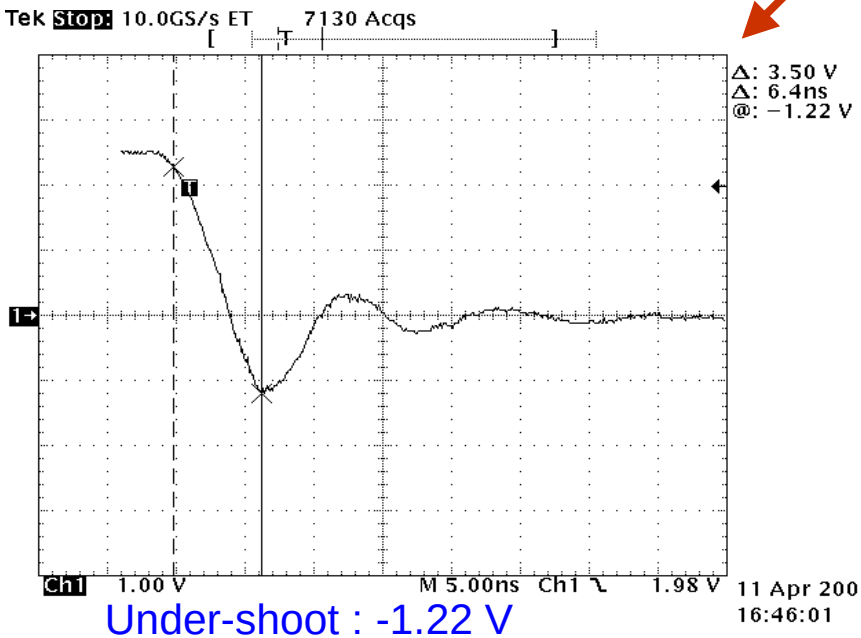


GTL+ bus noise margin

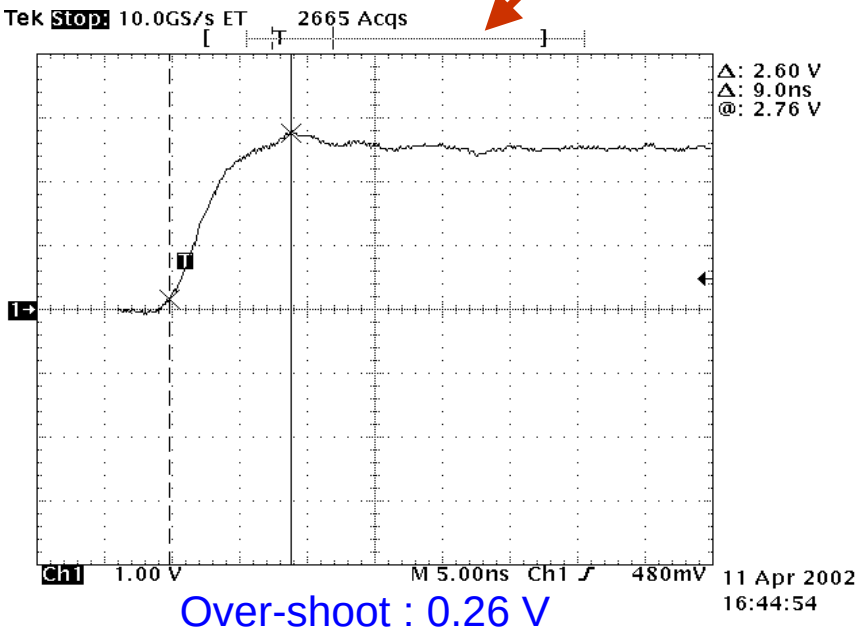
(more than 700 mV)



FEC internal data bus



Under-shoot : -1.22 V



Over-shoot : 0.26 V

FEC Power Consumption

- Board Controller : 140 mW
- Slow control circuitry : 5 mW
- ADC and Read Out Clock fan-out :~ 500 mW
- GTL transceivers : 60 mW
- 8 ALTRO : ~ 2060 mW
- 8 PASA : ~ 1530 mW
- Polarization circuitry: 7mW
- Power Regulators (20% avg. drop):~ 860 mW

TOTAL POWER CONSUMPTION : ~ 5200 mW => 40.5 mW / channel

Conclusions

Preliminary tests shown that the present version of Front end Card fully satisfies the requirements for the interface of the ALTRO chip to the read out bus.

Nevertheless the design features related to the analog section of the card (PASA chips and related signals routing) have still to be verified because of the logic for the read-out of events by the RCU is still under construction.