

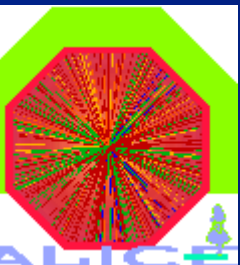
Readout Control Unit Status

Overview

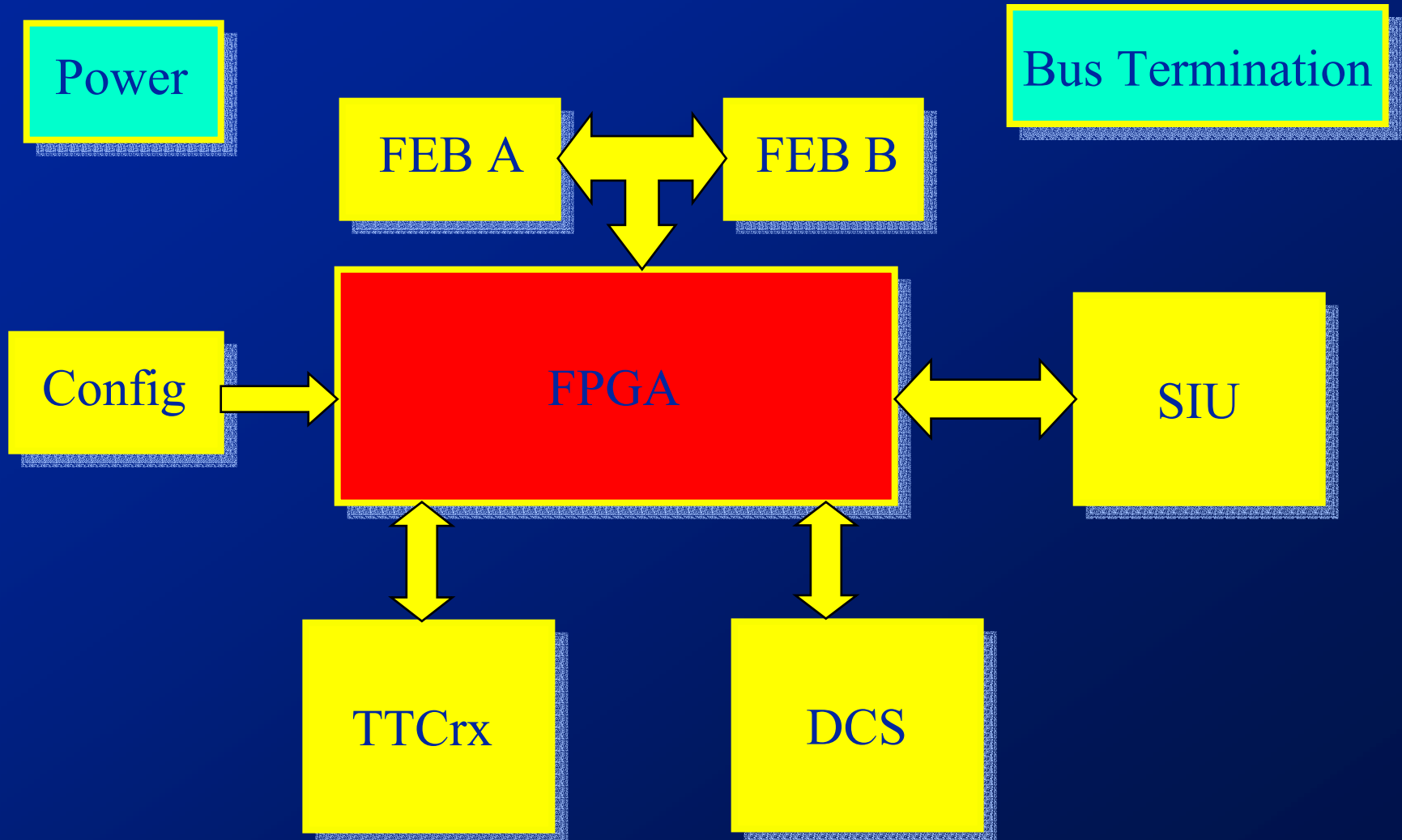
RCU card and sub-cards

Status of different modules/tasks

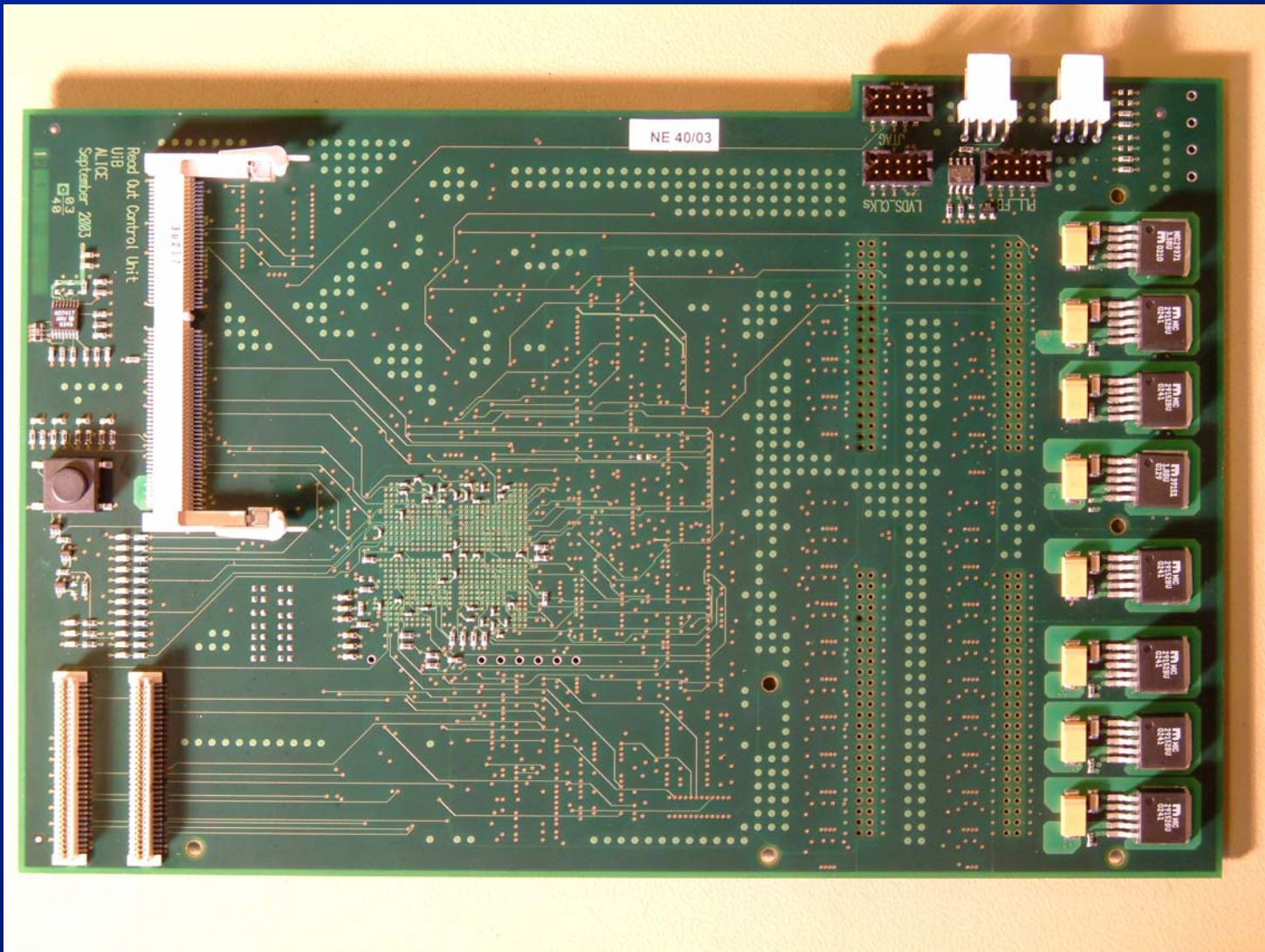
Milestones



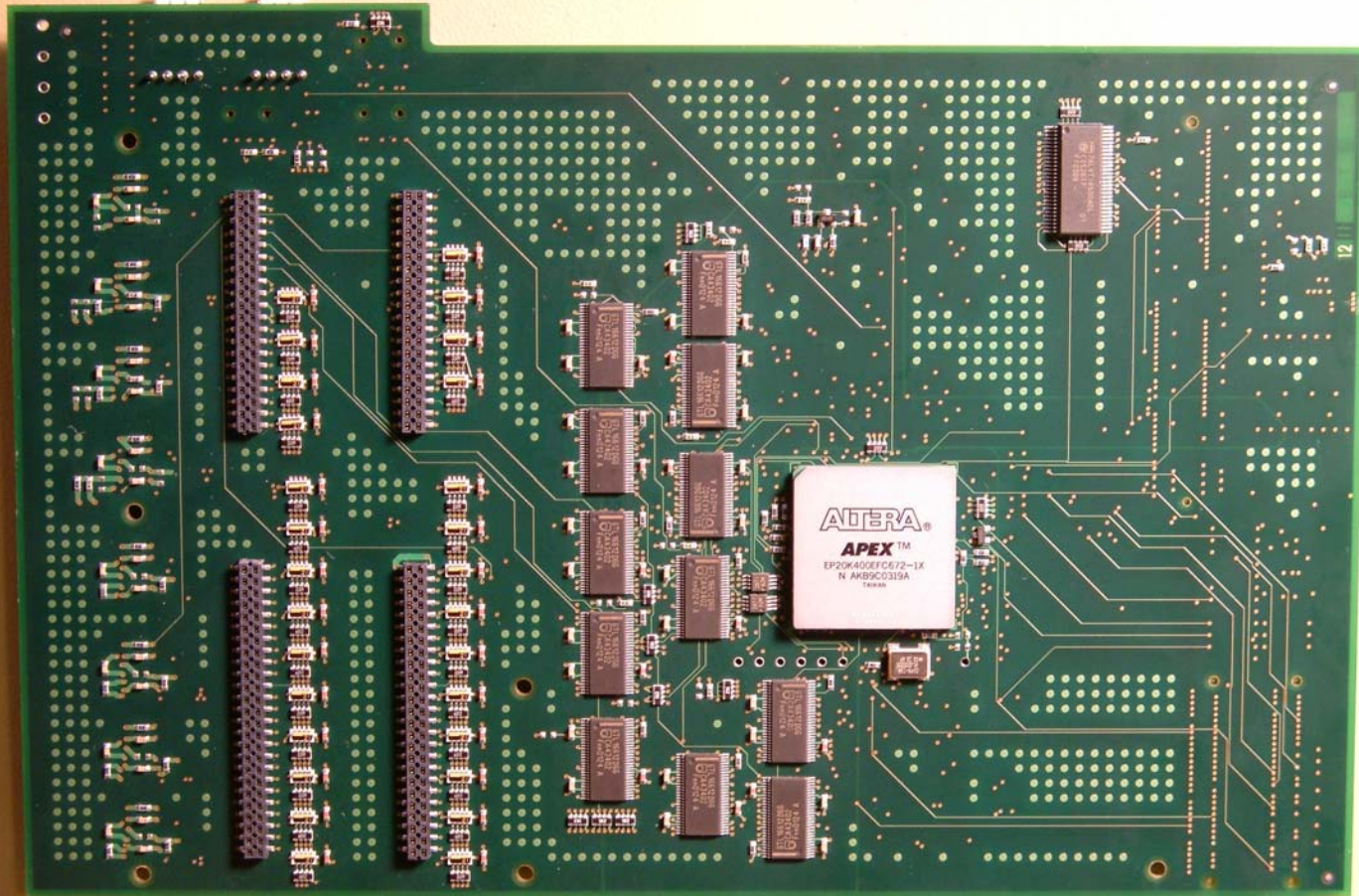
RCU Main Building Blocks



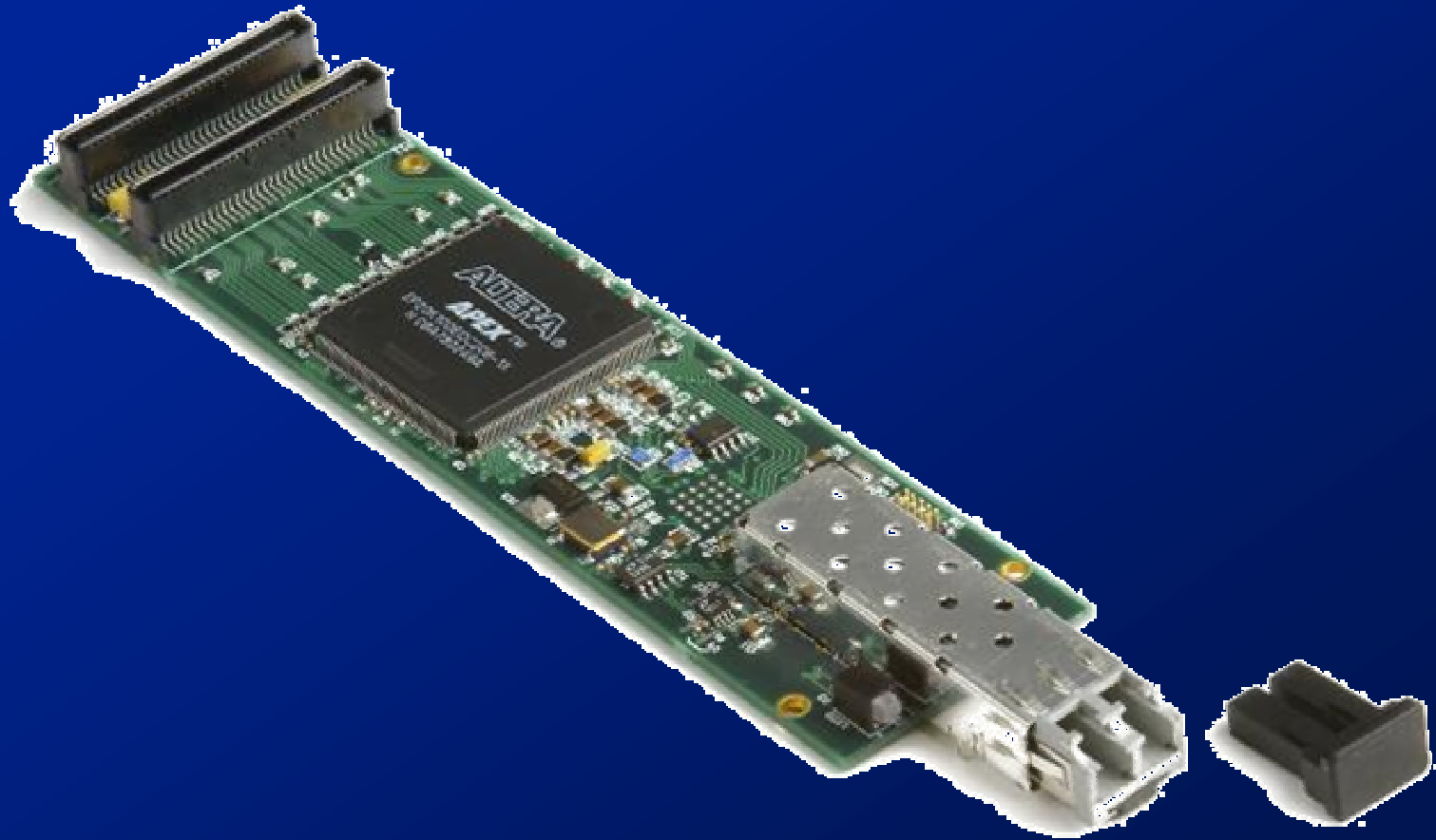
RCU Main PCB Top View



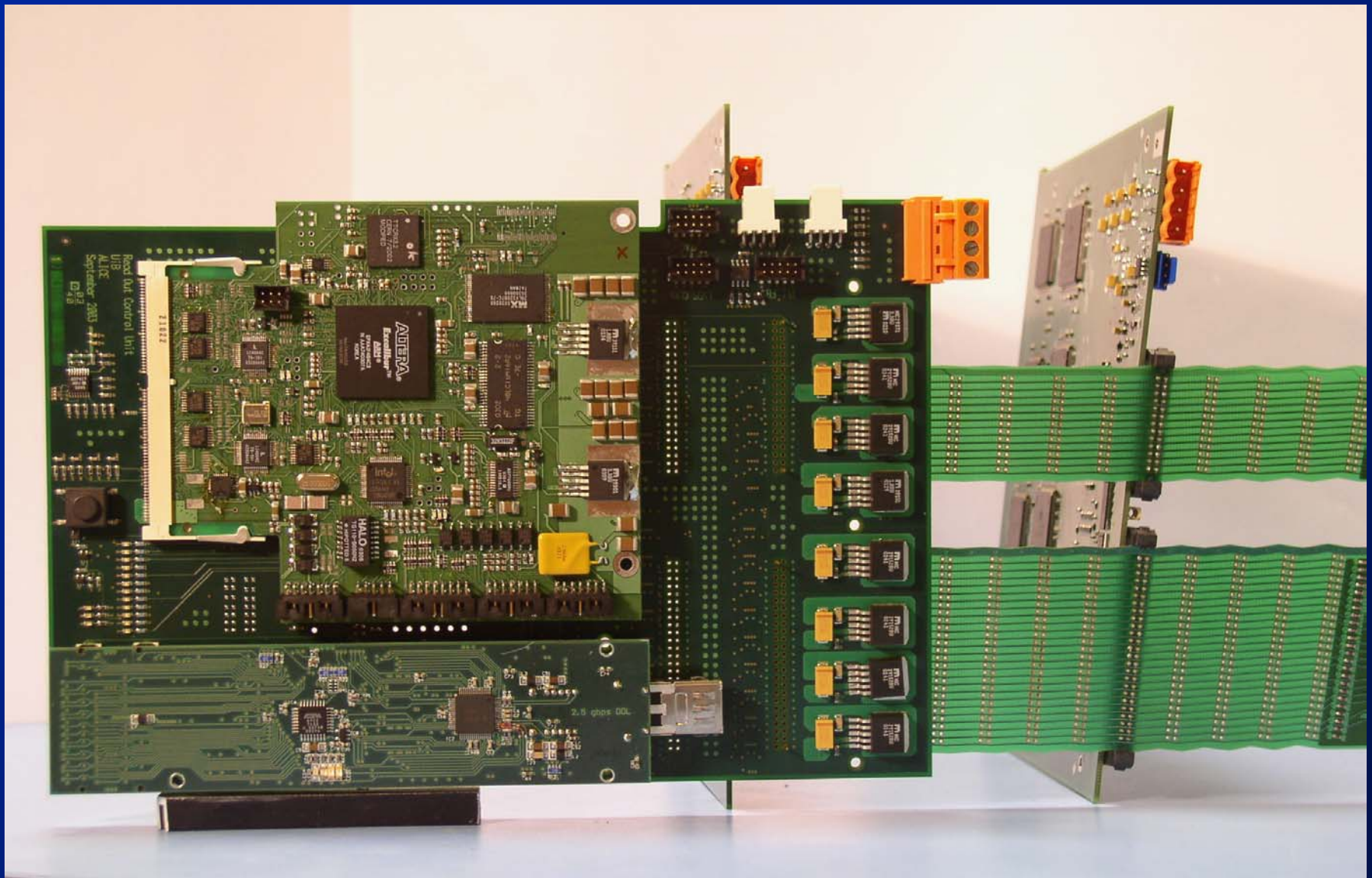
RCU Main PCB Bottom View



SIU board



RCU card with FEC



Internal and external connections

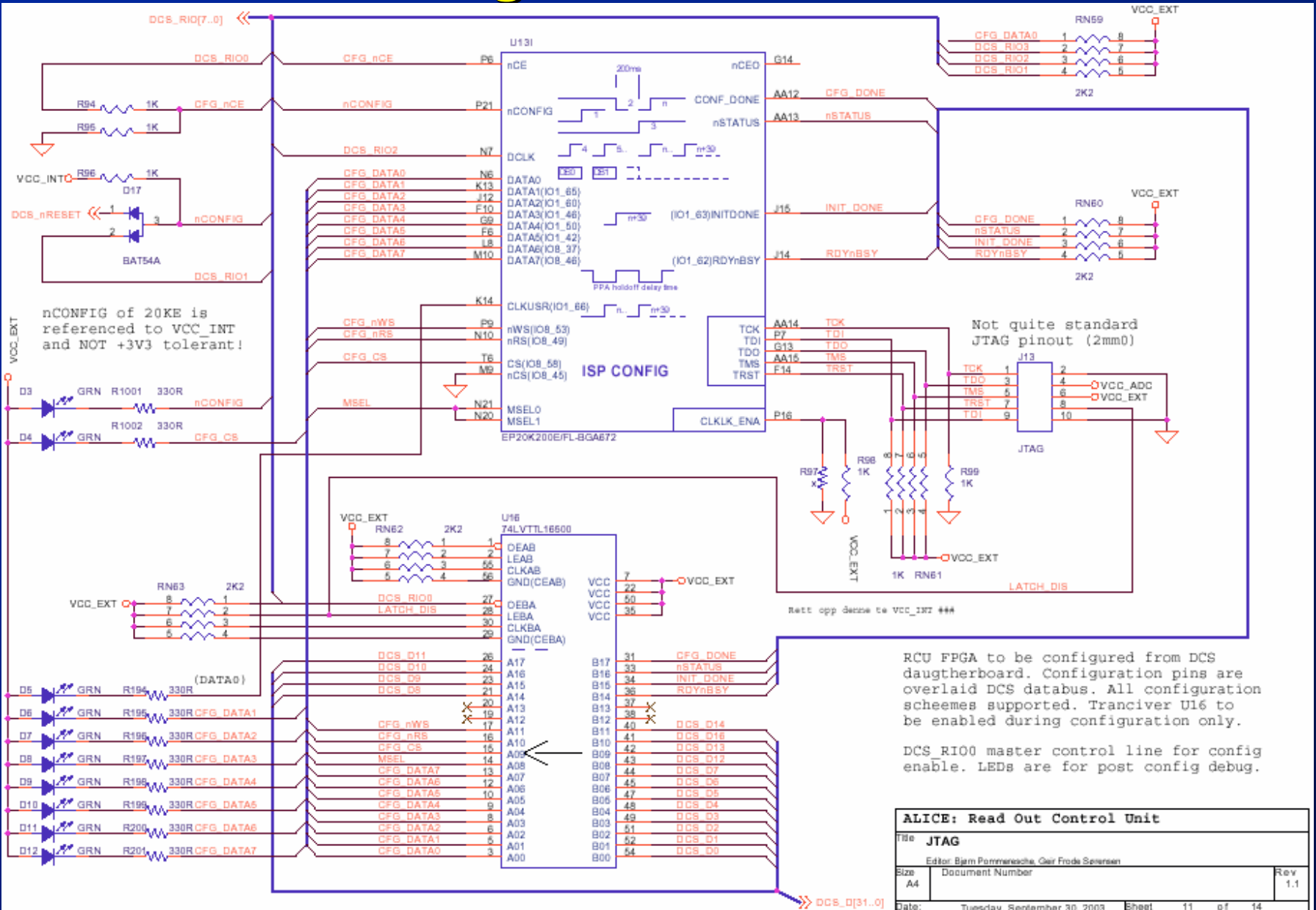
- **Internal**

- Connections from the FECs via backplane to the RCU MB
- Connections from RCU MB to TTCrx/DCS board via 144 pin connector
 - Includes programming interface from TTCrx/DCS board to RCU MB
- Connections from RCU MB to SIU card via CMC connectors
- Possible JTAG to TTCrx/DCS board from neighbour TTCrx/DCS board

- **External**

- Trigger information on Optical Link
- Data stream from SIU to DAQ on Optical link
- Power to RCU MB which is distributed to the DCS and the SIU boards
- Ethernet to TTCrx/DCS board

Configuration Scheme



RCU design Web Page

The screenshot shows a Microsoft Internet Explorer browser window with the title 'FEC - Microsoft Internet Explorer'. The address bar contains 'D:\rcu\index.htm'. The page content includes a header 'Read out Control Unit', a navigation bar with 'Back', 'Home', 'Up', and 'Next' buttons, and a main section titled 'Read out Control Unit (revision 1.1 - Oct '03)'. This section contains a list of links: 'Schematics (pdf)', 'Components numbering top (pdf)', 'Components numbering botom (pdf)', 'Pinning table EP20K200EFL-BGA672 (generated from Capture Cis) (xls)', 'More to come', and 'PCB GERBER files ()'. Below this list is a vertical list of layer files from 'Lay01.pdf (top)' to 'Lay12.pdf (bottom)'. The bottom of the page shows the start of a section titled 'Picture of the PCB'.

FEC - Microsoft Internet Explorer

Datei Bearbeiten Ansicht Favoriten Extras ?

Zurück Suchen Favoriten Medien

Adresse D:\rcu\index.htm Wechseln zu Links

Read out Control Unit

Back Home Up Next

Read out Control Unit (revision 1.1 - Oct '03)

- Schematics ([pdf](#))
- Components numbering top ([pdf](#))
- Components numbering botom ([pdf](#))
- Pinning table EP20K200EFL-BGA672 (generated from Capture Cis) ([xls](#))
- More to come
- PCB GERBER files ()

Lay01 [.pdf \(top\)](#)
Lay02 [.pdf](#)
Lay03 [.pdf](#)
Lay04 [.pdf](#)
Lay05 [.pdf](#)
Lay06 [.pdf](#)
Lay07 [.pdf](#)
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Lay09 [.pdf](#)
Lay10 [.pdf](#)
Lay11 [.pdf](#)
Lay12 [.pdf \(bottom\)](#)

Picture of the PCB

Status of external Communication

- RCU <-> DCS DIM Server Client Scheme over ethernet
(Presented by Christian Kofler)
- RCU <-> Trigger VME based test setup (VP 110 CPU board
running LINUX, TTCvi – Bergen)
Developed during summer 2003 at Cern
- RCU <-> DiU pRORC or HRORC based Test setup
- RCU <-> FEC Front End Card Interface
(Presented by Bernardo Mota)

Milestones

- **Milestones:**
 - **Design Document:** 1st ed Finished
 - **Module interface definitions:** Finished
 - **Module functional definitions:** Finished
 - **Implementation of the essential modules:** June/July 2003
 - **Radiation tests:** Partially finished
 - Oslo Cyclotron: October/November 2003
 - Uppsala TSL: November 2003
 - **Schematic design:** Finished August 2003
 - **PCB Layout:** Finished September 2003
 - **Engineering prototype:** Finished October 2003
 - **Test Firmware:** December 2003
 - **Hardware/Firmware integration:** December 2003
 - **Partial System Integration:** January 2004
 - **Qualification of the final design:** October 2003-March 2004
 - **Production:** Apr. 2004-July 2004
 - **Mass.production test:** August 2004 - March 2005
 - **RCU ready for installation:** October 2004

Open issues

- Migration to Actel

