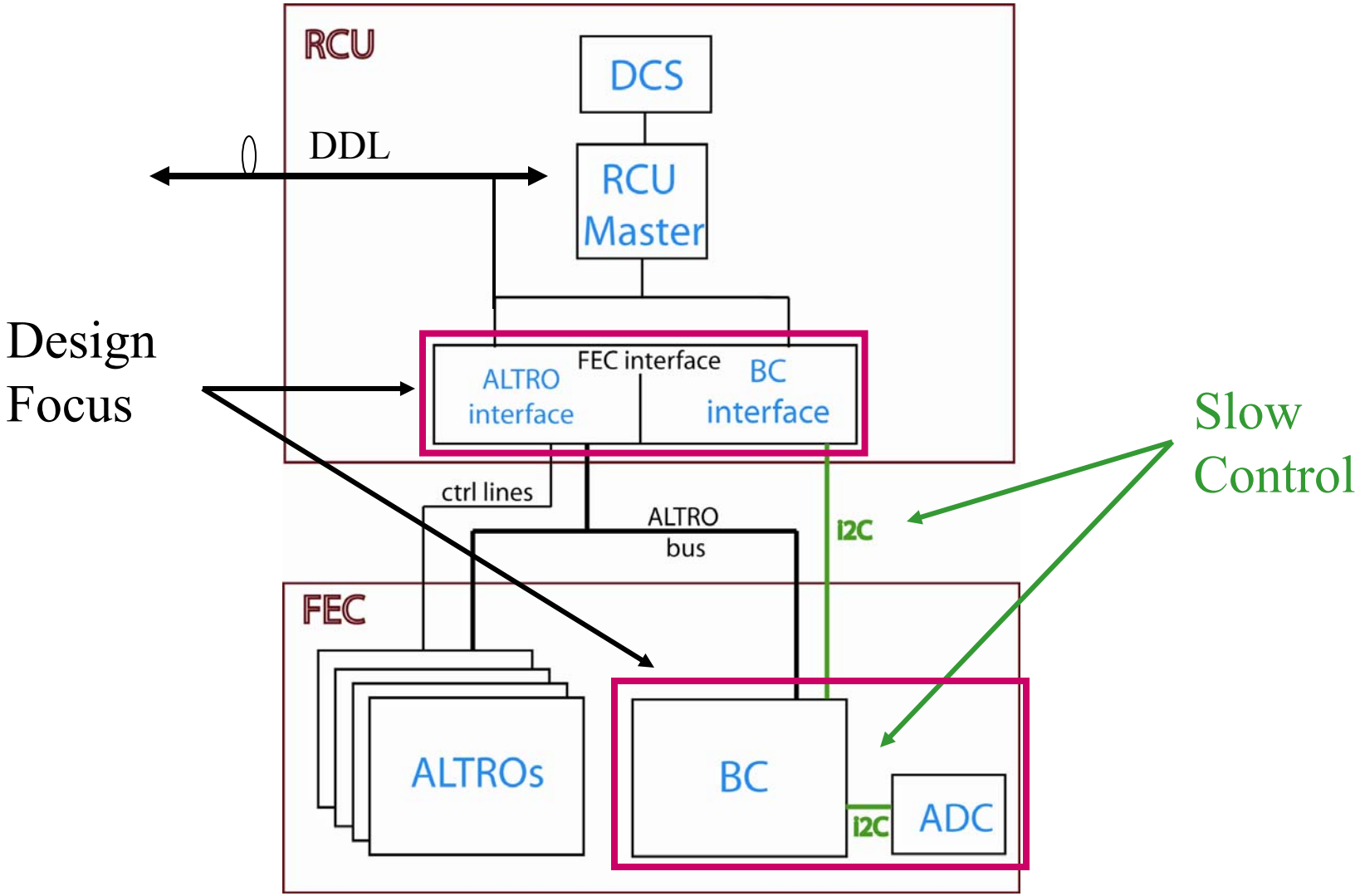
Front-End Card Interface of the RCU

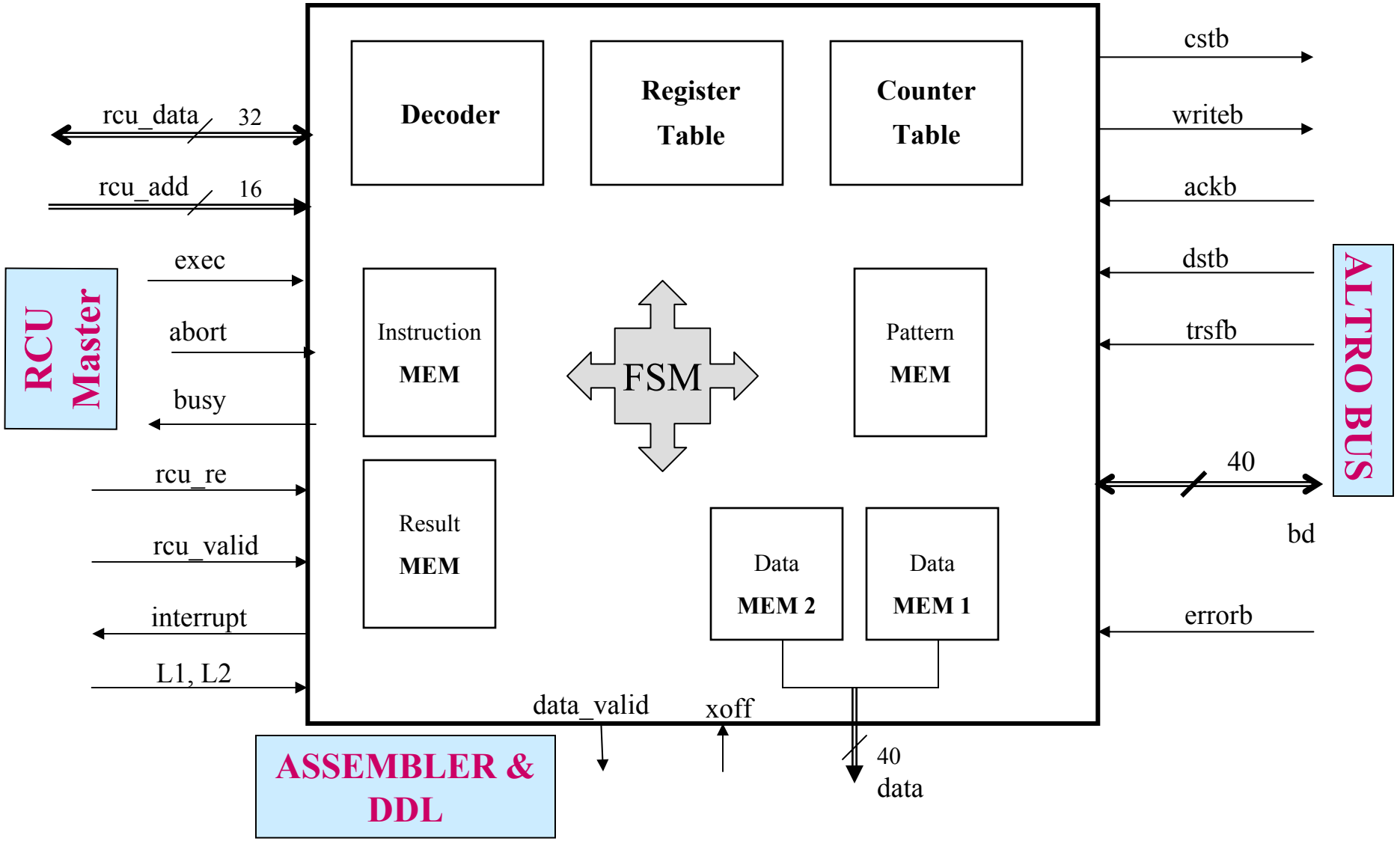
(Bernardo Mota & Carmen Gonzalez Gutierrez)

- ALTRO Interface
  - Block diagram
  - Memories and Functionality
  - Macro Instructions
  - “Microcontroller” Code
  - FEC debugging capabilities
- Board Controller Interface
  - Block diagram
  - Table of Registers
- Present Status

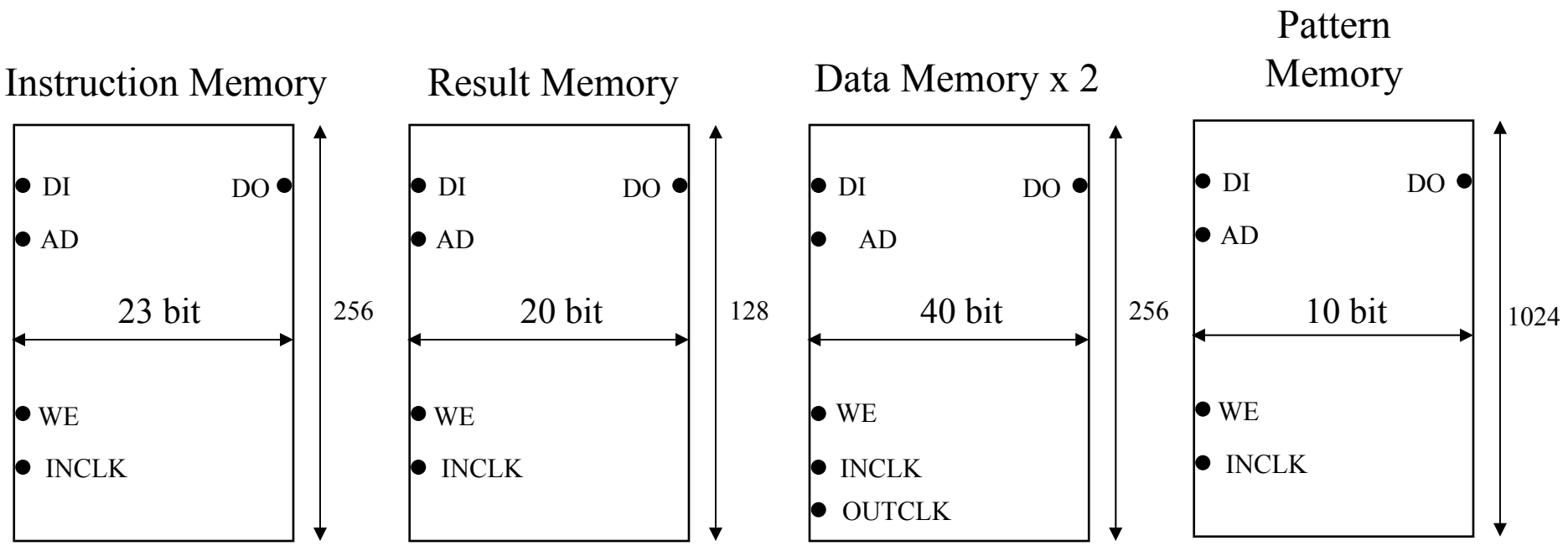
FEC Interface: *Block Diagram*



ALTRO Interface: *Block Diagram*

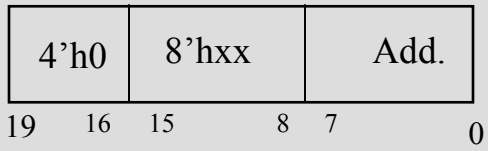


ALTRO Interface: *Memories and Functionality*

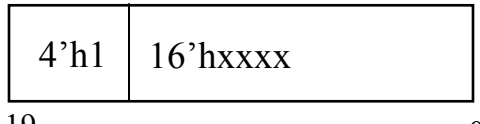


ALTRO Interface: *RCU Macro Instructions*

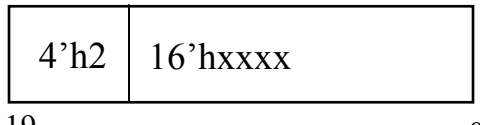
JUMP



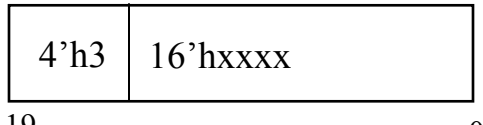
RS_STATUS



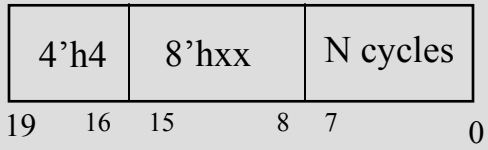
RS_L1CNT



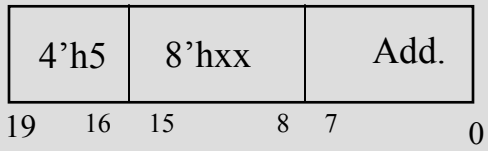
RS_L2CNT



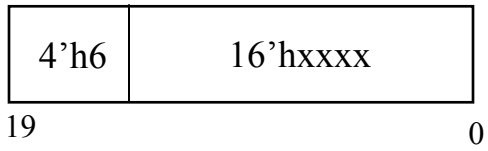
LOOP



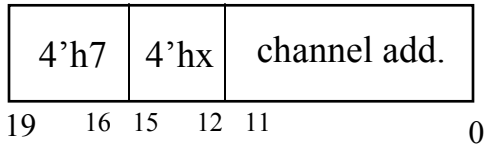
RETURN



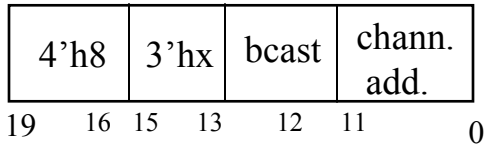
CHRDO



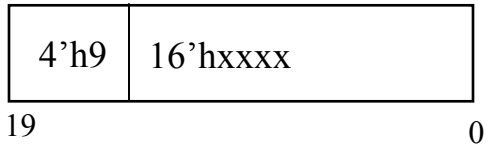
PMREAD



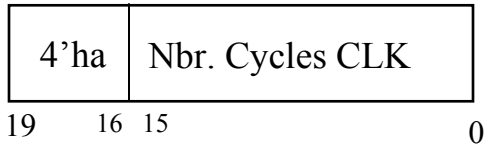
PMWRITE



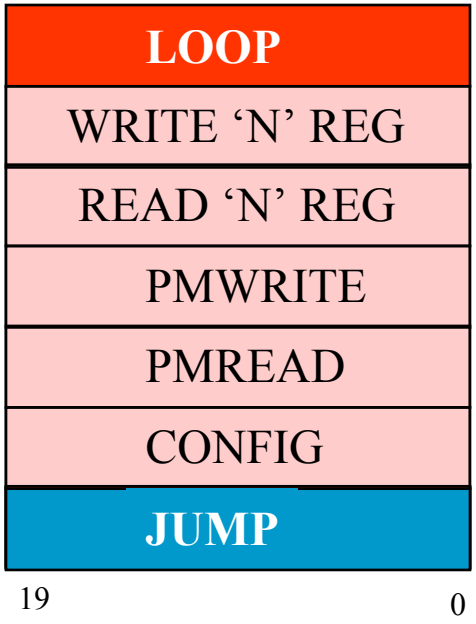
END



WAIT

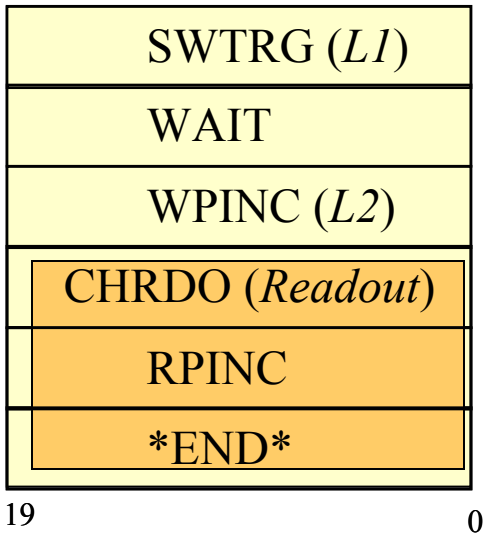


ALTRO Interface: *Microcontroller "code"*



Testing Registers and Memories of the ALTROs & Configuration

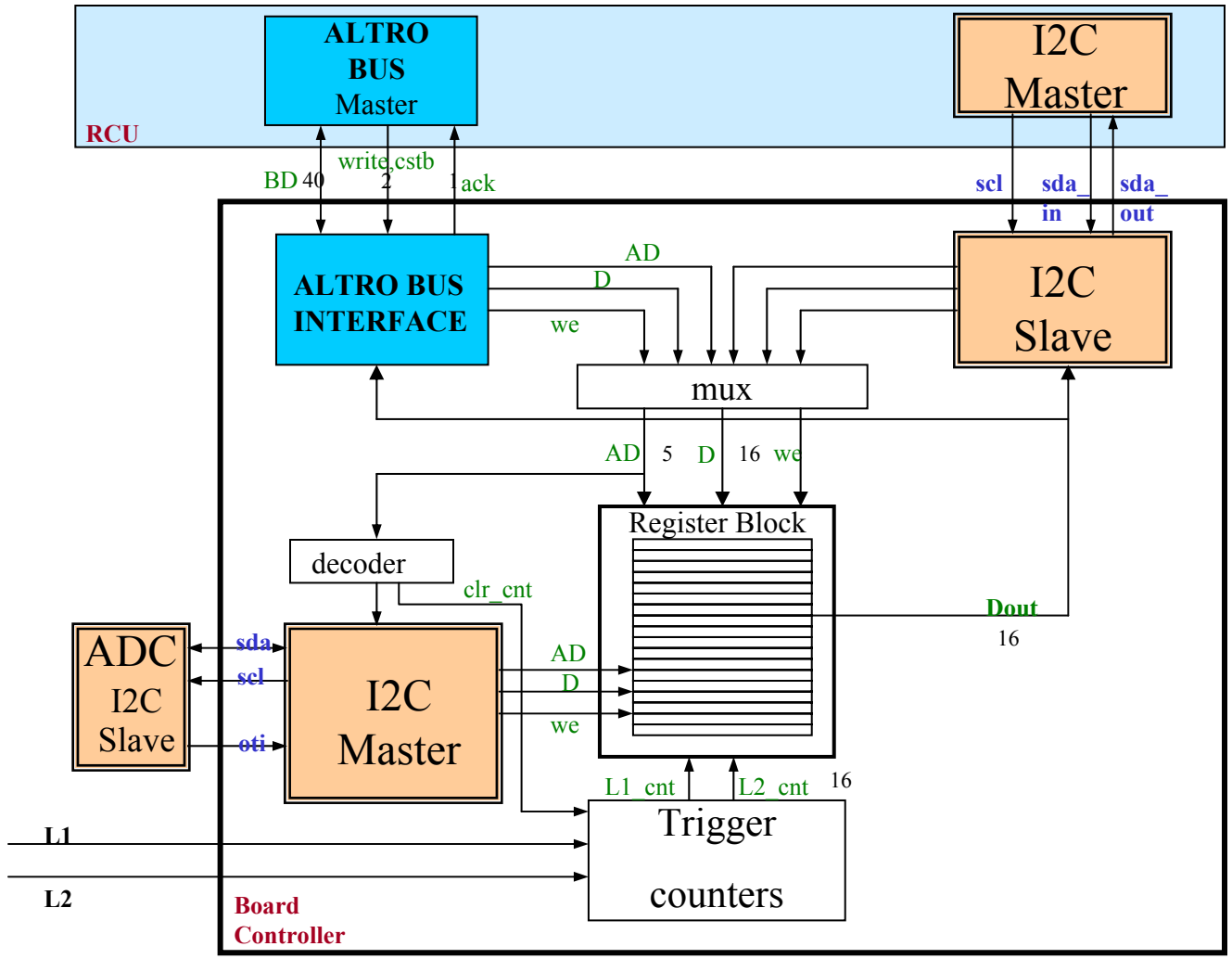
Testing Multi-Event Buffer & Readout



Normal Trigger sequence

ALTRO Interface: *Debugging Capabilities*

BC Interface: *Block Diagram*



BC Interface: *Table of Registers*

Reg. Addr.	*Mnemonic*	*Reg. Name*	*Width*	*Acc. Mode*	*Allow Bcast*	*Meaning*
01	T_TH	Temperature Thr.	10	R/W	Y	Maximum Temperature Threshold
02	AV_TH	AV threshold				Minimum Analog Voltage Threshold
03	AC_TH	AC threshold				Maximum Analog Current Threshold
04	DV_TH	DV threshold	10	R/W	Y	Minimum Digital Voltage Threshold
05	DC_TH	DC threshold	10	R/W	Y	Maximum Digital Current Threshold
08	TEMP	Temperature	10	R	N/A	Temperature Value
09	AV	Analog Voltage				Analog Voltage Value
0A	AC	Analog Current				Analog Current Value
0B	DV	Digital Voltage	10	R	N/A	Digital Voltage Value
0C	DC	Digital Current	10	R	N/A	Digital Current Value
10	L1CNT	L1 Counter				Number of L1 Trigger Received
11	L2CNT	L2 Counter				Number of L2 Trigger Received
12	SCLKCNT	Sampling clk counter	16	R	N/A	Sampling Clock counter
13	DSTBCNT	Data Strobe Counter	8	R	N/A	Number of Data Strobe in the last ReadOut

THRESHOLDS

MEASURABLES

COUNTERS

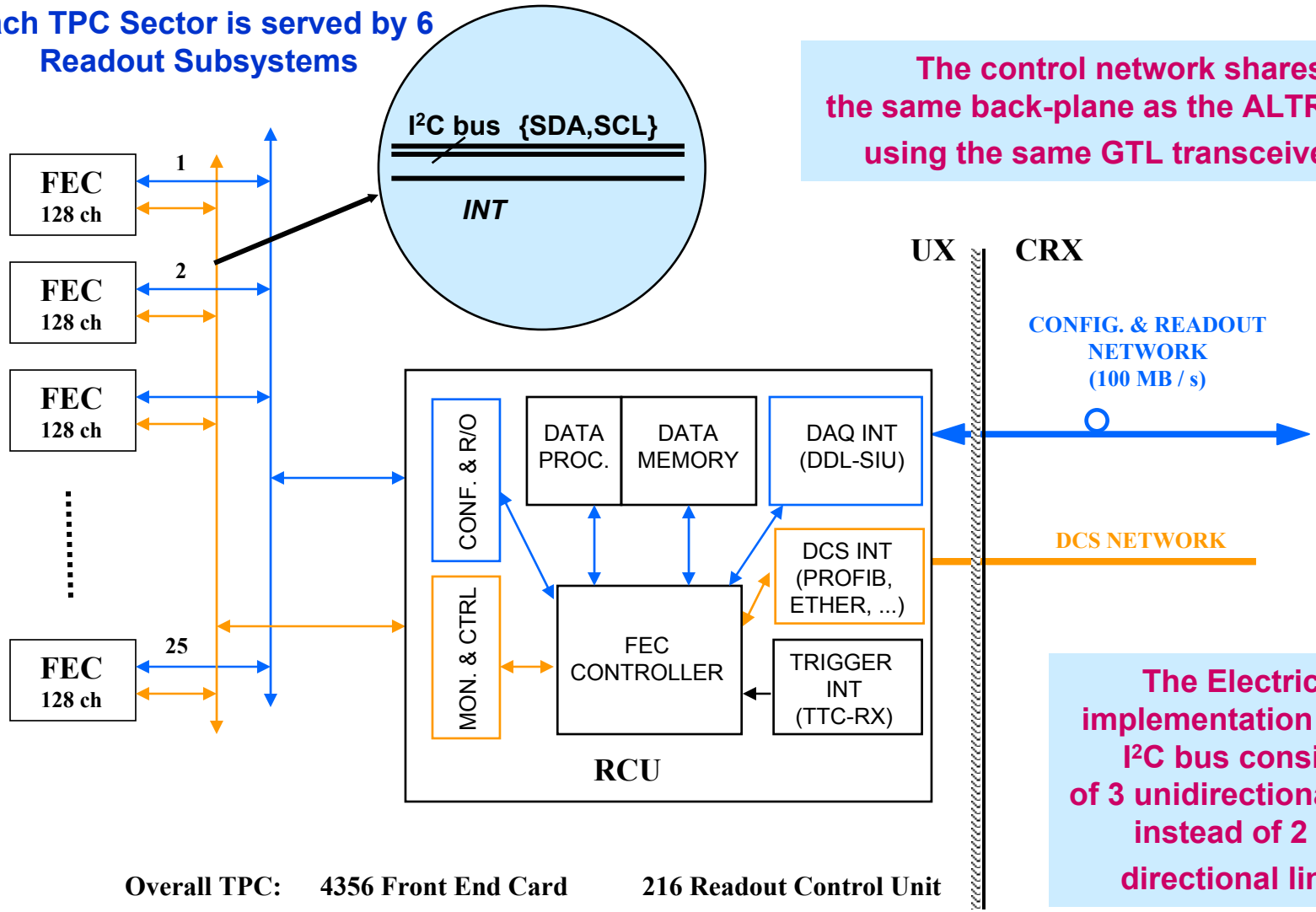
BC Interface: *Table of Registers*

14	CSR0	Configuration Status 0	14	R/W		Interrupt - Mask Register
15	CSR1	Configuration Status 1	14	R		Error Status Register
16	CSR2	Configuration Status 2	16	R/W		Card Configuration Status Register

18	CNTLAT	Counters Latch	-	W	Y	Latch L1, L2, SCLK counters
19	CNTCLR	Counters Clear	-	W	Y	Clear L1, L2, SCLK counters
1A	CSR1CLR	Conf. St. Reg 1 Clear	-	W	Y	Clear Error Status Register
1B	ALRST	ALTRO Reset	-	W	Y	Reset all the ALTROs
1C	BCRST	BC Reset	-	W	Y	Reset Board Controller
1D	STCNV	Start Conversion mADC	-	W	Y	Start Conversion / Read Out Monitor ADC

BC Interface: *System level Architecture*

Each TPC Sector is served by 6 Readout Subsystems



The control network shares the same back-plane as the ALTRO bus, using the same GTL transceivers.

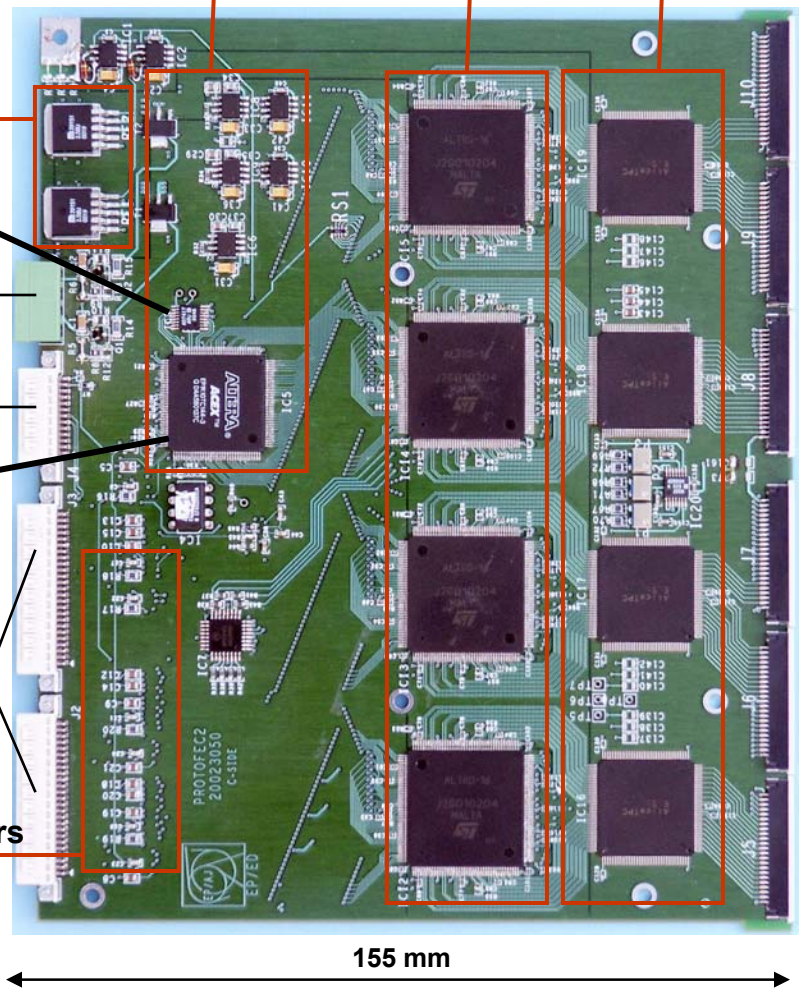
The Electrical implementation of the I²C bus consists of 3 unidirectional lines instead of 2 bi-directional links.

Overall TPC: 4356 Front End Card 216 Readout Control Unit

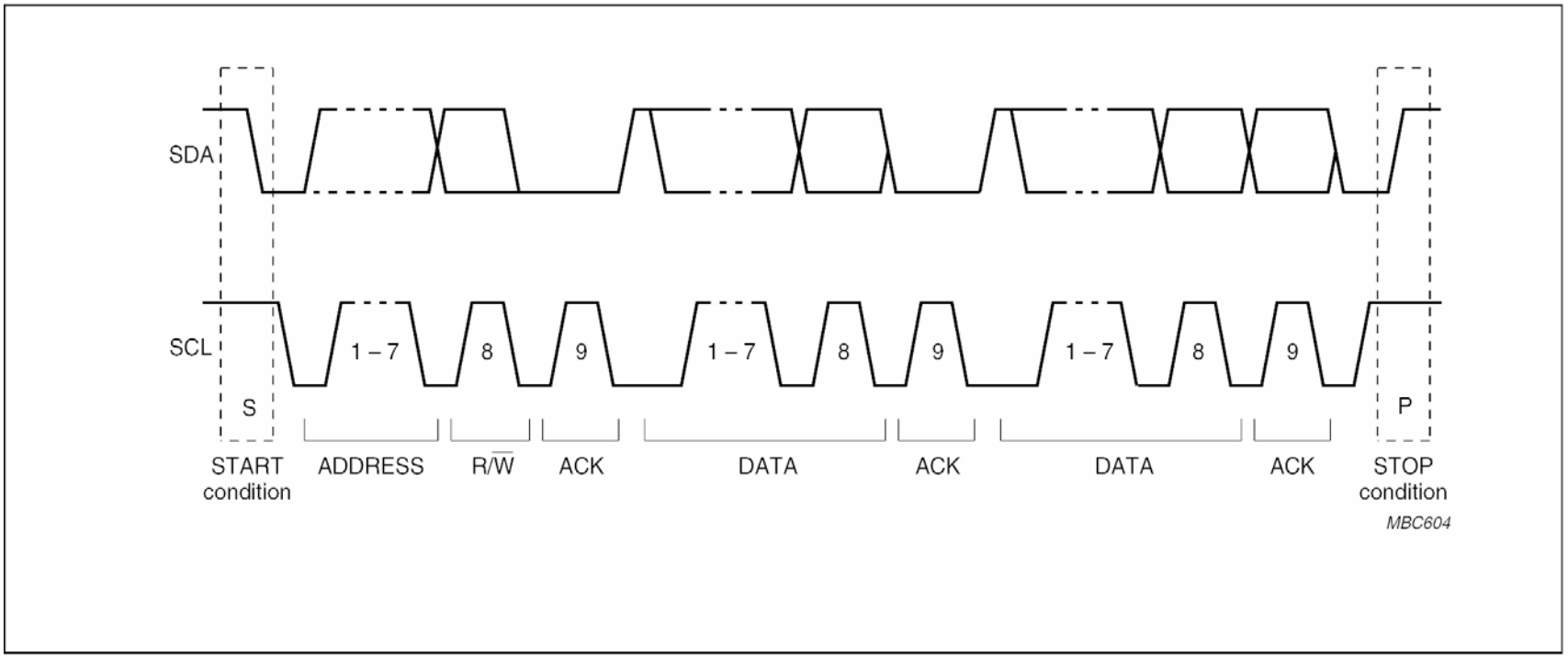
BC Interface: *Physical Layout*

5-channel 10bit ADC

FPGA hosting Board Controller logic and register set



BC Interface: *I2C Protocol*



BC Interface: *I2C Protocol*

- Transmission rate up to 3.4Mbit/sec in High Speed mode
- Worldwide standard protocol developed by Philips
- Maximum allowed bus capacitance of 400pF
- FECs can be connected or disconnected without disturbing the network functioning
- Bi-directional 8-bit serial data transfer
- Multi-master protocol with Arbitration

Present Status

ALTRO Interface

√ IP design completed and simulated

X Testing in PLDA board: End of October

√\ Additional macro instructions and active channel list to be included

Board Controller Interface

√ BC ⬌ ADC : Design completed, simulated and tested

√\ RCU ⬌ BC (I2C + ALTRO bus): integration and test missing