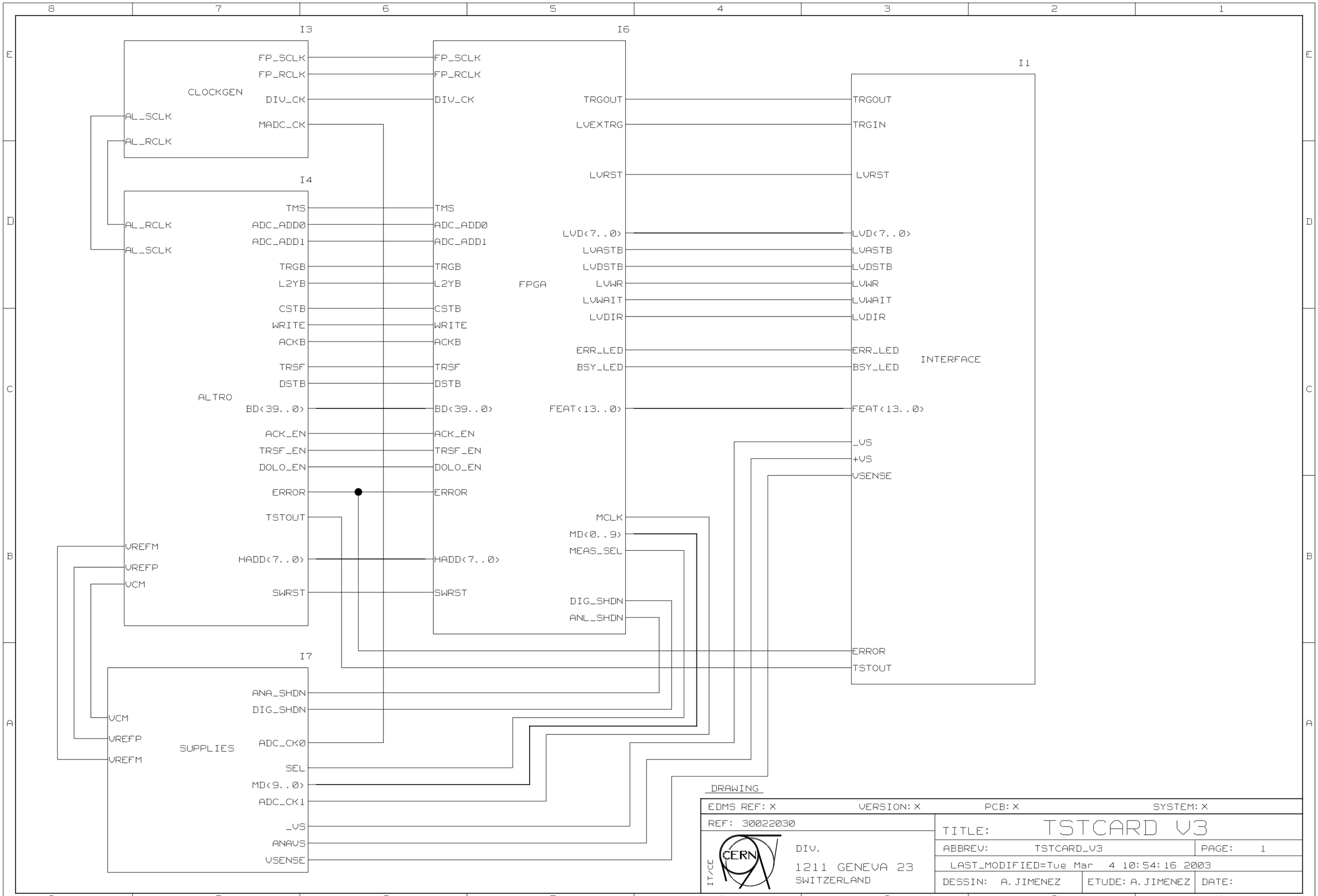

I3
CLOCKGEN
FP_SCLK
FP_RCLK
DIV_CK
MADC_CK
AL_SCLK
AL_RCLK
I4
ALTRO
TMS
ADC_ADD0
ADC_ADD1
TRGB
L2YB
CSTB
WRITE
ACKB
TRSF
DSTB
BD<39..0>
ACK_EN
TRSF_EN
DOLO_EN
ERROR
TSTOUT
HADD<7..0>
SWRST
VREFM
VREFP
VCM
I6
FPGA
TRGOUT
LVEXTRG
LVRST
LVD<7..0>
LVASTB
LVDSTB
LVWR
LVWAIT
LVDIR
ERR_LED
BSY_LED
FEAT<13..0>
MCLK
MD<0..9>
MEAS_SEL
DIG_SHDN
ANL_SHDN
I1
INTERFACE
TRGIN
_VS
+VS
VSENSE
I7
SUPPLIES
ANA_SHDN
ADC_CK0
SEL
MD<9..0>
ADC_CK1
ANAVS
DRAWING
EDMS REF: X
VERSION: X
PCB: X
SYSTEM: X
REF: 30022030
TITLE: TSTCARD V3
DIV.
1211 GENEVA 23
SWITZERLAND
IT/CE
ABBREV: TSTCARD_V3
PAGE: 1
LAST_MODIFIED=Tue Mar 4 10:54:16 2003
DESSIN: A. JIMENEZ
ETUDE: A. JIMENEZ
DATE:

PACKAGE TSSOP - DGG
P3V3=P2V5
IC13
74ALVC
164245
LVDIR
TP25
IN
4K7
R35
GND
IO
LVD<7..0>
LVDSTB
LVASTB
TP13
TP14
TP15
LVWR
OUT
LVDSTB
LVRST
LVASTB
TRGIN
1DIR
1OE
2DIR
2OE
1A<0>
1A<1>
1A<2>
1A<3>
1A<4>
1A<5>
1A<6>
1A<7>
1B<0>
1B<1>
1B<2>
1B<3>
1B<4>
1B<5>
1B<6>
1B<7>
2A<0>
2A<1>
2A<2>
2A<3>
2A<4>
2A<5>
2A<6>
2A<7>
2B<0>
2B<1>
2B<2>
2B<3>
2B<4>
2B<5>
2B<6>
2B<7>
100
R34
R32
R29
R27
R26
R25
R22
R21
D<7..0>
WR
DTSTB
PRST
ADSTB
TRG_IN
VCC
4.7K
R16
R17
R36
R33
R31
R28
J29
ADSTB
DTSTB
RESET
ERROR
SELECT
END
WAIT
INT
R75
R71
R66
R67
R65
R63
R62
R60
R59
R20
GENERIC EXTERNAL TRIGGER
PX5
TRG_IN
51
R97

PACKAGE TSSOP - DGG
P3V3=P2V5
IC10
P2V5
TP17
4K7
R24
LVWAIT
BSY_LED
TSTOUT
ERR_LED
ERROR
TRGOUT
ADVCC
VDD
100
R4
R3
4K7
R23
WAIT
R19
D3
BUSY
R16
D2
TSTOUT
R15
D1
ERROR
R14
560
D4
ALTRO ERROR
R13
D6
2.5V DIGITAL
R12
D5
2.5V ANALOG
R11
PX6
TRIGGER OUT
150
R96
GND

DECOUPLING TRANSLATORS
C9
C57
C77
C82
C94
C14
C55
C65
C75
C93
C83
C103
10uF
100NF

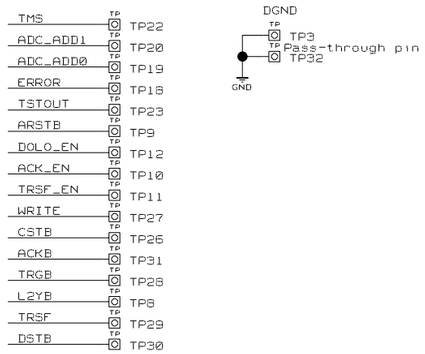
IO
+VS
VSENSE
FEAT<13..0>
_VS
Regulator
Daughtercard Socket
J55
J56
BARD10

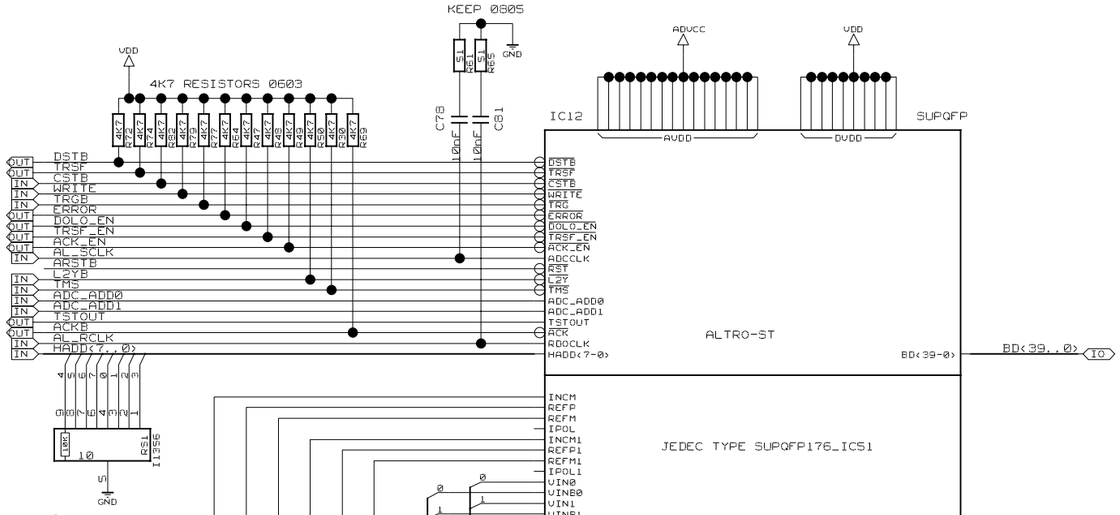
DRAWING
EDMS REF: X
VERSION: X
PCB: X
SYSTEM: X
REF: 30022030
CERN
IT/CE
DIV.
1211 GENEVA 23
SWITZERLAND
TITLE: INTERFACE
ABBREV: INT
PAGE: 6
LAST_MODIFIED=Tue Mar 4 11:02:40 2003
DESSIN: A.JIMENEZ
ETUDE: A.JIMENEZ
DATE:

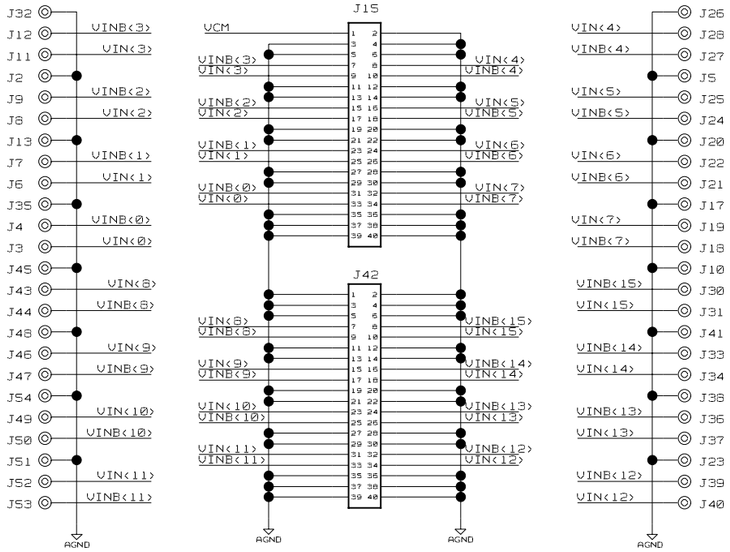
External Delay Cable
Stright Lemos
PX1
PX2
OUT AL_RCLK
R87 00
Impedance-Controlled Line
OUT FP_RCLK
Impedance-Controlled Line
IC19
MPC940L
VCCO VCCI
PCLK
PCLK
LCLK
SEL
GND
oGND iGND
P2V5
R37 360
C15 100NF
C17 100NF
C16 100NF
C121 15uF
GND
EXT
ST4
INT
PX4
EXTERNAL
RDO CLOCK
2.5 Vpp
R94 51
GND
VCC
QUARTZ1SPEED
QZ1 40MHz
OUT VCC
GND
SOCKET
R92 820
R40 820
C124 100NF
C125 10uF
GND
IC20
MPC940L
P2V5
R38 360
C119 100NF
C18 100NF
C115 100NF
C120 15uF
GND
OUT MADC_CK
OUT FP_SCLK
Impedance-Controlled Line
OUT AL_SCLK
Impedance-Controlled Line
EXT
ST3
INT
XTAL
ST5
FPGA
IN DIV_CK
PX3
EXTERNAL
ADC CLOCK
2.5 Vpp
R95 51
GND
VCC
QUARTZ1SPEED
10MHz QZ2
OUT VCC
GND
SOCKET
R93 820
R39 820
C122 100NF
C123 10uF
GND

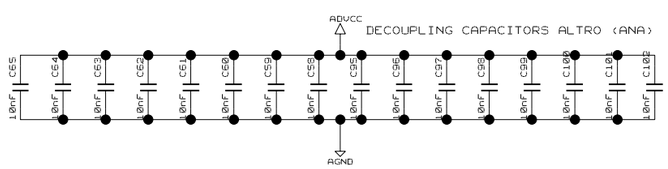
DRAWING

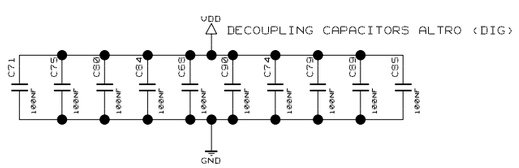
EDMS REF: X	VERSION: X	PCB: X	SYSTEM: X
REF: 30022030		TITLE: CLOCKGEN	
IT/CE CERN DIV. 1211 GENEVA 23 SWITZERLAND		ABBREV: CGEN	PAGE: 2
		LAST_MODIFIED=Tue Mar 4 10:54:10 2003	
		DESSIN: A. JIMENEZ	ETUDE: A. JIMENEZ DATE:

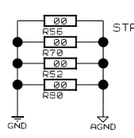


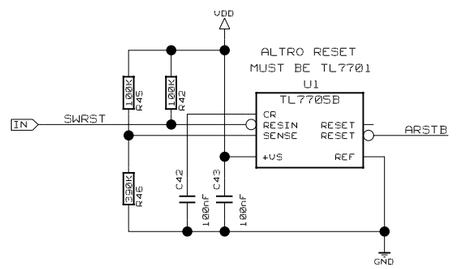












DRAWING

REF: 30022030

CERN CN/CE

DIV.

1211 GENEVA 23

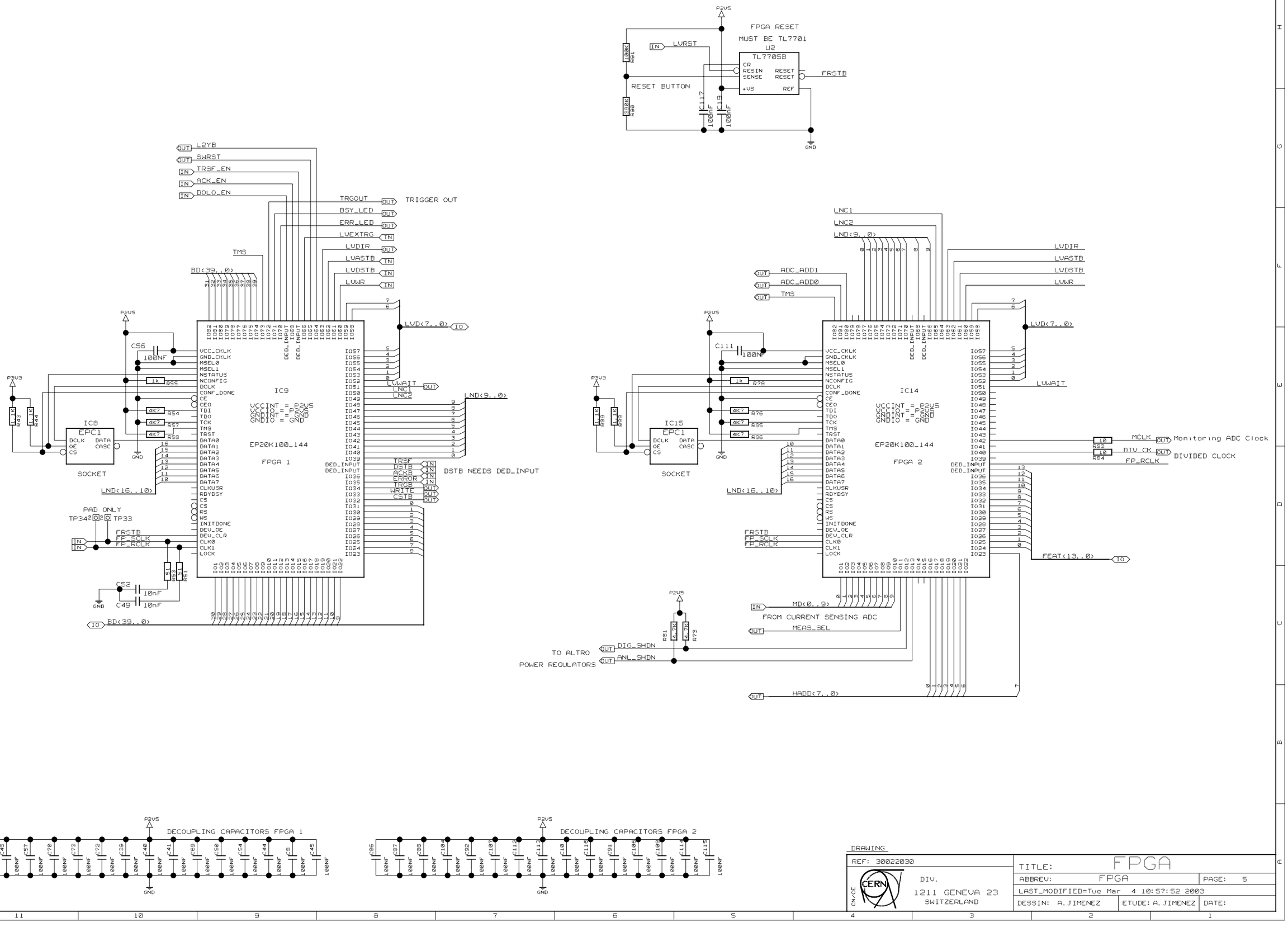
SWITZERLAND

TITLE: ALTRO

ABBREV: AL | PAGE: 3

LAST_MODIFIED=Tue Mar 4 10:54:40 2003

DESSIN: A.JIMENEZ | ETUDE:A.JIMENEZ | DATE:



DRAWING

REF: 30022030

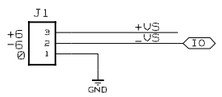
DIV.
1211 GENEVA 23
SWITZERLAND

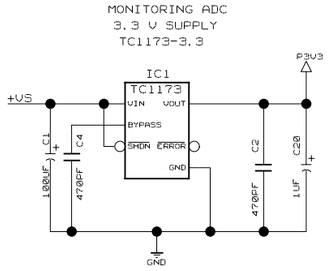
TITLE: FPGA

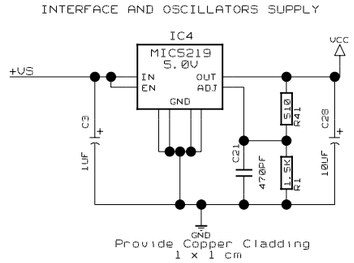
ABBREV: FPGA | PAGE: 5

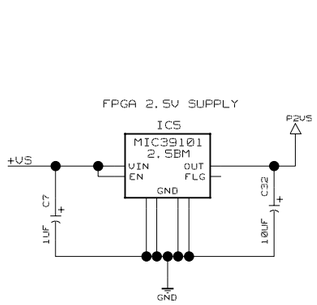
LAST_MODIFIED=Tue Mar 4 10:57:52 2003

DESSIN: A.JIMENEZ | ETUDE: A.JIMENEZ | DATE:

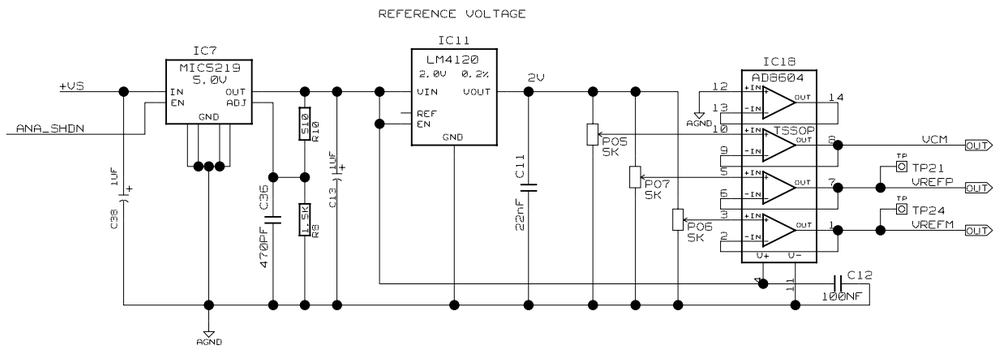




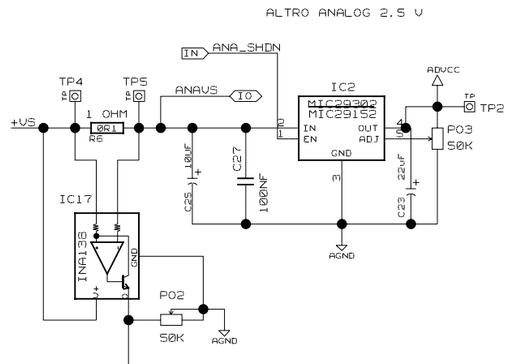


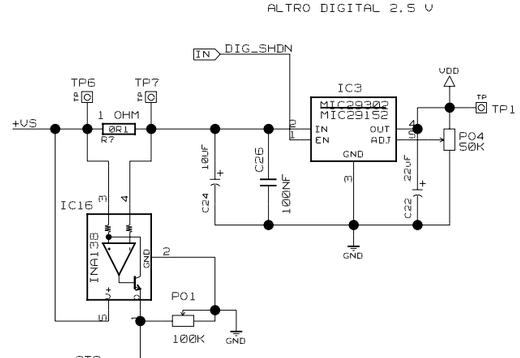


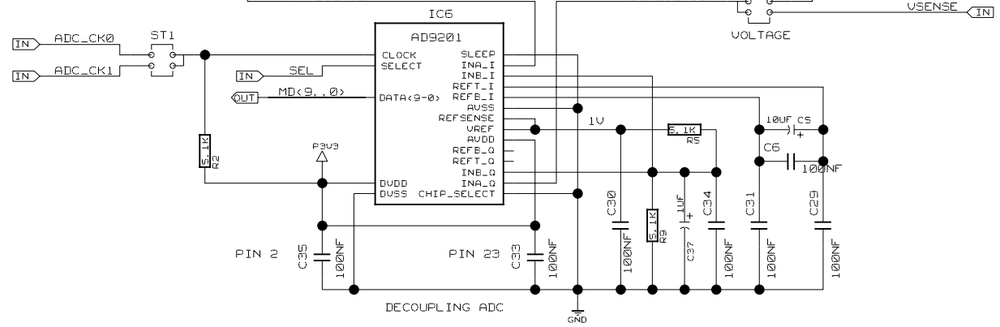
VDD = ALTRO 2.5V Digital
ADVCC = ALTRO 2.5V Analog
VCC = Interface and Oscillators 5V
P2V5 = FPGA, ClockBuf & Translators 2.5V
P3V3 = Monitoring ADC Supply 3.3V
GND = Digital Ground
AGND = Analog Ground



AGND AND GND JOINED UNDER REGULATOR







DRAWING

REF: 30022030	TITLE: SUPLLIES	
CERN DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: SUP	PAGE: 4
	LAST_MODIFIED=Tue Mar 4 10:53:25 2003	
	DESSIN: A.JIMENEZ	ETUDE: A.JIMENEZ DATE: