

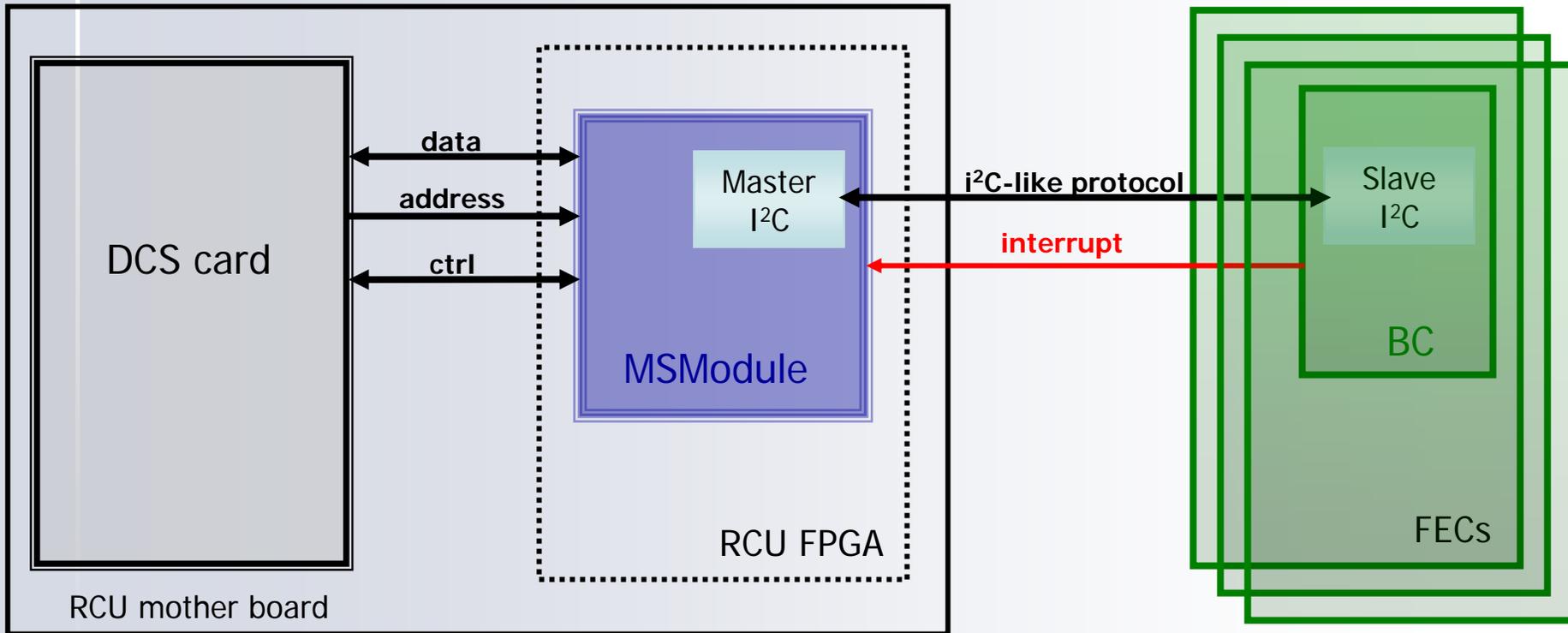
Monitoring and Safety Module

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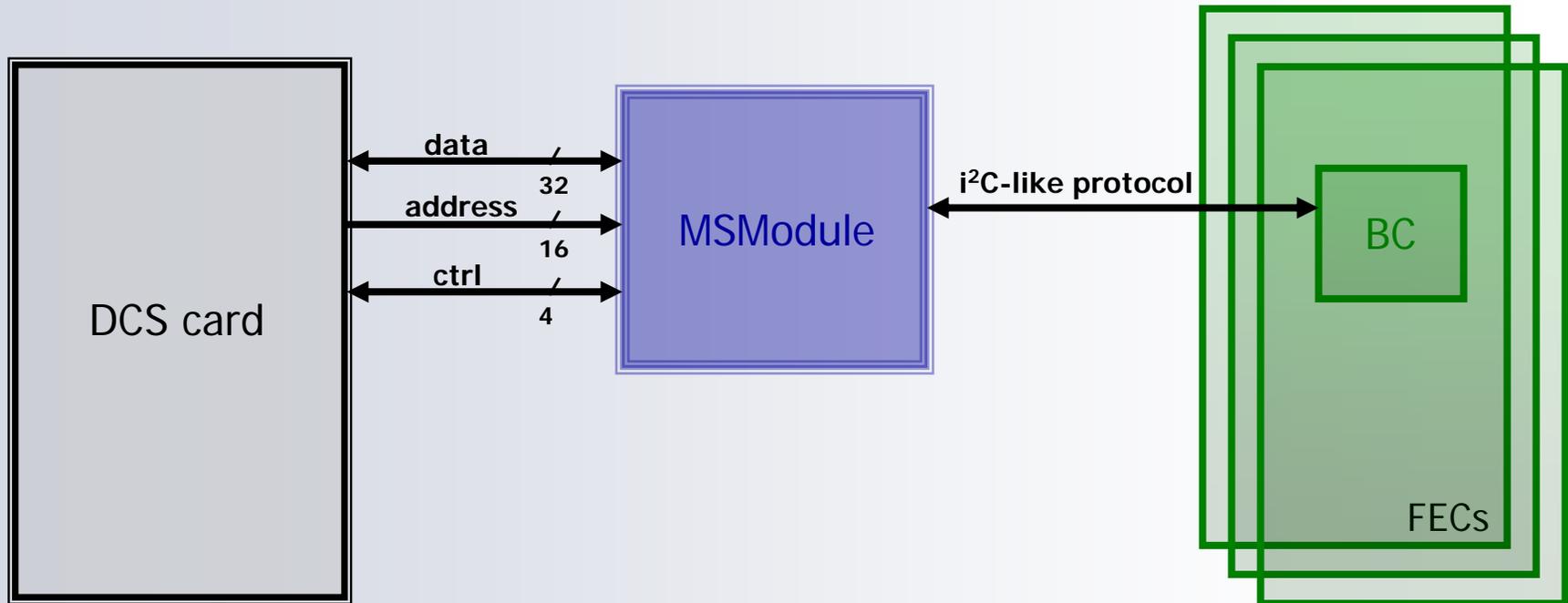
Monitoring and Safety Module

- MSModule is the block in the RCU FPGA responsible of the communication between the DCS and the Board Controller (BC) to **monitor** the status of the Front End Cards
- In case of abnormal situation (**interrupt**) in the FECs, the module **finds out** the problem (what and where), **handle the error** and **informs** the DCS

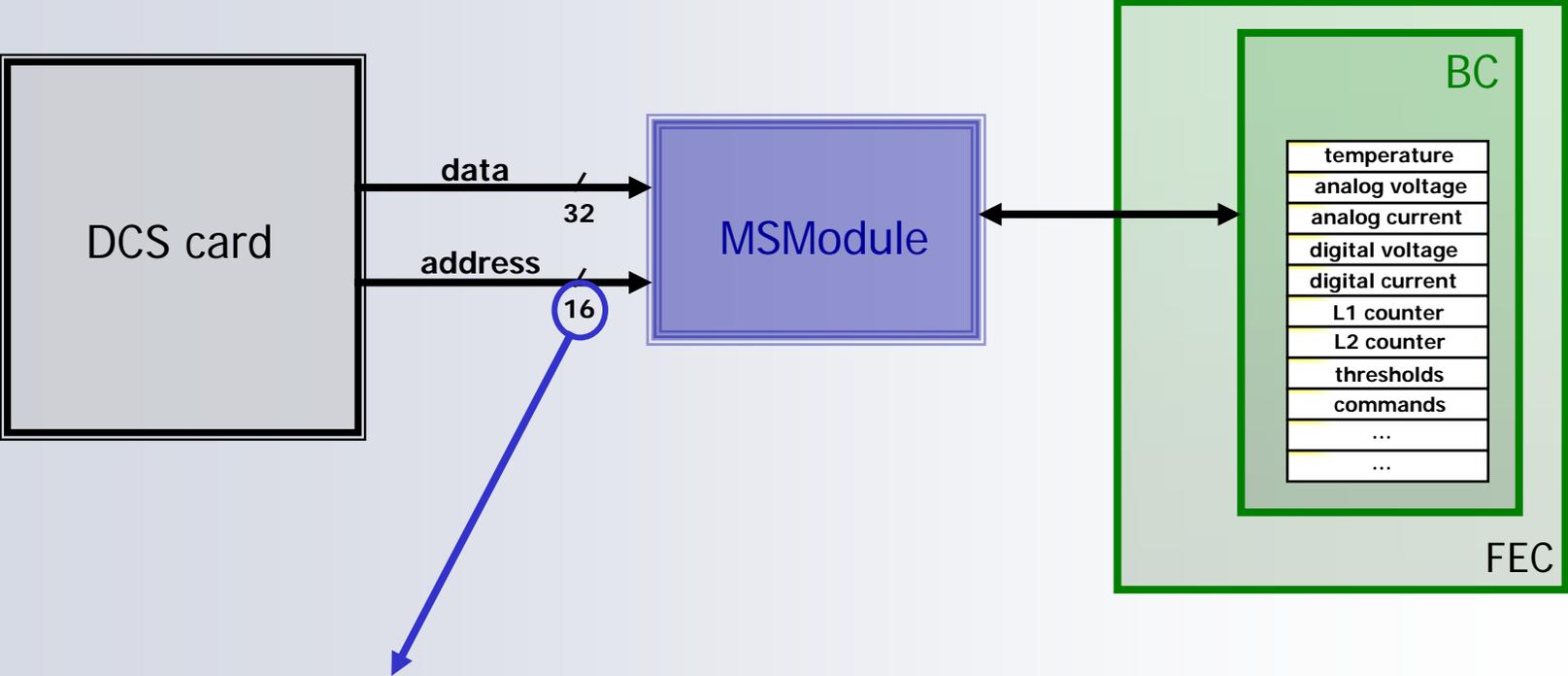


Monitoring 1/6

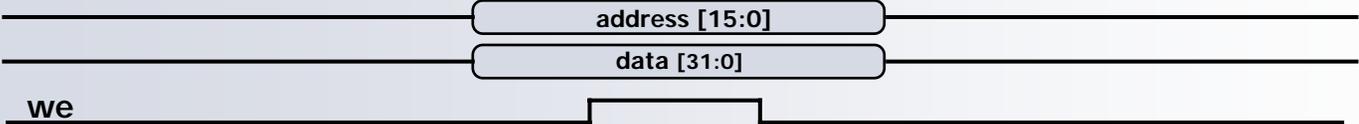
- The DCS sends commands to the MSModule to monitor the FECs
- The commands must contain:
 - FEC address (branch and hardware address)
 - parameter (BC register address)
 - Write or Read operation
- This specifications are done using the address and data buses:



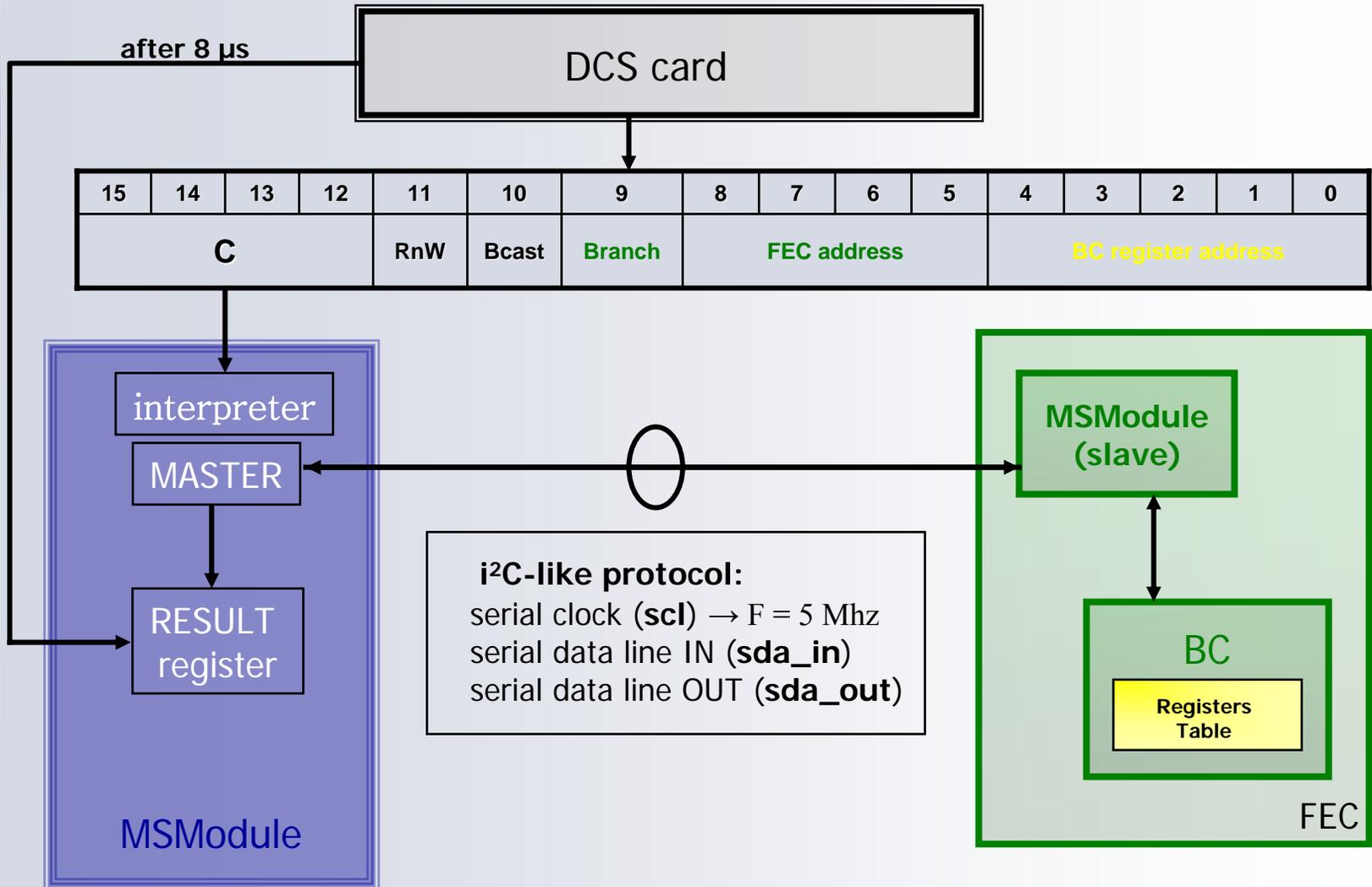
Monitoring 2/6



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				RnW	Bcast	Branch	FEC address				BC register address				



Monitoring 3/6



Monitoring 4/6

■ Parameters in the Board Controller (Read only):

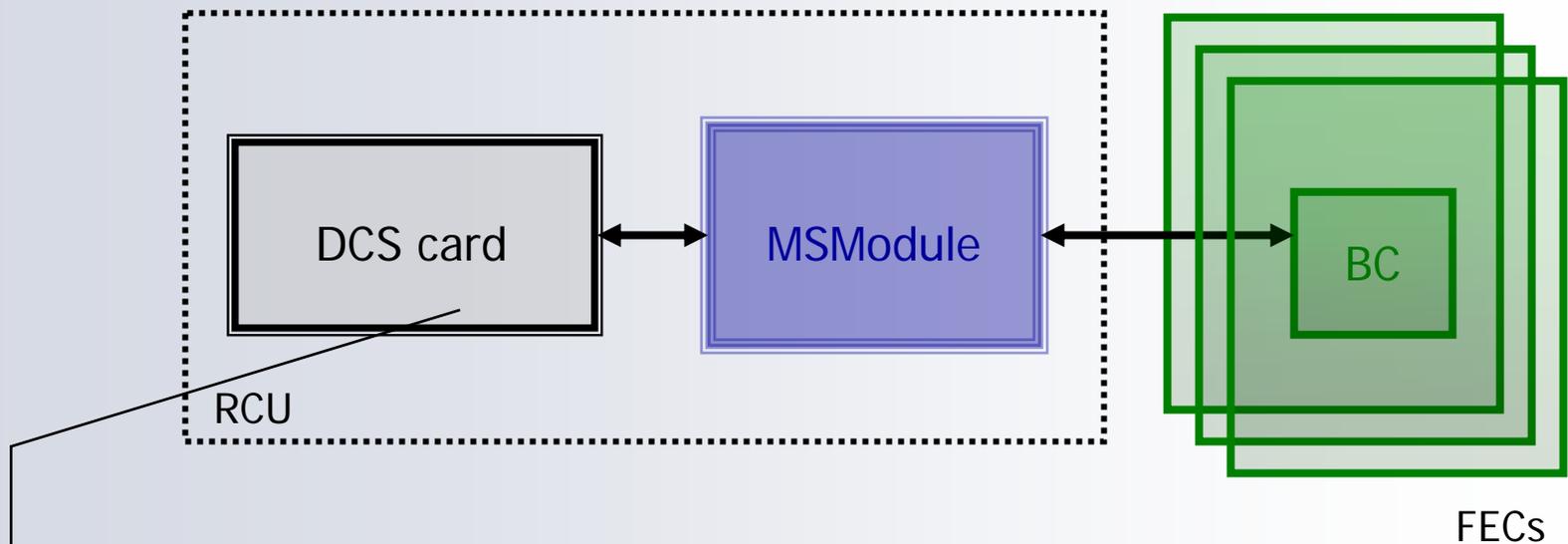
- Temperature
- Analog Voltage
- Analog Current
- Digital Voltage
- Digital Current
- L1 counter
- L2 counter
- Sampling clock counter
- Data strobe counter
- Status Registers

→ readout from a 5-channel ADC in the FEC

■ Commands (allow broadcast)

- Counters Latch
- Counters Clear
- Reset Status Register
- ALTRO reset
- BC reset
- Start Conversion of the monitor ADC

Monitoring 5/6



The DCS periodically monitors:

- Temperatures
- Voltages
- Currents
- Counters → Launch counters in the BCs in beacst mode:
 - L1 and L2 triggers
 - sampling clock
 - data strobe

Monitoring 6/6

Registers in the MSModule involved in the Monitoring process:

Front End Card Active List (FEC_AL): 32 bits

	28	27	26	25	24	23	22	21	20	19	18	17	16		11	10	9	8	7	6	5	4	3	2	1	0	
	BRANCH B														BRANCH A												
x	C	B	A	9	8	7	6	5	4	3	2	1	0	x	B	A	9	8	7	6	5	4	3	2	1	0	

Result Register (RESULT): 21 bits

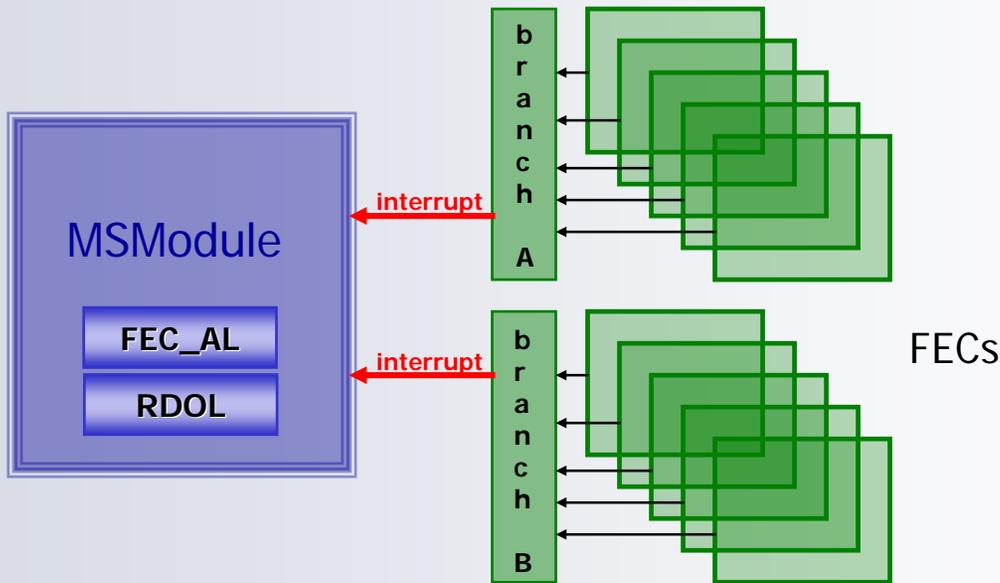
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEC address					BC register															

Error Register (ErrREG): 2 bits

1	0
Not acknowledge from the addressed FEC	Instruction to a not active FEC

Safety 1/4

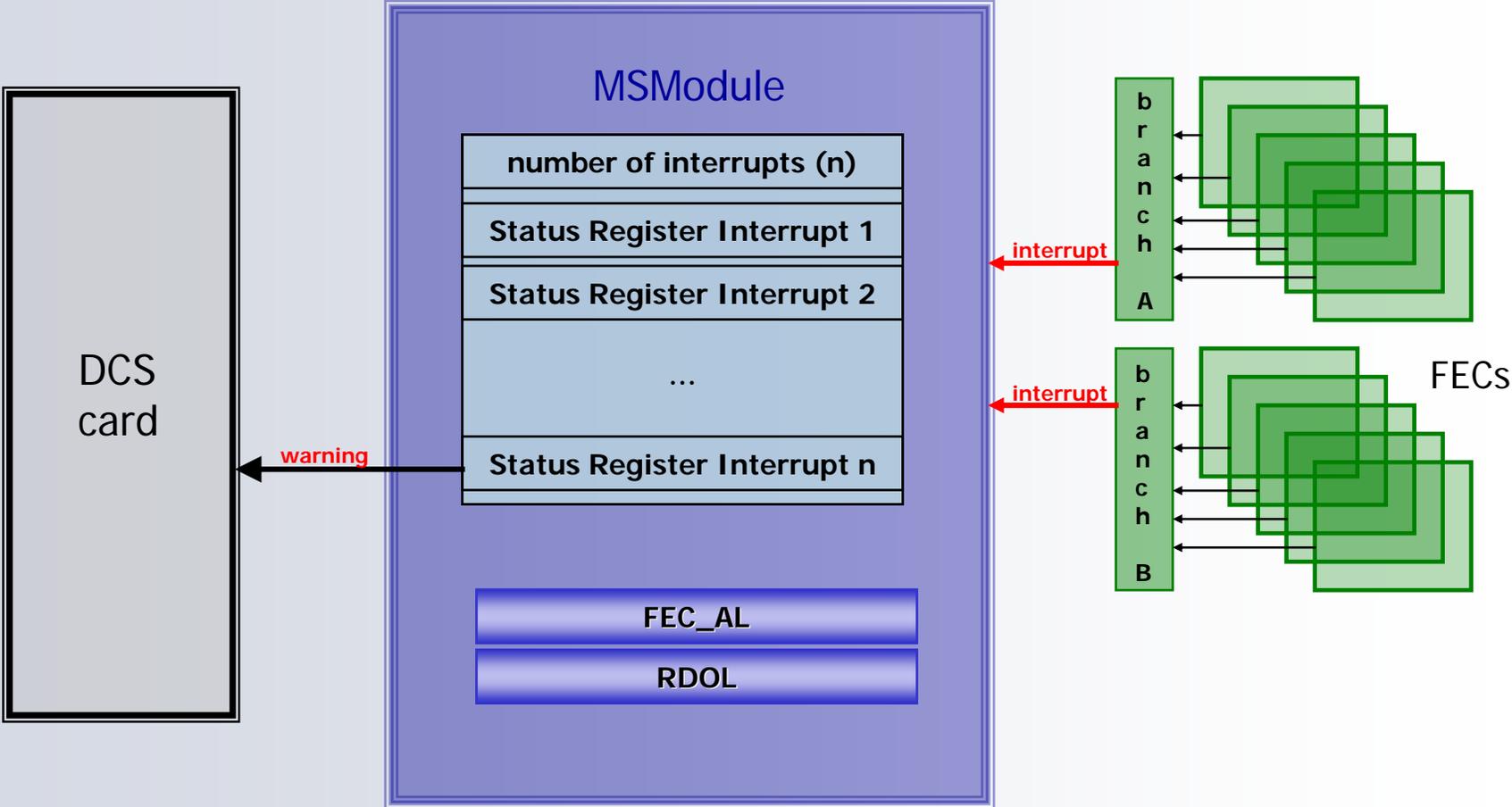
- When the MSModule receives an Interrupt it does not know which FEC asserted the signal
- It starts polling the active FECs (FEC_AL register) to identify the card and the error



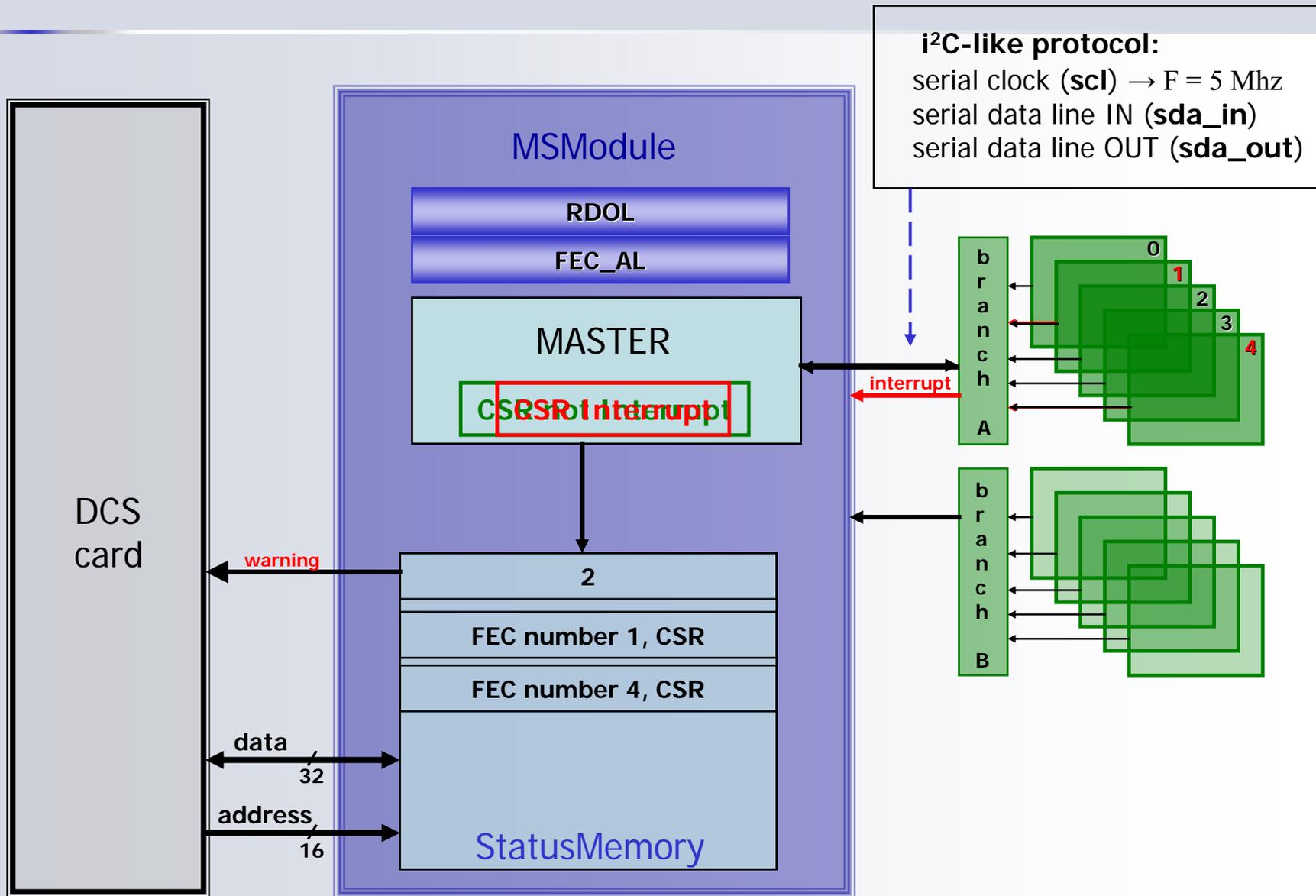
- The errors are classified in “hard” and “soft” error:
 - Hard error → the card is immediately switched off and removed from the FEC_AL
 - Soft error → the error is masked in the FEC and the card is removed from the Readout List
- The MSModule writes the StatusMemory to inform the DCS

Safety 2/4

Status Memory: 16 bits x 32 words



Safety 3/4



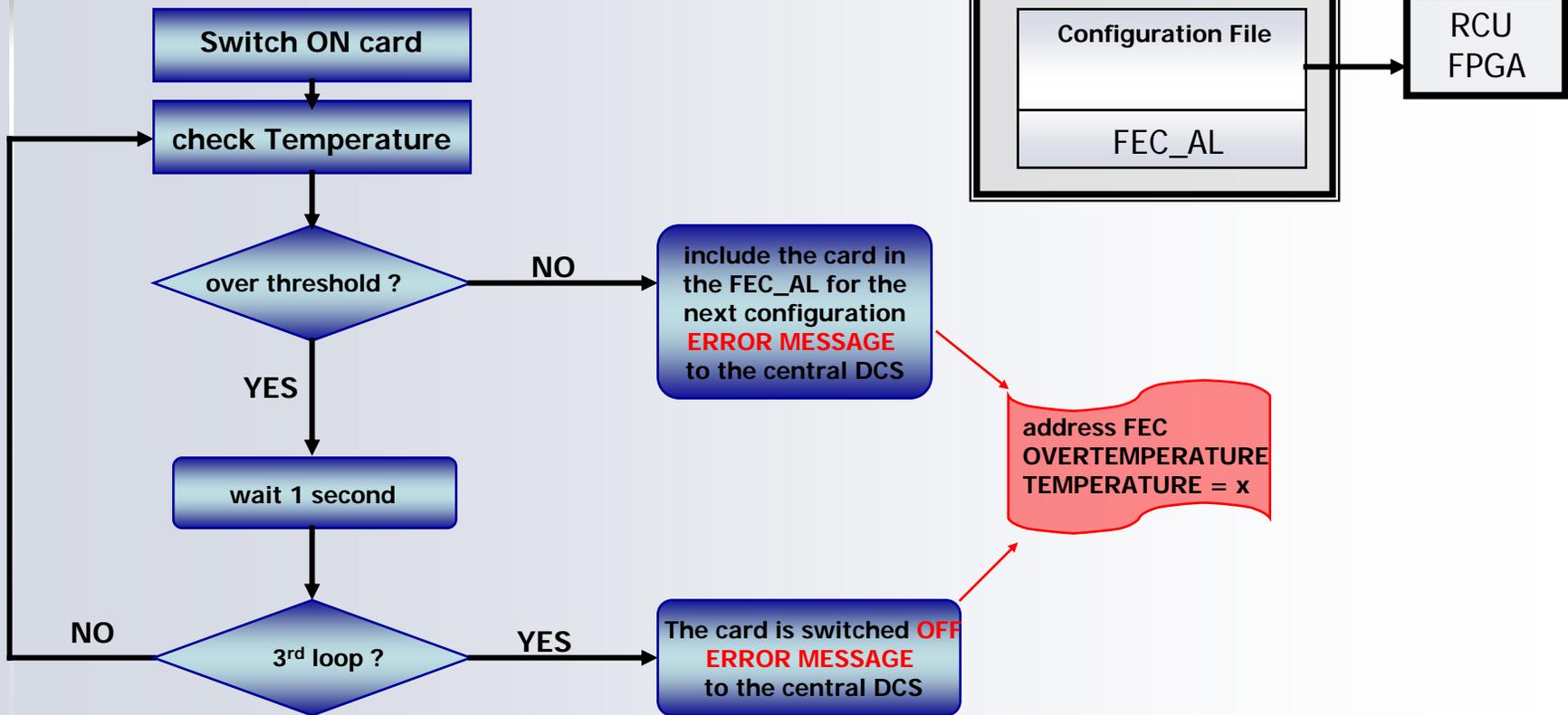
Safety 4/4

Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt source not Identified	branch	FEC address				Card ON/OFF	Hardware Interrupt	missing scilk	alps error	paps error	dc > th	dv < th	ac > th	av < th	temp > th
								BC Configuration Status Register							

Error Handling in the DCS card

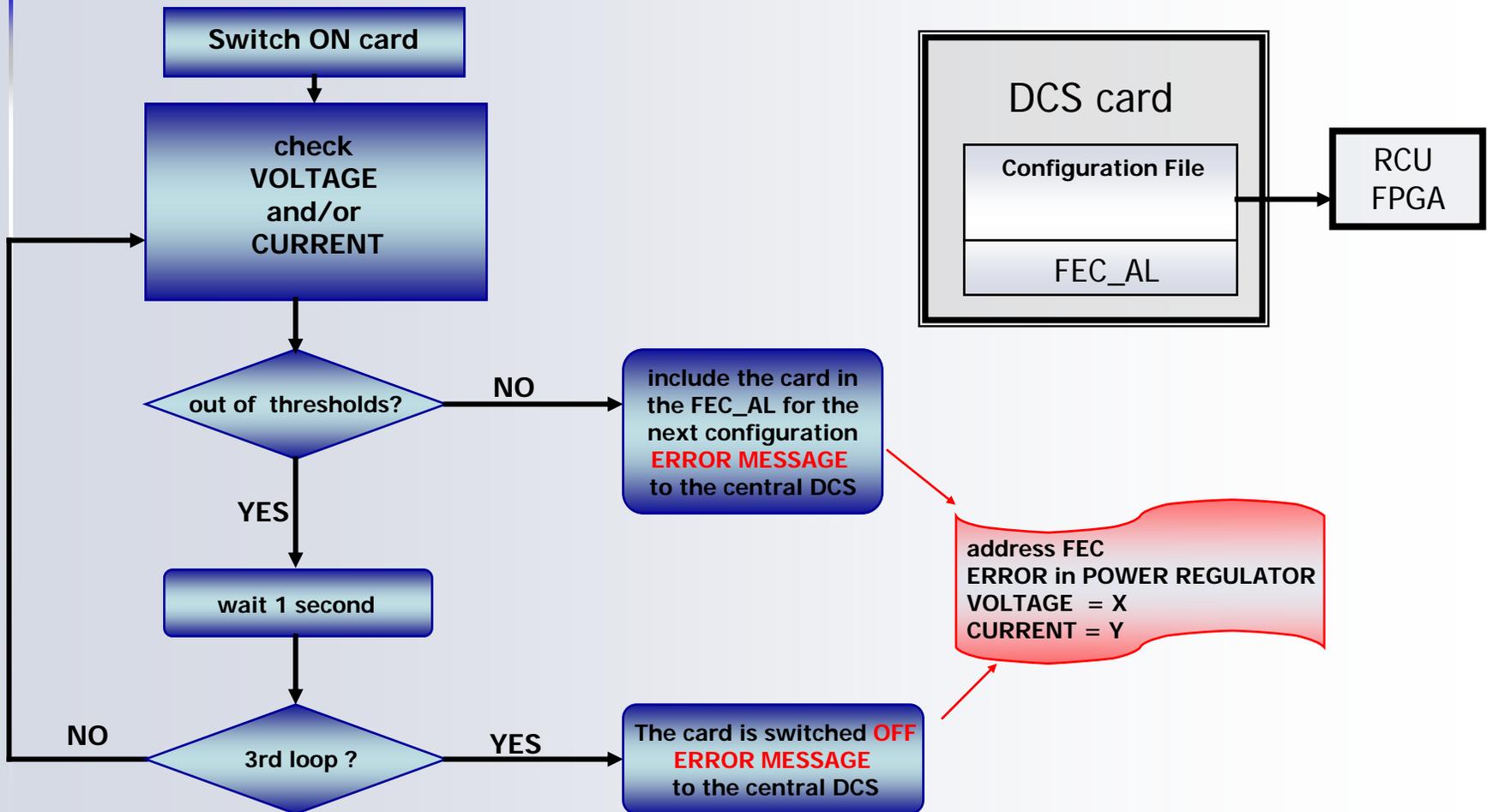
- When the “warningDCS” is asserted, the DCS should:
 - read the StatusMemory in the MSModule
 - run specific routines depending of the content:
 - OVER TEMPERATURE →The card was SWITCHED OFF



Error Handling in the DCS card

■ ERROR IN SOME OF THE POWER REGULATORS → The card was SWITCHED OFF

- Over CURRENT
- Under VOLTAGE



Present status

- Completed tested
 - All the functions of the BC:
 - Write/Read the configuration parameters
 - Read all the parameters of the board (temp, voltages, currents, counters ...)
 - Error flags
 - Interrupt assertion
 - The communication between the MSModule and the BC
 - The communication between the DCS card and the MSModule
 - The Error Handling in the MSModule

- Performance:
 - The Local Slow Control network runs at a clock frequency of 5 MHz.
 - The protocol requires the transmission of a large number of control words. A single 16-data bit transaction, e.g., requires 8 μ s.
 - When an interrupt occurs, the RCU starts polling the error/status register of all FECs of one branch. This action could require up to 100 μ s in the case of a readout partition with 13 FEC/branch.