Readout Control Unit – Mass production and Test

TPC Electronics Meeting – Bergen 7 April 2005

Outline :

- Organization aspect of the mass production:
  - Price Inquiry and Time Schedule
  - Components choice

- Production Quality Test :
  - PCB Electrical tests
  - Automated Visual Inspection
  - X-rays BGA inspection

- Manufacturing Approval

- Mass Test :
  - Electrical tests of the board (active components and connectors)
  - Functional test
  - Firmware and Software required

- Summary

RCU Mass Production – Price Inquiry

Scope of the Price Inquiry:

Supply of 260 RCU.

In a first step a 15 modules pre-series will be ordered.

This will be followed by the order to complete the full production

The specifications concern the production of RCU modules comprising :

- Purchase of some of the passive components (all Capacitors and Resistors)
- Manufacturing of the printed-circuit boards
- Component mounting (SMD and traditional)
- Final assembly
- Quality control

Purchase Options:

N1 – Rights to order up–to 20 additional modules at the same price/conditions of the 260

N2 – Use of standard FR4 instead of halogen-free laminates in the PCB manufacturing

N3 – X-ray inspection of the 100% (instead of 10%) of the BGA assemblies

RCU Mass Production Price Inquiry – Cover Letter

ORGANISATION EUROPÉENNE POUR LA RECHERCHE NUCLÉAIRE
EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
Laboratoire Européen pour la Physique des Particules
European Laboratory for Particle Physics

GENEVE, SUISSE
GENEVA, SWITZERLAND

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GENEVE 23
Switzerland

Telex/Telex: 419000 CER CH
Téléfax/fax: + 41 22 767 6555
Téléphone/Telephone: + 41 22 767 6111

Your reference:

Our reference:

Geneva, 17 March 2005

Re: Price Enquiry - **DO-22078/PH/ALICE**

ALICE TPC READOUT CONTROL UNIT

Dear Sir/Madam,

CERN, which is located at Meyrin/Geneva, invites offers for the above mentioned supply. All the documents listed in and annexed to the present letter form an integral part of this price enquiry.

The following conditions will apply to this price enquiry.

1 - Setting out of offers

Offers cannot be considered unless they are submitted on the attached price enquiry form.

2 - Despatch of offers

The offers and all accompanying documents must be sent in duplicate to the following address:

Procurement Service
Att'n: Laszlo Abel
CERN
CH-1211 GENEVA 23

The offer is to be sent to the above address not later than:

15 April 2005

The postmark will be accepted as proof of date of posting. The envelope shall clearly state the name of the company and the reference of the here above mentioned price enquiry.

In case firms consider the establishment of a consortium in order to reply by a joint offer to the present price enquiry, the following conditions shall apply:

- The consortium must submit its offer via one firm who shall be nominated by the other firms participating in the consortium as their sole representative with the power to act on their behalf in all matters concerning the purchase order.

- The firm acting as a representative shall give evidence of its compliance with the above provision by submitting a power of attorney signed by duly authorized signatories of each firm.

- The firms participating in the consortium shall clearly state the distribution of activities among them concerning the performance of the purchase order, and shall adhere to the stated distribution during the validity of the said purchase order.

- The firms participating in the consortium shall be jointly and severally liable for the performance of the purchase order.

We are at your disposal for any further information that you may consider necessary and would ask you to contact, preferably by telefax.

For commercial or administrative matters:

Laszlo ABEL
Tel: (+41) 22 76 79561
Fax: (+41) 22 767 7530
Laszlo.Abel@cern.ch

For technical matters:

Roberto CAMPAGNOLO
Tel: (+41) 22 76 71945
Fax: (+41) 22 767 83 10
Roberto.Campagnolo@cern.ch

or in case of absence:

Luciano MUSA
Tel: (+41) 22 76 76261
Fax: (+41) 22 767 83 10
Luciano.Musa@cern.ch

Yours faithfully,

Laszlo Abel
Purchasing Service

Enclosures:
Tender Form DO-22078/PH/ALICE
Technical Specification DO-22078/PH/ALICE and annexes
Safety Instruction TIS IS41
General Conditions of CERN Contracts CERN FC/1814-II

… sent to a list of firms

Names given by us:

1. NOTE Xperi AB
2. FINMEK S.p.a.
3. Ste COFIDUR sa (Techci)
4. CAEN S.p.a.
5. BARCO Electronic Manufacturing

Names given by (Finnish-) Industrial Liaison Office:

6. JUTRON - OULU
7. SIRICO Electronics - PIETARSAARI
8. SCANPIIRI OY - SALO
9. EXTRABIT OY -OULU

Time Schedule for the RCU Mass Production

Contractual Schedule:

PHASE	DESCRIPTION	LATEST DELIVERY DATES
1	CERN Delivery of the components specified in the Bill of Material, with the exception of all Capacitors and all Resistors (to be purchased by the contractor).	2 weeks after notification of the order
2	Pre-series of 15 RCU modules delivered at CERN.	4 weeks after reception of the components delivered by CERN
3	Notification of the Approval Certificate by CERN (see 2.3 – Manufacture Approval)	2 weeks after delivery of pre-series at CERN
4	Delivery to CERN of the series production of modules to complete the order	8 weeks after the reception of the Approval Certificate

Project deadlines:

Price Inquiry closing date: 15 of April

RCU Design Review : 20 April
Contract award : 2nd half of April

Mass Production Start: beginning of May
Pre-series @ CERN: end of May/ beginning of June
Full production delivery: end of July

Issues in the choice of some components

Since last January TPC Electronics meeting :

- ✓ Xilinx FPGA size (vs. required resources and price)
- ✓ RCU to DCS connectors (2x 70 pins 1.27mm. pitch board stackers)
- ➢ JTAG connectors type

Xilinx FPGA size choice

Device utilization summary (for the current design):

		Device: **2vp4**ff672-5		**2vp7**ff672-5	
Number of Slices:	2300	3008	76%	4928	46%
Number of Slice Flip Flops:	2746	6016	45%	9856	27%
Number of 4 input LUTs:	4145	6016	68%	9856	42%
Number of bonded IOBs:	235	348	67%	396	59%
Number of BRAMs:	11	28	39%	44	25%
Number of GCLKs:	9	16	56%	16	56%
Number of DCMs:	2	4	50%	4	50%
Config (Mbits):		3.01		4.49	

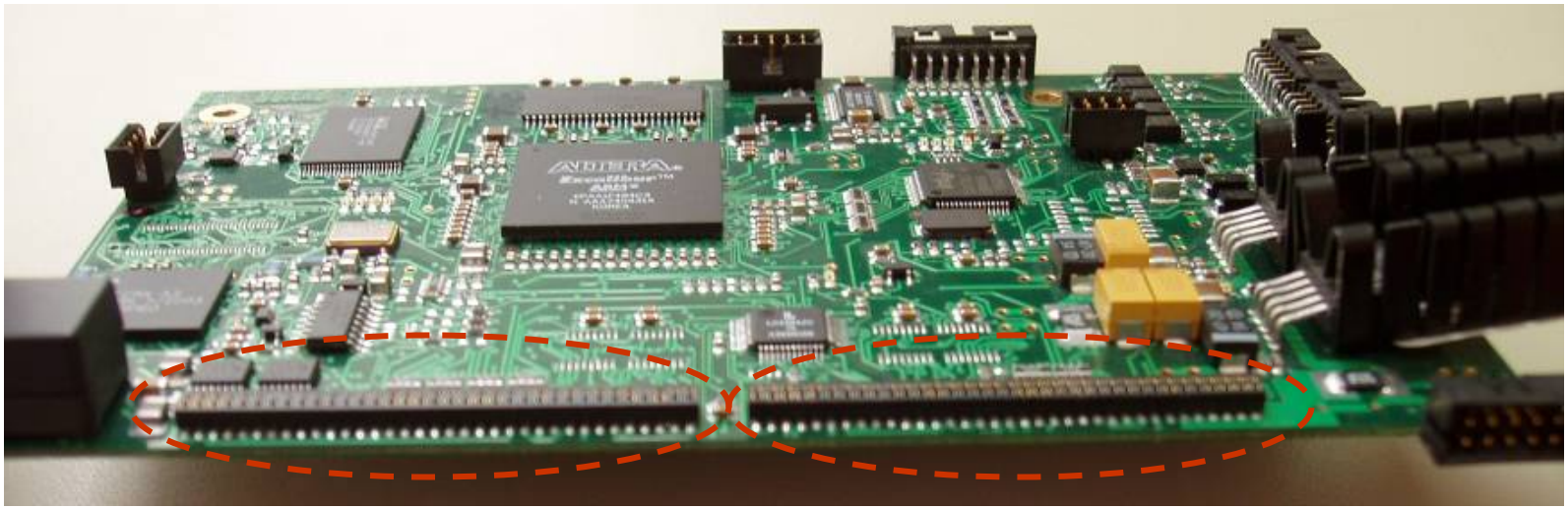
(RCU – Flash memory size : 64 Mbit)

‘Market survey’ price range:

XC2VP4 : 95 to 129 USD
XC2VP7 : 119 to 186 USD
(+ 24 $: < 3 % compared to the final price of the board)

→ Selected device : XC2VP7-5FF672C

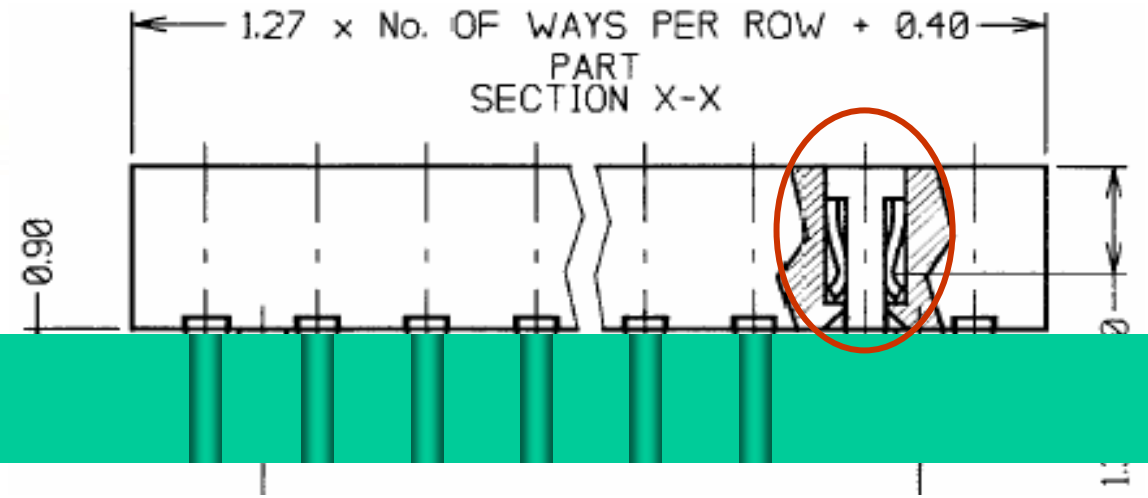
DCS connectors



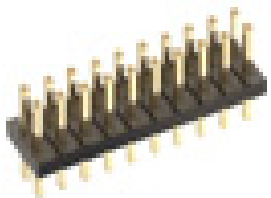
Harwin M50-315 1.27mm Pitch SMS,
with ‘pass-holes’ PCB (back-insertion)

RCU – DCS board stacker – Harwin solution

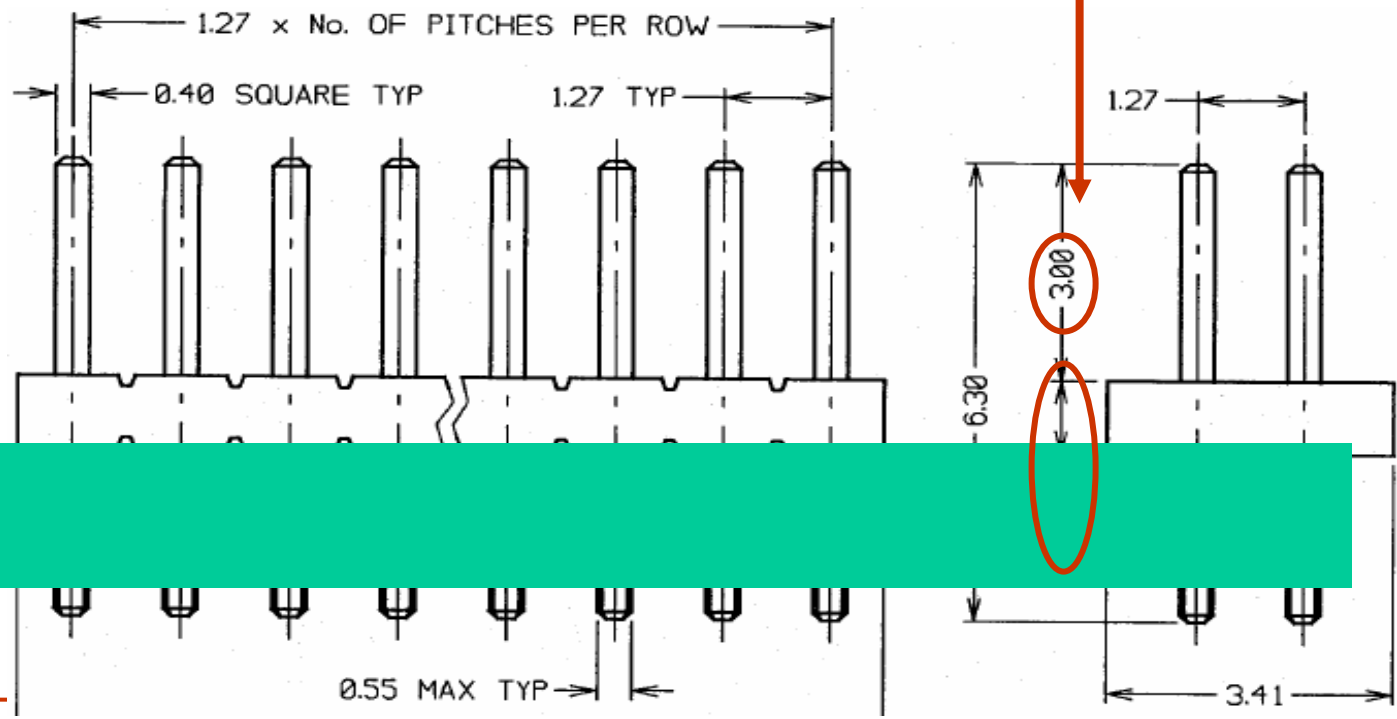
M50-315



DCS PCB
1.2 mm.

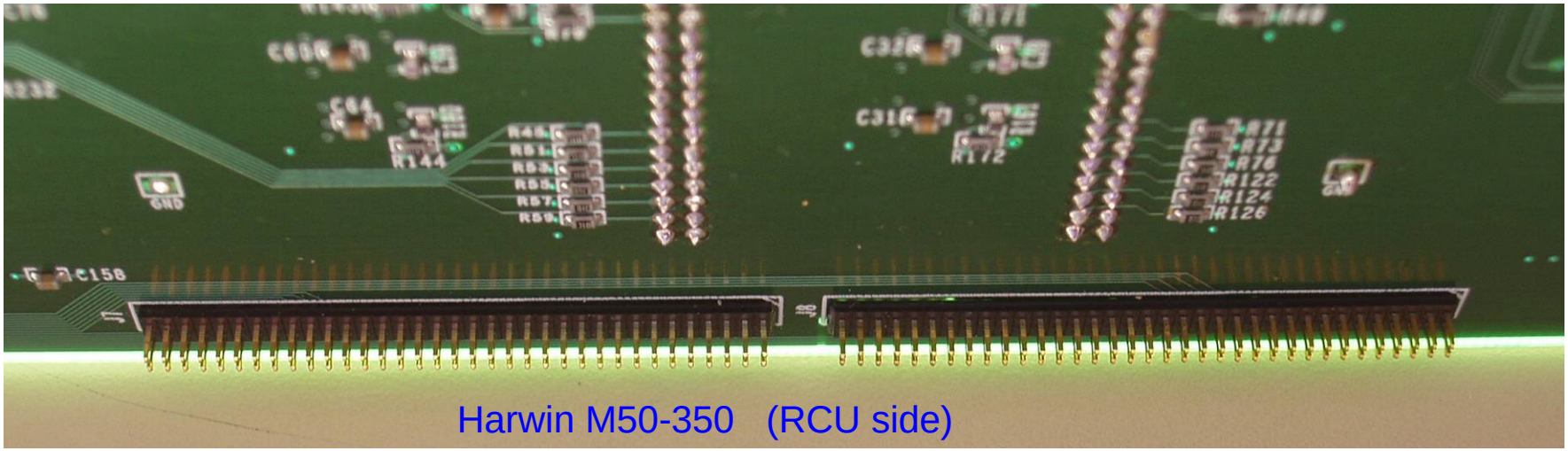


M50-350 (360SMS)

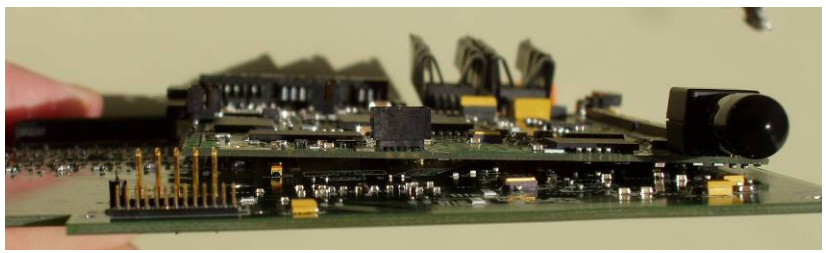


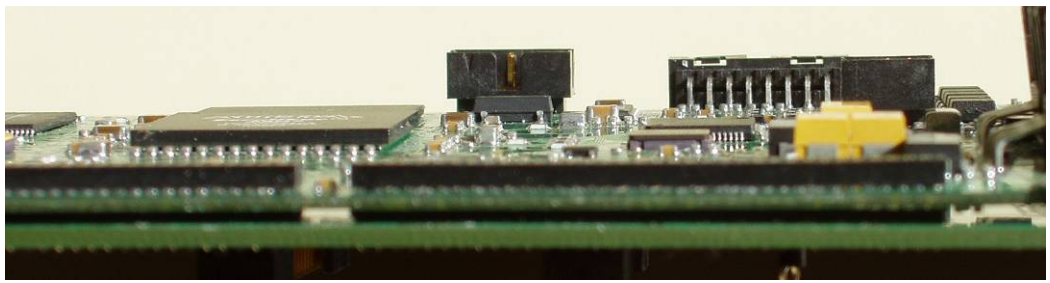
RCU PCB
1.8 mm.

RCU – DCS : Harwin connectors assembly



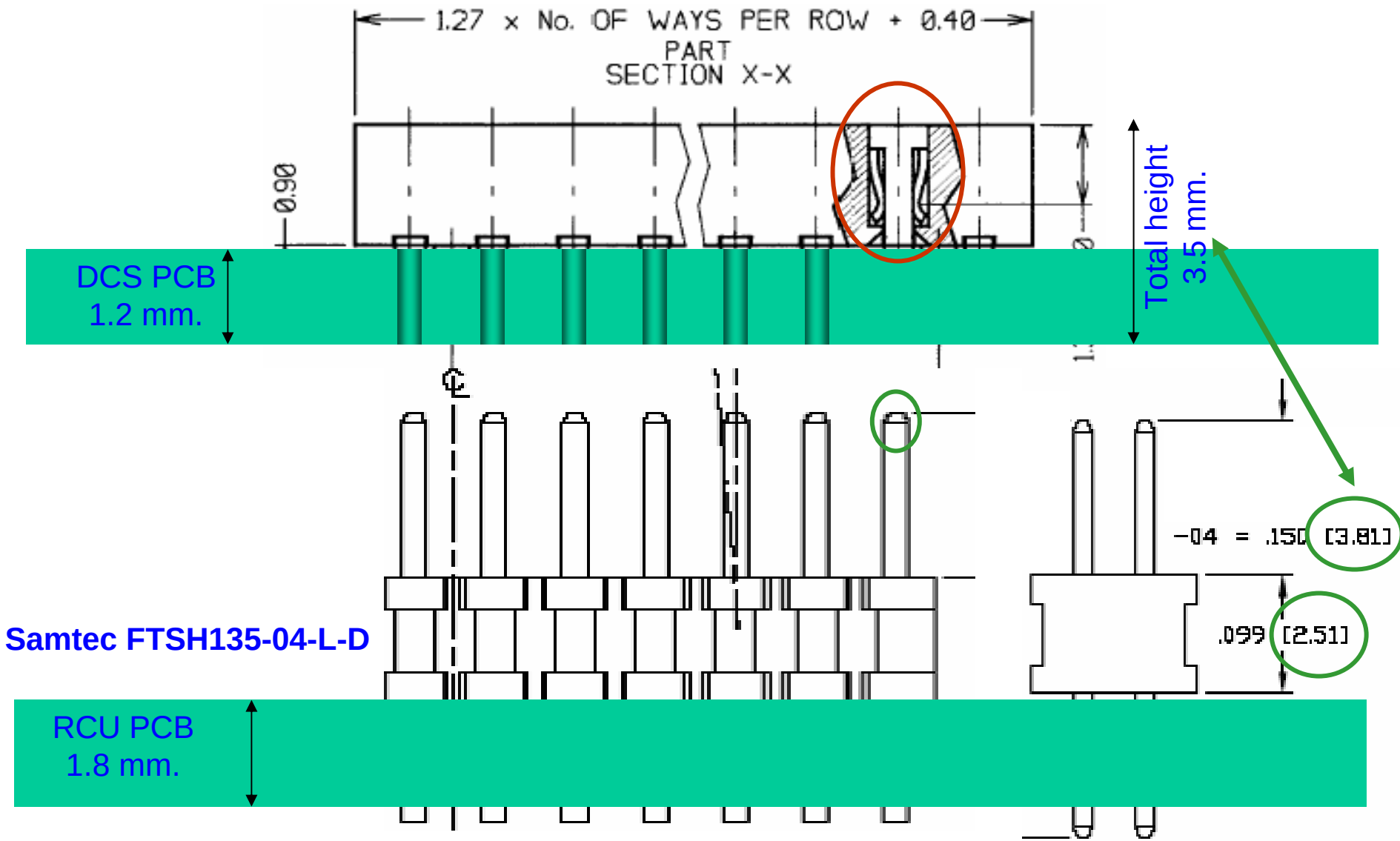
Harwin M50-350 (RCU side)





DCS plugged to the RCU with the Harwin connectors both side
(card tilting , short circuit risk , unplugging of the connectors)

RCU – DCS board stacker – Harwin / Samtec mixed

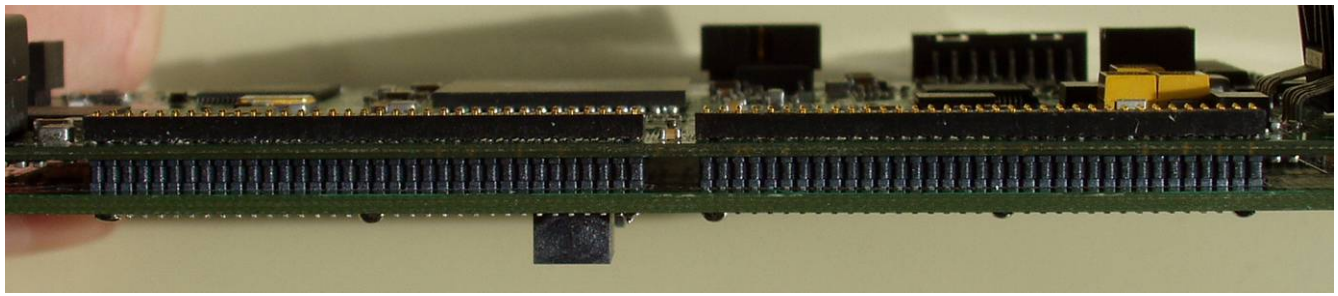


RCU – DCS : Harwin and Samtec assembly

Harwin M50-350

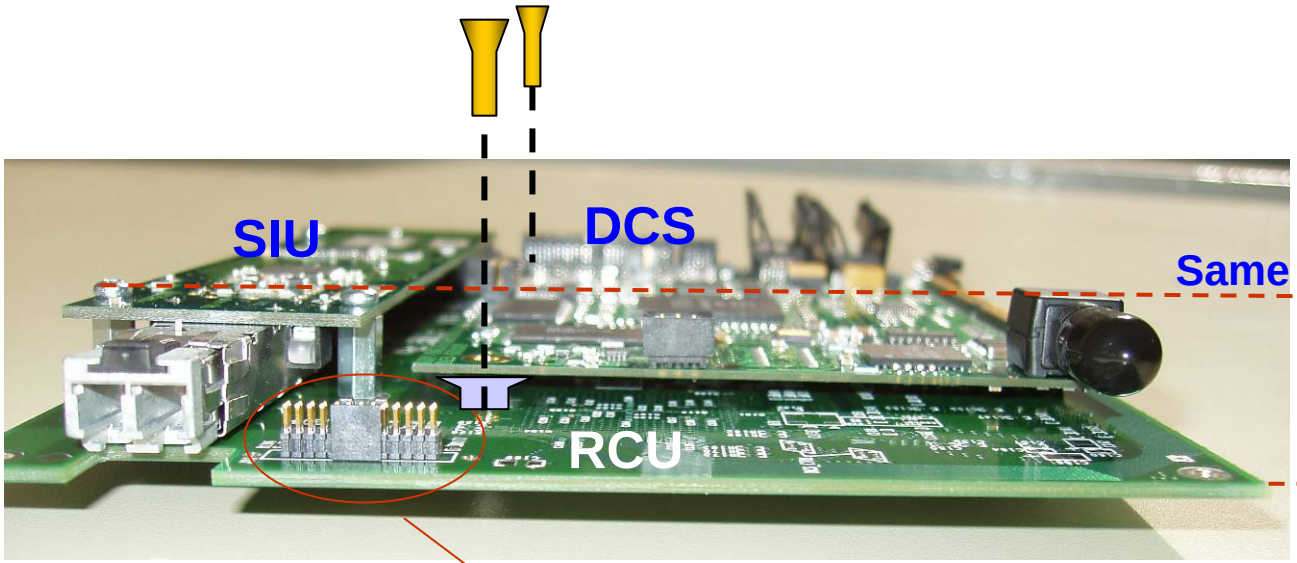
Samtec FTSH –04

Boards stacking :
2.5 mm distance +
improved contact surface



Mechanical aspects

SIU – RCU – DCS Final assembly



Same mezzanines assembly height

13 mm

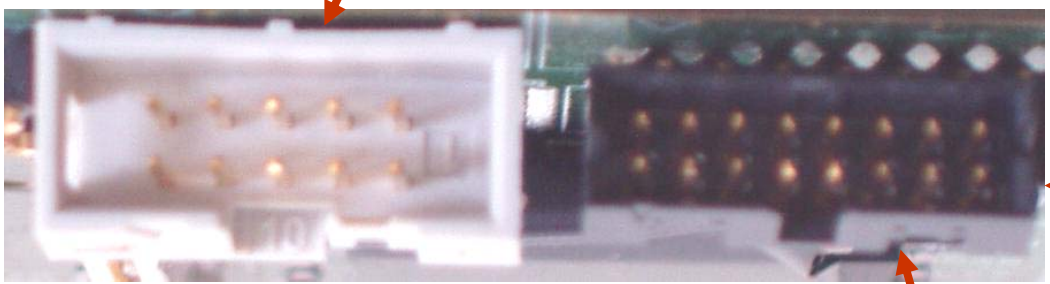
Detail of the ACTEL-Jtag connector
(standard set by the Actel Flash-Pro connection cable)

Question : To fix the DCS card to the RCU PCB,
can we use whatever type of spacers and screws ? (Nylon, Bronze, Steel, Copper…)

XILINX - JTAG connector

Xilinx Jtag Programmer

Actual Jtag connector 2x 5 pins 2.54 mm pitch
(needs adaptor and additional Vref connection)



MOLEX 87831-1420 :
14 pins 2mm. Pitch shrouded header

Mass Production Tests

Contractual Quality controls to be done by the board manufacturer:

- Electrical test of the PCB before components assembly
- Automatic Optical Inspection after component assembly
- Specific X-ray inspection for the Ball Grid Array assemblies
  (Xilinx FPGA in FF672 – 1mm fine pitch flip-chip BGA package)

Tests to be done by us:

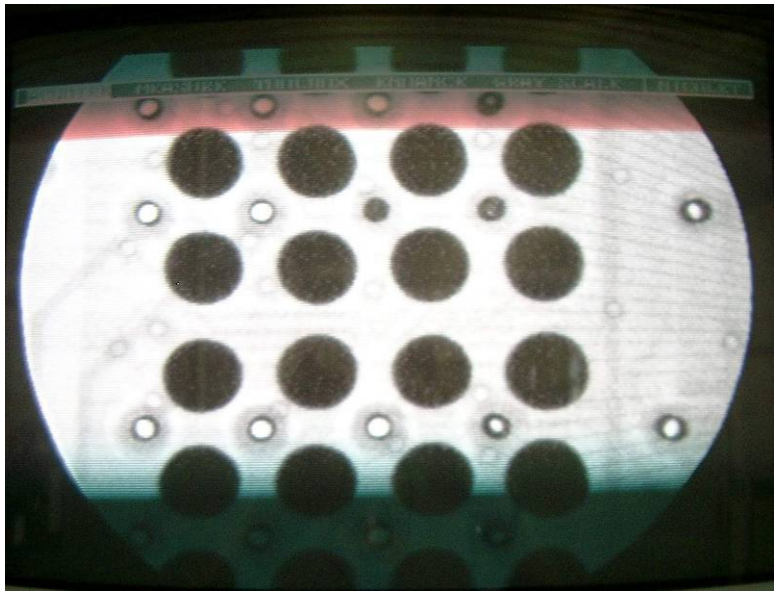
- Pre-series Manufacture Approval
- Burning Test
- Board Electrical tests
- Functional Tests

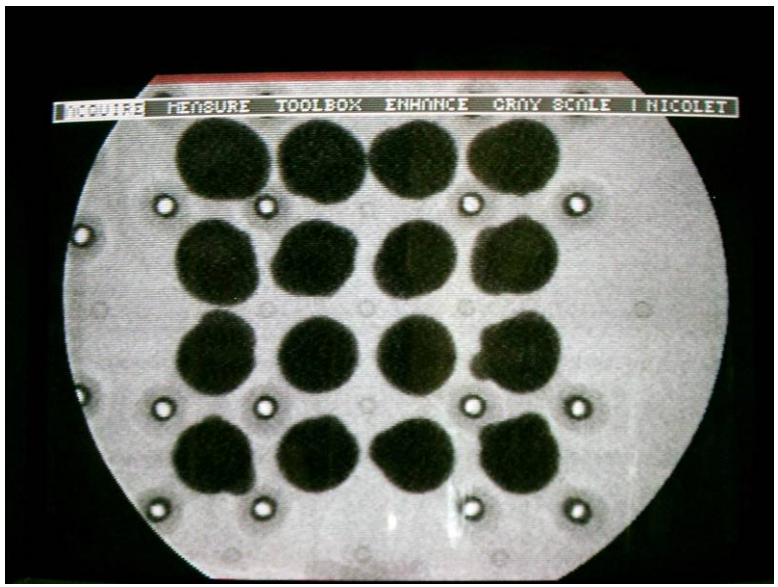
Manufacturers typical assembly and inspection implant

- Screen-printers
- Pick &Place
- Reflow
- Optical inspection

Flying probe testers , Open-checker
(Takaya – Fixtureless In-Circuit Test, on demand/payment….)

Examples of X-ray inspection





Laser technology for BGA re-working

Pre-series manufacture approval 1/2

Contractually, after the reception of the production pre-series of 15 RCU,
we have 2 weeks (maximum) to notify to the manufacturer one of the following possibilities:

- Approval Certificate if the modules fulfills all the specifications
- Ask for some specific process/assembly re-tunings
- Cancel the whole contract (and then re-start the flow with another company)

It is then extremely important in the short time being able to characterize the 15 boards
knowing that, once the Approval Certificate will be issued, the full production
has to be done with the same technology and tooling used for the pre-series.

Pre-series manufacture approval 2/2

In addition to the visual inspection of the manufactured boards and a Burning Test, a set of electrical/functional tests must be performed.

Concerning the PCB manufacturing, the correct use of different laminates with the proper dielectric compensation (for the impedance controlled lines) can be verified analyzing the signal integrity of the most critical paths (with the same technique as for the prototype characterization).

The component verification (in particular concerning the passive components supplied by the manufacturer) and the overall card assembly shall be certificated with the same test set-up planned for the mass production test (to be ready then by end of May).

Board Electrical Tests

After the verification of the current absorption with the board ‘stand-alone’ without and with the test firmware uploaded, the goal of the electrical test to be executed on each board is:

To verify the signal distribution at the pin level of the connectors
(and, implicitly, the correct assembly of a number of components sitting on the board like the GTL transceivers, Clock drivers and most of the FPGAs connections) .

To validate the interconnectivity of all the components that are not verified with the first part of the test (i.e. the remaining FPGAs and memory connections)

Verification of the signal distribution on the RCU connectors

The connectivity of the RCU is characterized by :

1- The main Power supply connector/distribution and the additional Ground socket
(proven with direct measurement of the regulated voltages from the LDOs)

2- the number of test points and external signals injection pins distributed on the board
(to verify the integrity of clock and trigger signals, to stimulate different test conditions
and to access dedicated test signals both at the PCB-board and at the FPGA-internal levels)

3- the two JTAG connectors for the direct programming of the Actel and Xilinx devices
(implicitly verified during the upload of the firmwares into the 2 FPGAs)

4- the two-branches backplane connectors
(test protocol completed)

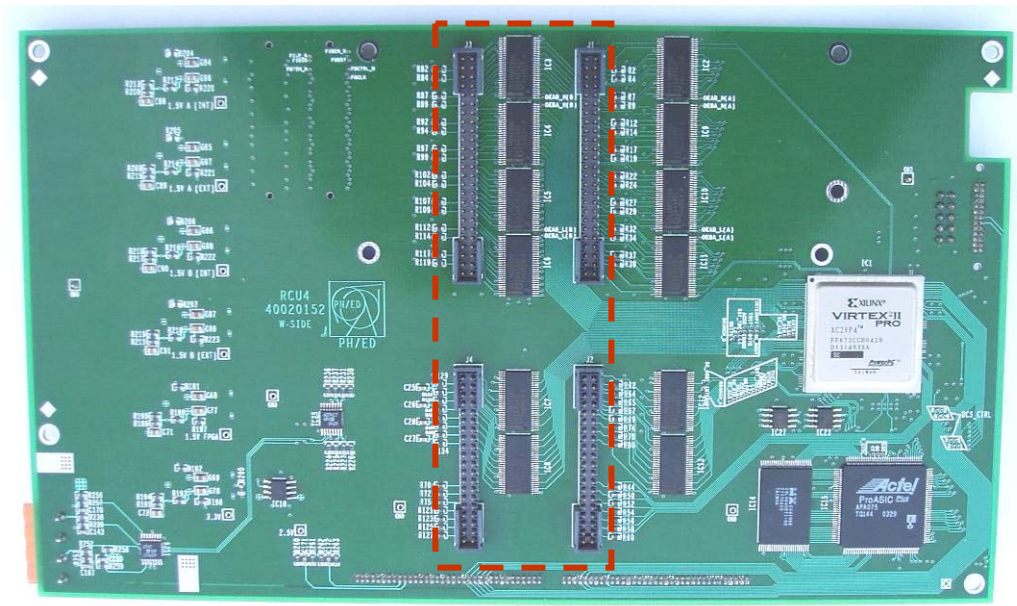
5- the SIU-DAQ connectors
(details of the test protocol need to be defined with DAQ designers)

6- The DCS connectors
(test of DCS connectors requires the development of a specific firmware for the DCS board)

Backplane connector signals

Summary :

2 Branches of Altro readout Bus
each characterized by 2 PCB backplanes distributing
40 data lines,
  9 Protocol Control Lines
  2 Clocks (1 single ended and 1 differential)
  4 Slow Control signals (3 protocol +1 interrupt)
13 Card enable lines (+5 Vtt termination pins)



Readout Backplane signals (per branch)

SAMTEC MMS-125-01-L-DV - on backplane		
PIN	FNCT	Termination required-technology
1	GND	
2	D39	GTL
3	D38	GTL
...	...	
46	D2	GTL
47	D1	GTL
48	D0	GTL
49	VTT	(to the termination on backplane)
50	VTT	(to the termination on backplane)

SAMTEC MMS-120-01-L-DV - on backplane		
PIN	FNCT	Termination required-technology
1	GND	
2	ERROR_GT	GTL
3	DSTB_GT	GTL
4	ACKN_GT	GTL
5	TRSF_GT	GTL
6	GND	
7	L2_GT	GTL
8	L1_GT	GTL
9	WRITE_GT	GTL
10	CSTB_GT	GTL
11	RST_GT	GTL
12	GND	
13	RDO_ CLK	GTL
14	INTERRUPT	GTL
15	SC_DIN	GTL
16	SC_DOUT	GTL
17	SC_CLK	GTL
18	GND	
19	VTT	(to the termination on backplane)
20	VTT	(to the termination on backplane)
21	VTT	(to the termination on backplane)
22	GND	
23	SCLK_DN	On backplane only - LVPECL
24	GND	
25	SCLK_DP	On backplane only - LVPECL
26	GND	
27	PWR SW-1	
...	...	
38	PWR SW-12	
39	PWR SW-13	
40	GND	

Test of the Backplane connector signals

Solution: Dedicated RCU ‘Altro-protocol interface’ and Board Controller firmware.

Debugging principle:

- Write (into the BC) and read back test patterns to verify connectivity, stuck lines and short circuit between adjacent paths.
- Verification of the card address register in function of the card switch.
- Direct measurement of the VTT and of the Clocks (and triggers) signal integrity on the bus

Test protocol interface (and result): accessing, via the DDL interface, dedicated RCU registers (Xilinx FPGA)

Status: completely defined and in the implementation phase

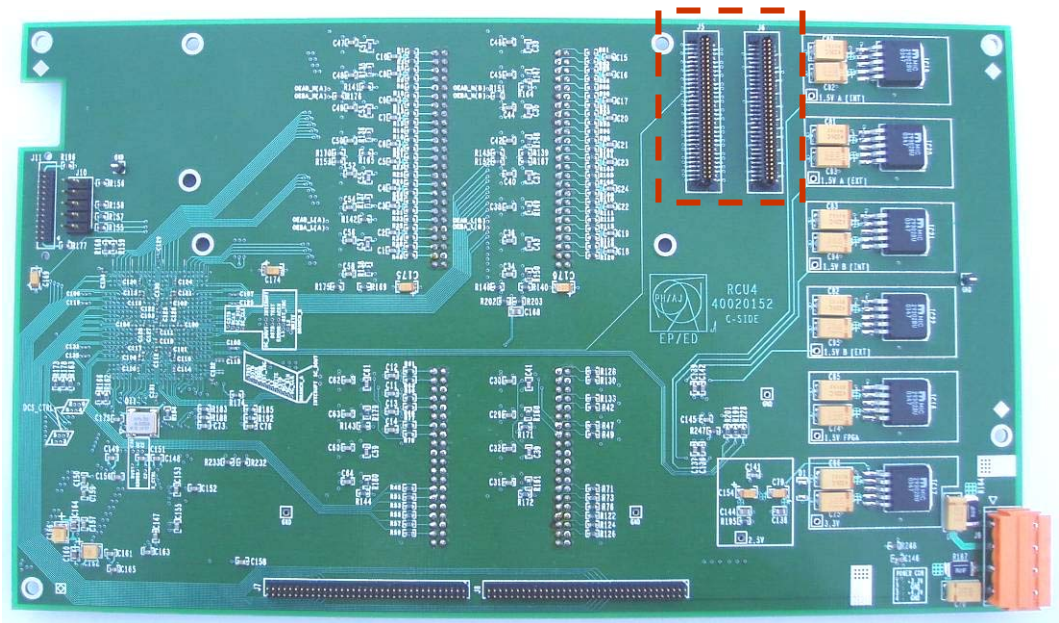
SIU connector signals

Condition:

2 mezzanine Surface Mounted Connectors
All the signals have Test Points (vias) on RCU PCB.

The 1st connector brings all the SIU-RCU interface protocol signals (32 data, 1 Clock and 6 control lines) and the regulate 3.3V power supply (on a number of Pins).

The 2nd connector replicates the power supply connections and makes available the SIU JTAG TAP port (not used).



Pin-out of the 2 SIU-CMC connectors

CMC SIU (P11 connector)				CMC SIU (P12 connector)			
1	FIBEN_N	-12V	2	1	+12V (1)	TAP_TMS	2
3	GND	FILF_N	4	3	TAP_TDI	TAP_TDO	4
5	FOBSY_N	FIDIR	6	5	TAP_TCK	GND	6
7	BUSMODE1#	+5V	8	7	GND	TAP_TRST	8
9	FBCTRL_N	FBTEN_N	10	9	-	-	10
11	GND	FBD0	12	11	BUSMODE2#	+3V	12
13	FOCLK	GND	14	13	-	BUSMODE3#	14
15	GND	FBD1	16	15	+3.3V	BUSMODE4#	16
17	FBD2	+5V	18	17	-	GND	18
19	V(I/O) (+3.3V)	FBD3	20	19	-	-	20
21	FBD4	FBD5	22	21	GND	-	22
23	FBD6	GND	24	23	-	+3.3V	24
25	GND	FBD7	26	25	-	-	26
27	FBD8	FBD9	28	27	+3.3V	-	28
29	FBD10	+5V	30	29	-	GND	30
31	V(I/O) (+3.3V)	FBD11	32	31	-	-	32
33	FBD12	GND	34	33	GND	-	34
35	GND	FBD13	36	35	-	+3.3V	36
37	FBD14	+5V	38	37	GND	-	38
39	GND	FBD15	40	39	-	GND	40
41	FBD16	FBD17	42	41	+3.3V	-	42
43	FBD18	GND	44	43	-	GND	44
45	V(I/O) (+3.3V)	FBD19	46	45	-	-	46
47	FBD20	FBD21	48	47	GND	-	48
49	FBD22	+5V	50	49	-	+3.3V	50
51	GND	FBD23	52	51	-	-	52
53	FBD24	FBD25	54	53	+3.3V	-	54
55	FBD26	GND	56	55	-	GND	56
57	V(I/O) (+3.3V)	FBD27	58	57	-	-	58
59	FBD28	FBD29	60	59	GND	-	60
61	FBD30	+5V	62	61	-	+3.3V	62
63	GND	FBD31	64	63	GND	-	64

Test of SIU connector signals

Testing method:

- Measurement of the regulated voltage (3.3V on all dedicated RCU pins) before plugging the SIU.

- (Verification of the Clock signal integrity on foCLK).

- Running already developed 'check-ddl' routines helps in a first DDL system verification.

→The possibility to force the status of some SIU control lines is required to complete the characterization

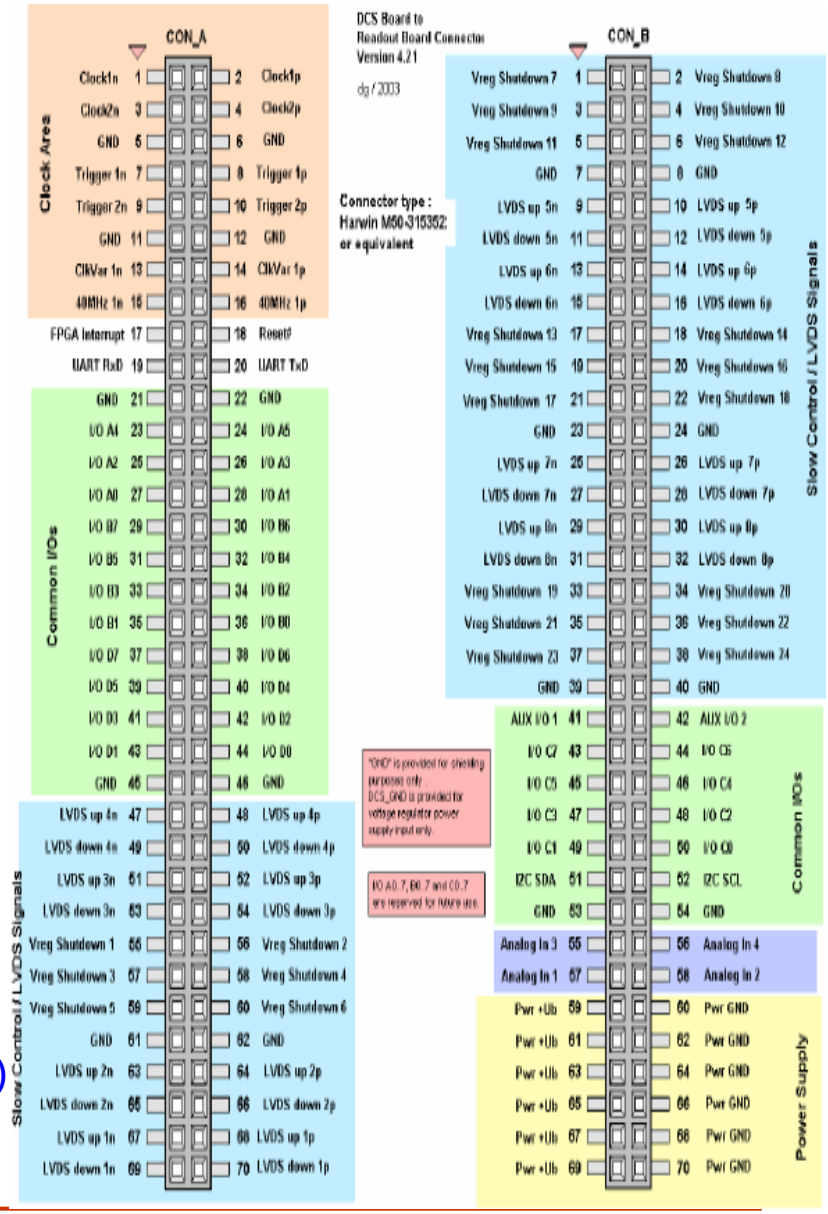
(Note that the use of the DDL link for the debugging of the Altro readout Backplane represents an additional SIU interface test)

Request to DAQ designers: To define the way to pre-set signals that in the laboratory set-up conditions would be never asserted (i.e. Link Full)

DCS connector signals

RCU-DCS connectors Signals:

- Differential signals (2xClock + 2xTrigger)
- 2 RCU-Sense Voltages to the DCS ADC (ConB pins 20,18)
- DCS FPGA Interrupt / Reset / UART Rxd and TxD (**Q:** do we really need them ?)
- 7 RCU regulators enable lines (VregSH 6..0: ConB pins 19,17,5..1)
- 32 Bi-directional Data Lines (D31..0: ConA pins 32..25, ConB pins 54..47 , 44..29)
- 16 DCS→RCU address lines (A15..0: ConB pins 16..9 , ConA pins 70..63)
- 8 Control lines (WarningDCS, CSTB, R/W, ACKN + 4under definition) (DCS_CTRL7..0: ConB pins 50..43)



Test of the RCU - DCS connectivity 1/3

Direct measurement :

- Differential signals (Clocks and Triggers) :
  connecting the TTC-fiber to the DCS, then verifying the presence of the expected signals
  (Checking the RCU-PCB Test Points for the 2 differential lines of each signal)

- 2 RCU-Sense Voltages to the DCS ADC :
  available on pins 1,3 (5,7) of DCS con#11 – after RCU Power Supply Enable

- DCS FPGA Interrupt (to DCS-Excalibur EXT_INT_PIN , DCS-TP 14) – the RCU drives the line
  Reset (from DCS power supply supervisor , DCS TP 13) " " "
  UART Rxd and TxD (DCS con#1 pins 3 and 4 respectively) " " "

Test of the RCU - DCS connectivity 2/3

Measurement after writing DCS registers with specific test patterns:

- 7 RCU regulators enable lines :
  Verifying the correspondent RCU regulators Enable/Output voltages for different enabling patterns (00, 7F, 59 , 26 hex)

Question/Request to DCS firmware developers:

How access to the DCS ‘VregShutdown xx’ Register ?

Test of the RCU - DCS connectivity 3/3

Verification with specific Logic (both DCS and RCU FPGAs):

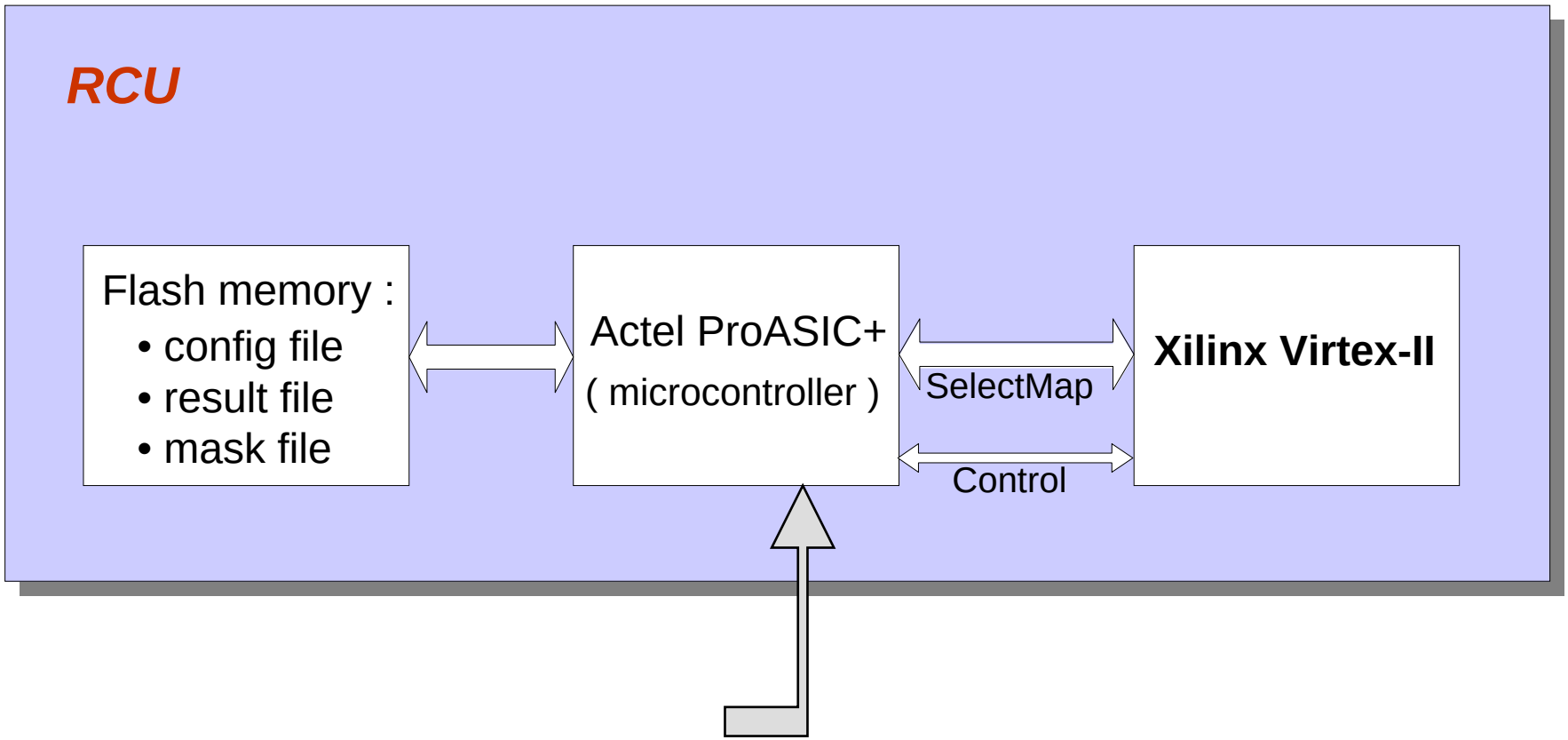
- 32 Bi-directional Data Lines
- 16 Unidirectional DCS→RCU address lines
- 8 Control (bi-directional) lines (DCSCTRL[5..0])

Implementation: DCS is the master, it Writes and Reads back a 53-bit register in the RCU.
The test protocol requires 1 of the not used lines (DCS_CTRL[7]) to set the RCU in Test mode.
The Read/Write line remains DCS_CTRL[2]=R/W , Strobe DCS_CTRL[1]=CSTB

Description of the operations: (Operator send Test Instructions and get results via DCS Eth-link)
1- A test pattern is specified in a dedicated DCS register
2- The command to start the test is issued
3- DCS sets the RCU in test mode, the Test-Write is asserted, the DCS 53 bit test-register (32Data +16Address +5remainingControl) content is copied in the RCU in correspondence of the Strobe
4- When the Test-Write is released, with still the test mode on (Test-Read mode), the RCU puts on the buses the value previously stored for the duration of Strobe.
5- The result is stored in a second DCS test register
6- The cross verification of smart patterns (000, FFF, AAA, 555) allows to verify the connectivity.

Request to DCS firmware developers: Implement the test logic with two 53-bit register (plus relative command decoder and bi-directional line buffers).

Test of the FPGA reconfiguration circuitry 1/3



Configuration File Verification/update via DCS
(Control [7..0], Data [31..0], Addr [15..0] : Shared bus with the Xilinx FPGA)

Test of the FPGA reconfiguration circuitry 2/3

Select Map and Actel – Xilinx dedicated Control Signals :

Sel_Map [7..0]:	Standard I/O on Actel	Dual-purpose for Xilinx
RDWR_B:	Std I/O	Dual Purpose
CS_B:	Std I/O	Dual Purpose
Busy:	Std I/O	Dual Purpose
OE:	Std I/O	Dual Purpose
CLK:	Global	Dual Purpose
OSCCLK:	Global	Dual Purpose
	(It's the Clock from the on-board Quartz)	

CCLK:	Std I/O	CClk Dedicated
CE:	Std I/O	Done Dedicated
CF:	Std I/O	Prog_B Dedicated

Proposed Test: 1- Programming the Actel with the final 'scrubbing' firmware
2- Flashing the memory with the Xilinx Run-firmware'
3- Verifying the correct Xiling programming after RCU Power Cycle

This test **should verify** the whole Actel - Xilinx connectivity. **Isn't it ?**

Test of the FPGA reconfiguration circuitry 3/3

Connectivity between Memory and Actel:

Flash Memory Buses:
Flash_Address [21..0]
Flash_Data [15..0]
Flash_Ctrl [4..0]:Reset, WE, OE, CE, Byte

All of them are Standard I/O on the Actel FPGA

Test Principle:
The test Firmware shall perform a combination of address / data patterns
to be written and read-back from the Memory (i.e. a ramp covering all the locations).

It is a sequence of operation started via a DCS Start signal sent to the Actel FPGA,
the result of the comparison is stored in a specific DCS register.

Request to DCS firmware developers: Adding to the Reconfiguration firmware the block of logic to execute the Flash memory verification described.

Board functional Tests

The use of the set-up for the backplane mass production test (25 Front End Card – holder) represents an easy (and ready) facility to perform the following Functional Tests :

1. Verification of the supply voltages and currents
2. Flashing and checking the Xilinx reconfiguration logic
3. Distribution of the Trigger and Clock signals (from TTC system)
4. Test of RCU accessibility/communication through DDL and DCS interfaces.
5. Readout of the on-board monitor ADCs (input currents and Vtt voltages)
6. Accessibility test of all CSRs via Altro Bus and Slow Control Network
7. FEC Error and Interrupt signals handling
8. Initialization of the FECs
9. Exercising the Readout of FEC with different patterns stored in the ALTRO Pedestal memories
10. Handling of Legal and Illegal trigger sequences (generated with the Local Trigger Unit)
11. Verification of the logic for busy / trigger accept / reject
12. Trigger related data Readout for a combination of sets of
    Trigger rate, Event size and with Sparse Readout logic enabled/disabled

Test Software development

Software programs functionalities required for the Mass Test:

- Read and Write main FPGA registers and test of the overall registers accessibility
- Help in finding misbehaviors in writing and reading back
- Configure the System
- Write in the pedestal memories and readout different patterns
- Check the Readout of trigger related data
- verify the slow control Functionalities
- Handle Error and Interrupt conditions
- Verify the Sparse Readout and FEC-Test Mode readout

Status: we have developed some very basic Labview Vis and C modules for the prototype characterization.

Urgent : to complete the set and verifying its reliability by end of May.

Summary

Mass production organizational aspects are well on track :

Price Inquiry will be closed the 15.04, the week after we will know the awarded Firm

We are on time for the procurement of all the components,

getting (pretty) good prices and delivery time.

Mass Tests procedure is completely defined.

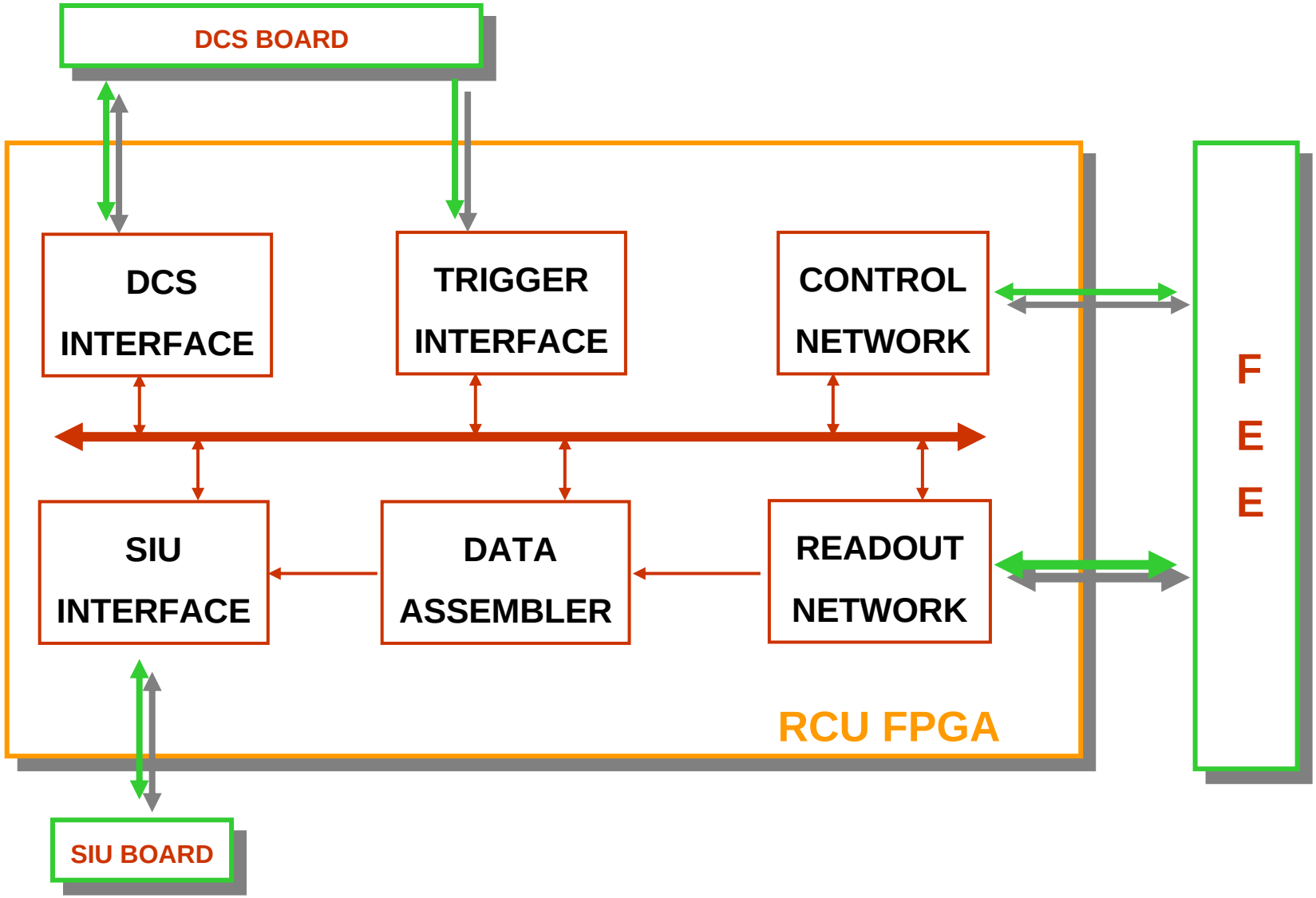
Tools for the Mass Test : Some of them are ready,

others require common efforts to get them ready on time. In particular :

1. Implementation of the mass test-logic blocks in the RCU-Xilinx firmware.
2. Modification of the FEC Board Controller Firmware for the test of the ALTRO-bus interface
3. DDL mode of operation that allows the verification (flipping) of all the SIU Interface lines
4. DCS Firmware 'Test – blocks' to check the connectivity with the RCU and Scrubbing circuitry
5. Actel Firmware to verify the connectivity with the Flash memory
6. Development of Test analysis software (Labview and C)

End of the presentation

Readout Control Unit – Firmware



Complete production Mass test – Time estimation

Each RCU module requires the following time estimation for the mass production test:

The electrical tests of each :	~ 20 min
The Functional Test	~ 30 min
The filling of the production Data Base	
The filling of the Test Log-book	
Final verification and Packing	~ 15 min
	~ 1h per card

→ 8 cards per day

→ ~ 35 working days (2 months)

(full production delivery estimated by end of July)

→ starting from august … completed by October.