

Progress on the RCU Prototyping

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CERN PH/ED



Overview



Architecture



Trigger and Clock Distribution



Instruction Sequences



Current Capabilities



Present Status

On Behalf of:

Carmen Gonzalez Gutierrez

Roberto Campagnolo

Roland Bramm

Torsten Alt

Kjetil Ullaland

Jorgen Lien

Are Martinsen

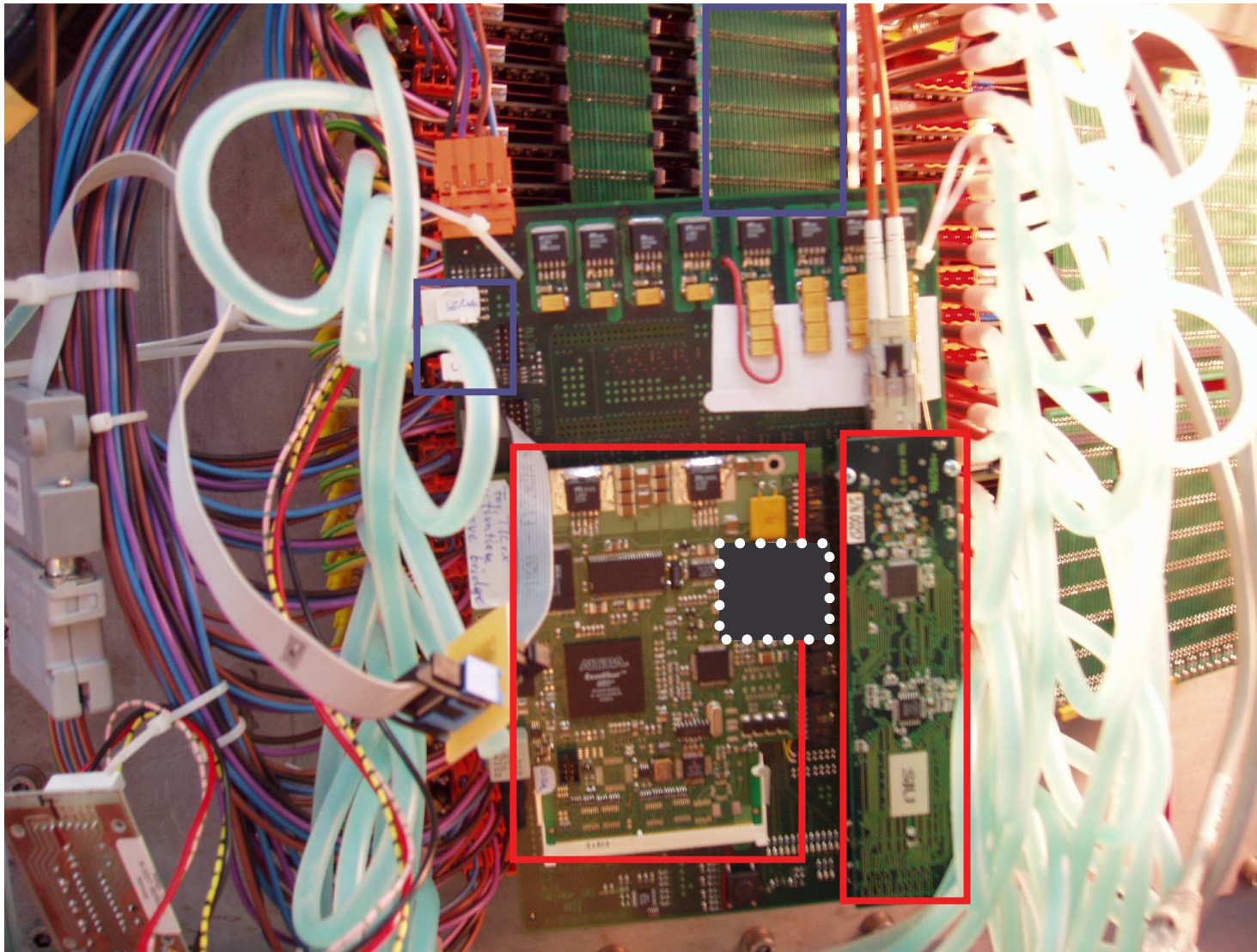
Matthias Richter

Heinz Tilsner

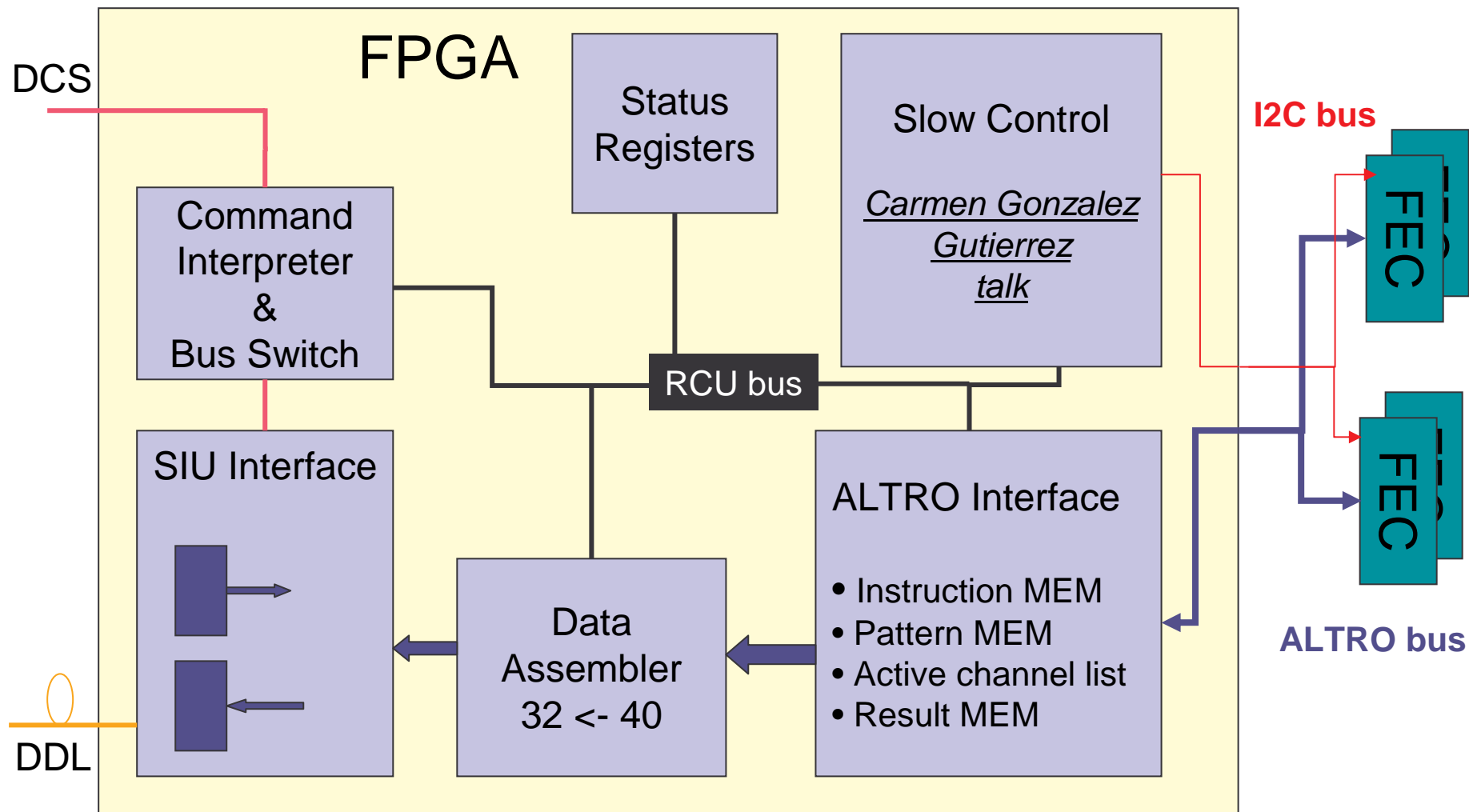
Sebastian Bablok

Christian Kofler

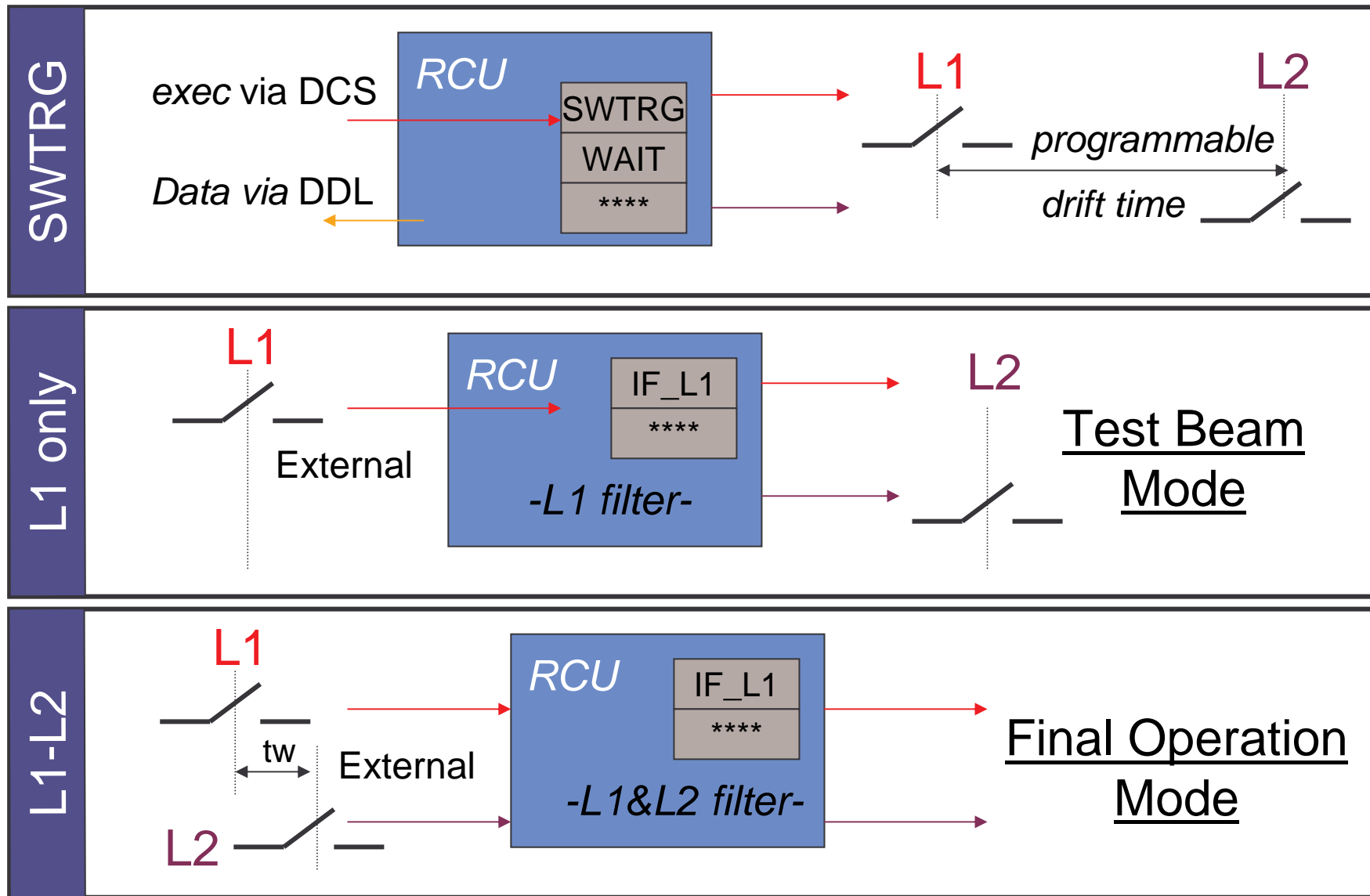
Overall Frontend System



Architecture

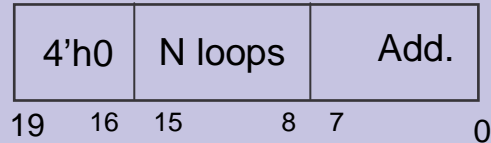


ALTRO Interface: Trigger Modes

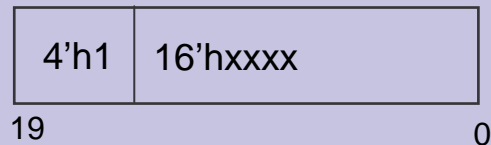


Instruction Codebook

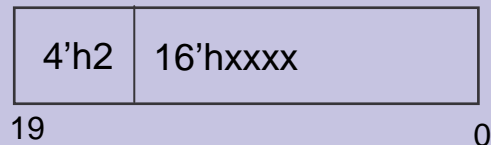
JUMP/LOOP



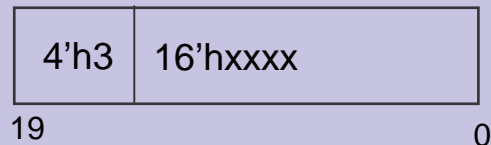
RS_STATUS



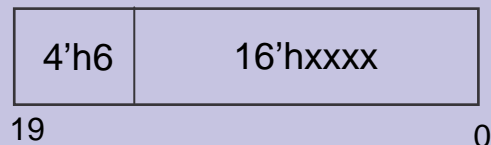
RS_L1CNT



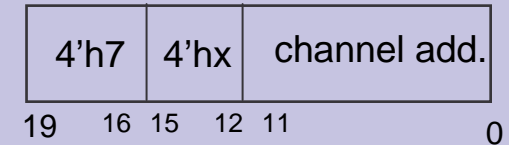
RS_L2CNT



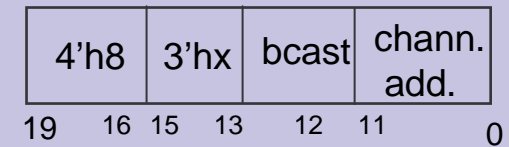
CHRDO



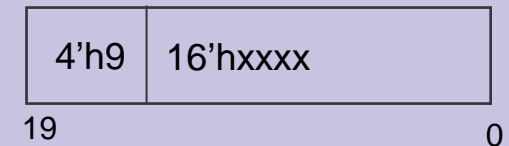
PMREAD



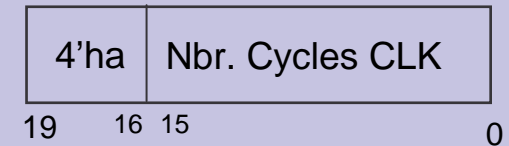
PMWRITE



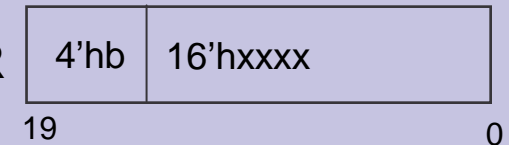
END



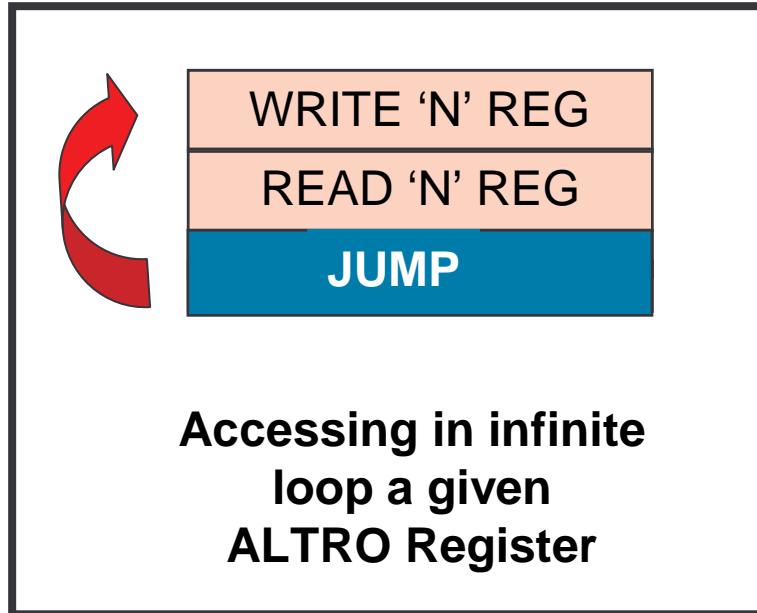
WAIT



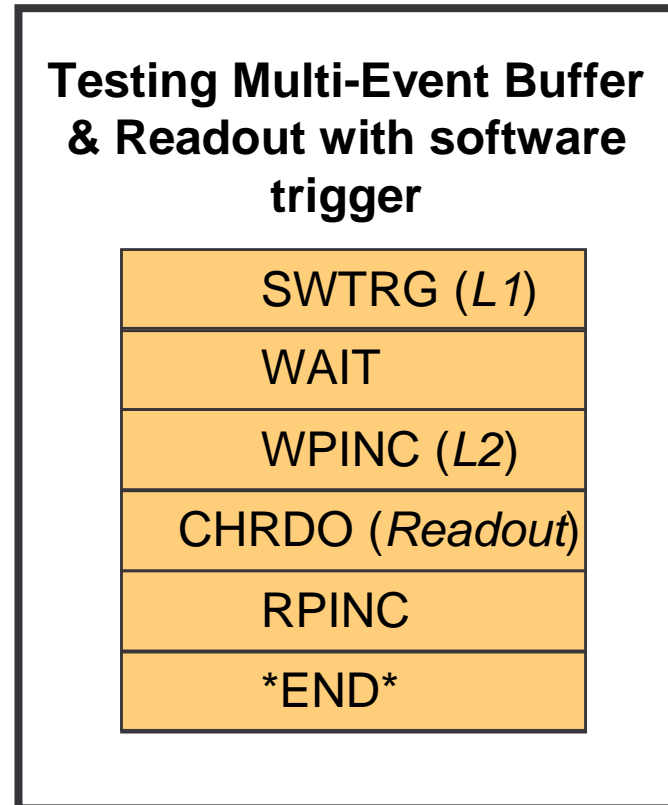
IF_TRIGGER



Examples of Instruction Sequences



Scope probing for electrical integrity check



From ALTROs to DAQ w/ software trigger

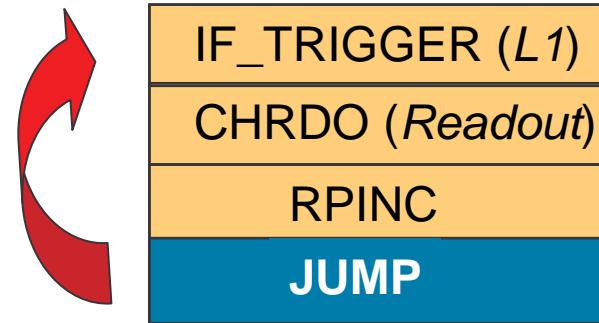
Examples of Instruction Sequences

Cardio Test

READ HWADD '0'
READ HWADD '1'
- - -
READ HWADD 'i-1'
READ HWADD 'i'
END

Which cards are responding to basic register access?

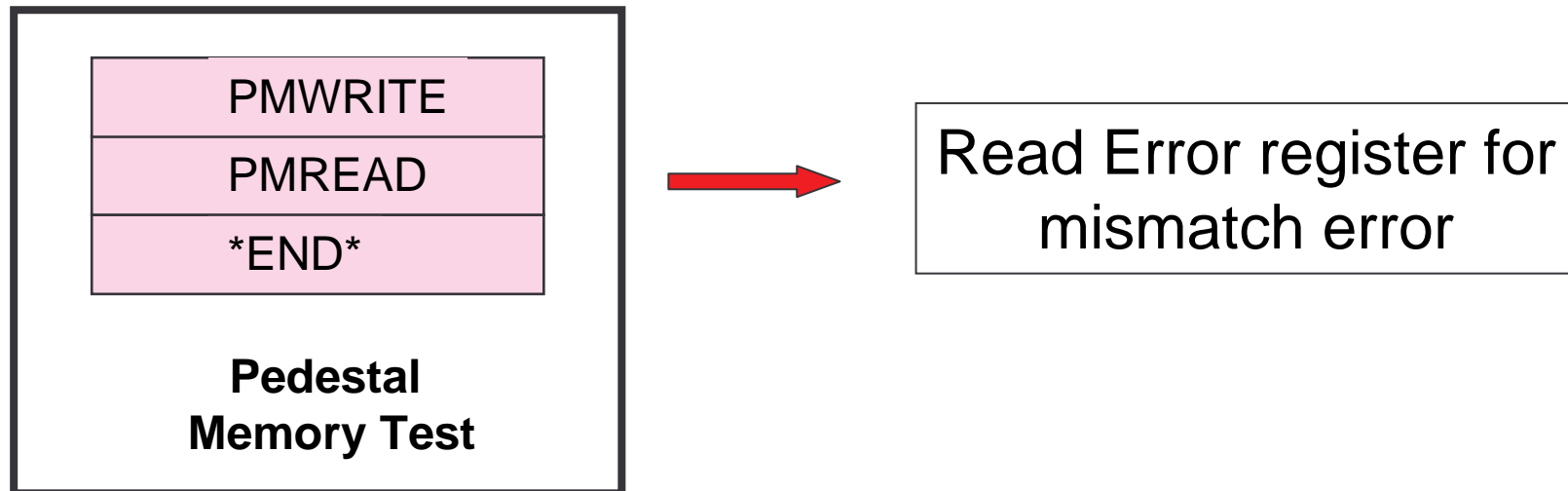
Test Beam Mode



From ALTROs to DAQ w/ external L1-trigger:

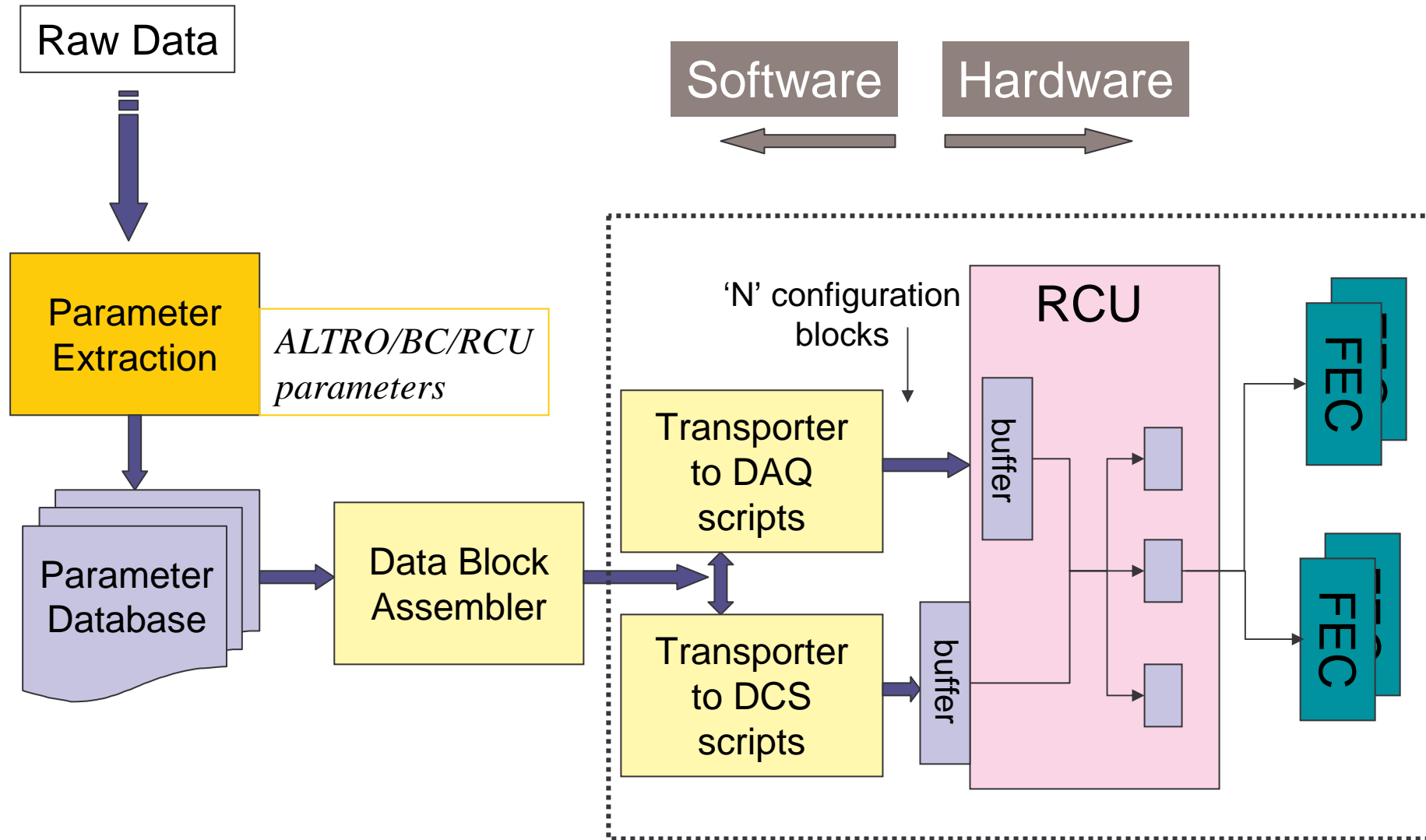
- ADC sampled data
- Pattern stimuli

Examples of Instruction Sequences



Checking ALTRO Pedestal
memory access in a fast way

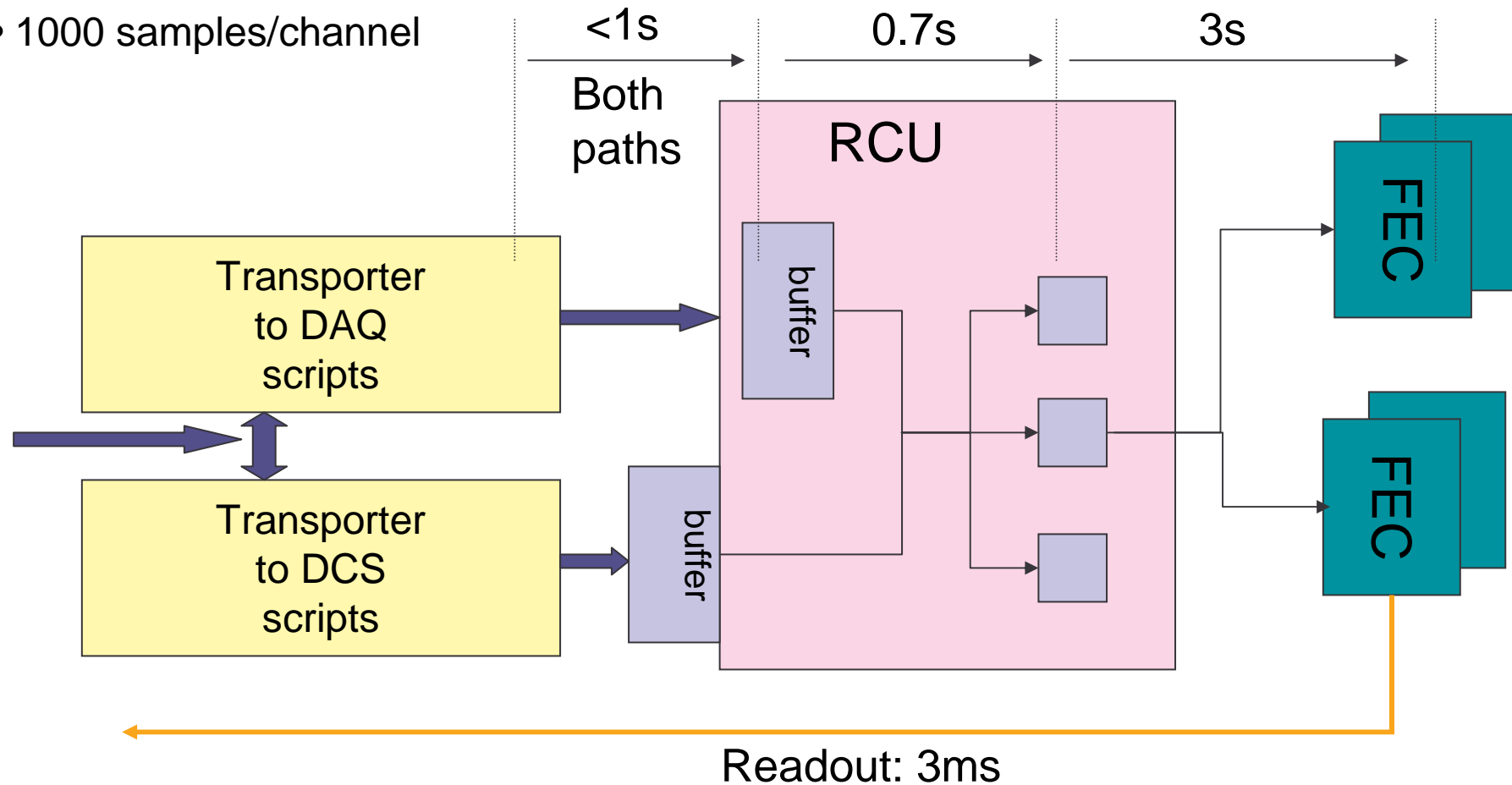
Current Configuration Paths



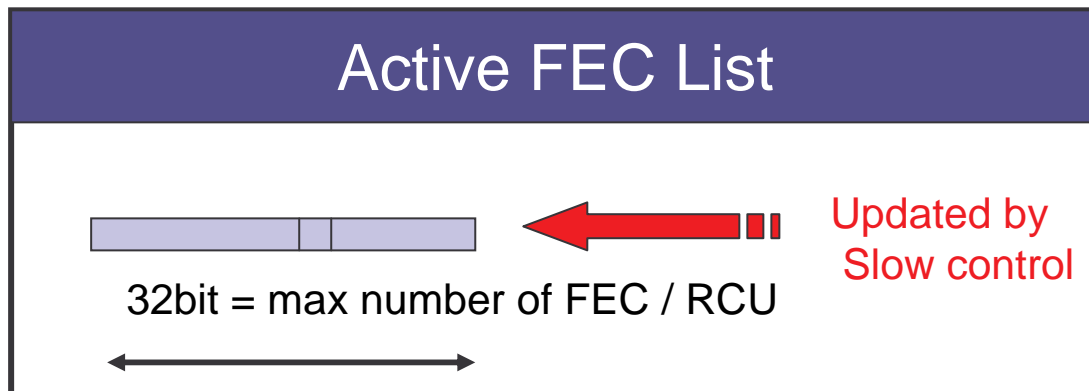
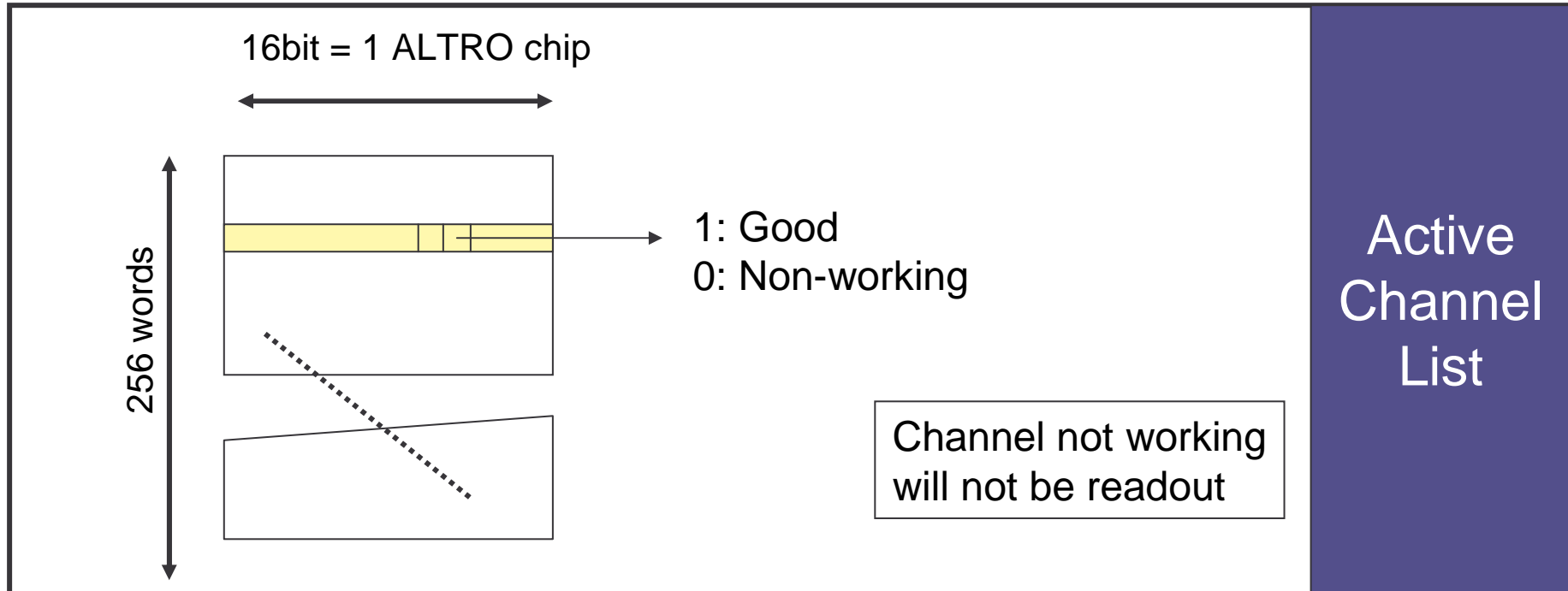
Configuration and Readout Time

Overall configuration data: 7MByte/RCU - Worst case scenario:

- 3200 active channels
- 1000 samples/channel

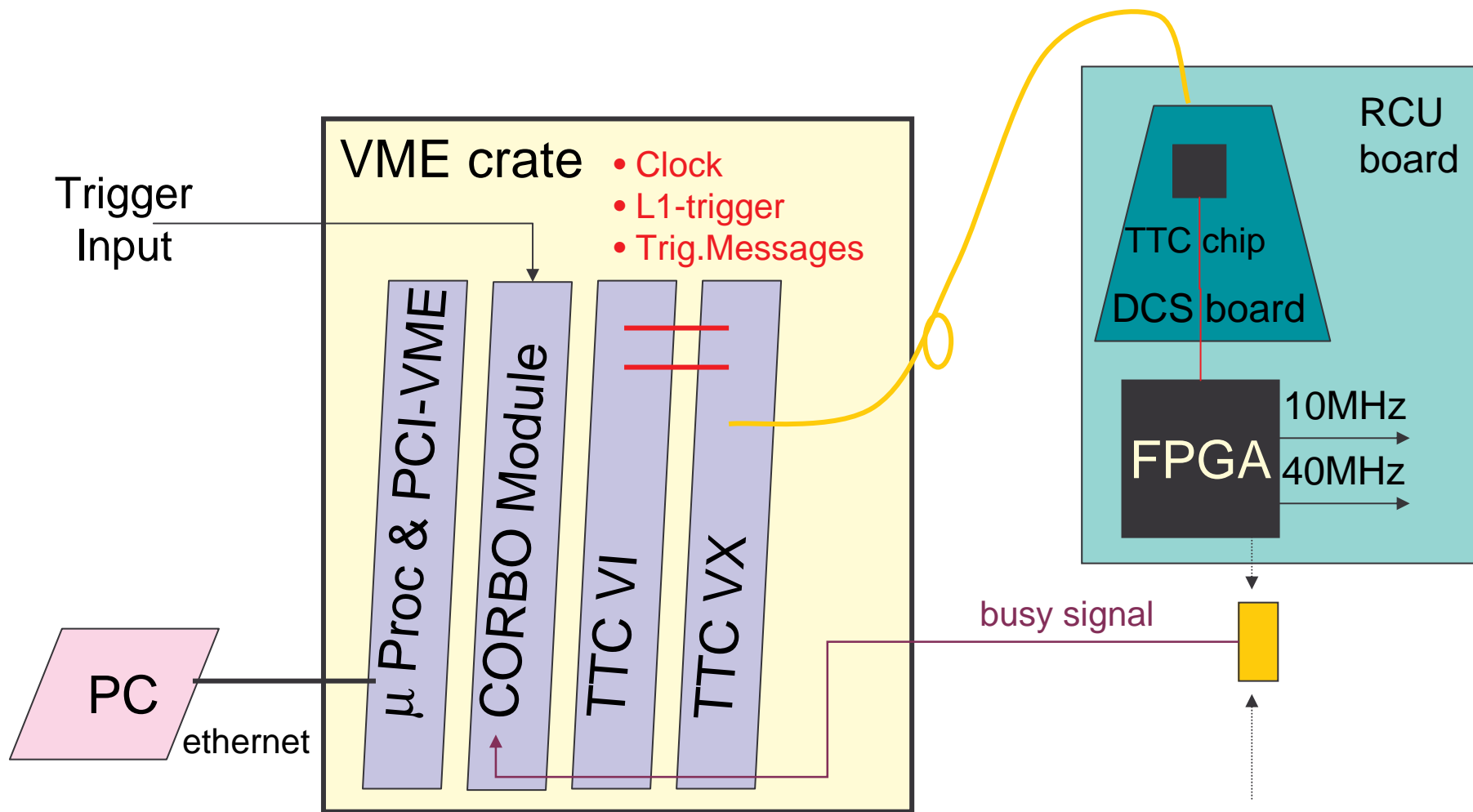


Active Channel / FEC List



Improving readout efficiency by storing the current status of one channel or board

Current Trigger and Clock Distribution



Operation in High Trigger Rate

4.7KHz Event Rate



80MByte/s

LDC status display

LDC name: epaitbeam01ldc

Events recorded

Events recorded rate

Bytes injected

Bytes injected rate

Bytes recorded

Bytes recorded rate

Bytes in buffer

Number of Equipments

Readout SOR/EOR phases

Recorder SOR/EOR phases

edmMaskValidityRange

GDCs nearly full

GDC status

GDC name

Number of events

Event rate

Events recorded

Events recorded rate

Bytes injected

Bytes recorded

Bytes recorded rate

Event builder SOR/EOR phases

Event builder status

STANDALONE_DAQ

File View Options Windows

DAQ - Run Control

DOMAIN: tpc32547

Disconnected Configuration

Connected Run Parameters

Ready to start

Data Taking Phase

Start Processes

Run AutoStart

Recording Enabled

AFFAIR HLT

GDC ON

ALIMDC EDM

Start

Stop

Pause trigger

Abort

RUN NUMBER : 264 DAQ Internal Logic Engine Status : STARTING_LDCS

Info: Starting run 264: Please wait

Trace

Fri 14 17:19 Starting run 264

Fri 14 17:18 Run parameters loaded from : /dateSite/configurationFiles/RunParameters.rcPa

Fri 14 17:18 Configuration loaded from : /dateSite/configurationFiles/DAQconfiguration.rcCor

Fri 14 17:18 RC options loaded from : /dateSite/configurationFiles/RCoptions.rcOpts

Fri 14 17:18 Run number read from /dateSite/configurationFiles/runNumber.config

Conditions:

- 100 samples/channel
- 128 channels
- 40MHz Readout clk
- 10MHz Sampling clk

Exercise of full Readout Chain was performed successfully at KHz range trigger

Present Status

RCU Development

✓ System fully tested and operational:

- 2 branches (12 + 13 frontend cards) in a total of 3200 channels
- DCS board running Linux on ARM processor and Ethernet link (*Torsten Alt talk*)
- DAQ with both DAVE system and lower level script language for config.
- Communication between RCU and HLT fully operational
- Installed in the T10 Area, ready for beam (*Roberto Campagnolo talk*)

✓ ALTRO Configuration tested using both the DCS board and the DDL link

✓ Slow Control through I²C fully operational measuring T^o, Currents and Voltages
(*Carmen Gonzalez Gutierrez talk*)

~~✓~~ Configuration of the RCU firmware from the DCS Board close to completion

? Improvement in readout time by a factor of 2: Replication of readout logic