Radiation tests of the TPC FEE

CERN, 30 August 2004

Luciano Musa – CERN / PH - ED

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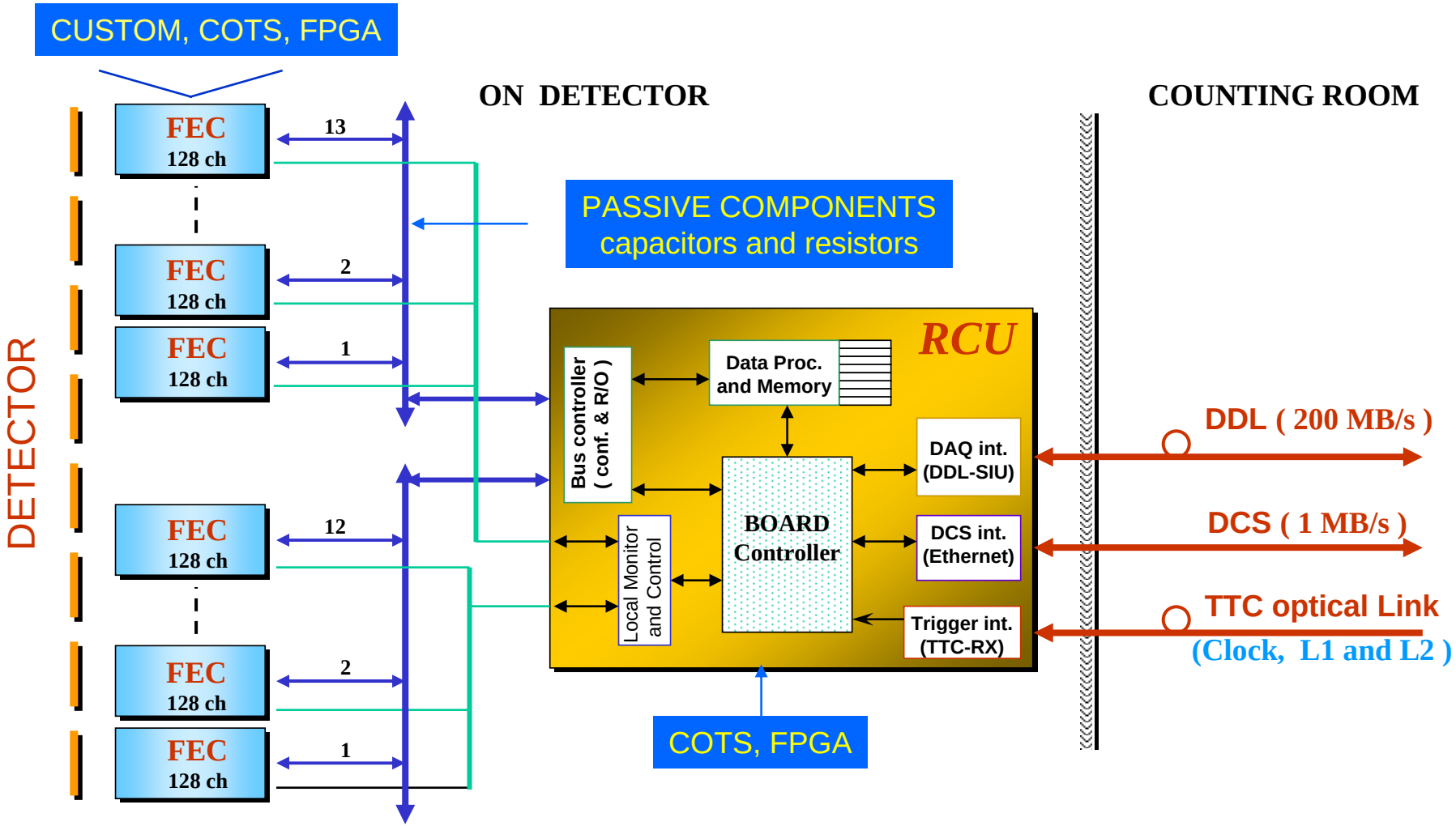
- System overview
- Radiation Levels at the TPC
- Radiation Facilities and Test Setup
- Characterization (TID and SEE) of the FEC components
  - Custom (ALTRO and PASA)
  - COTS (LDO, VREF, AMPLIFIERS, TRANSCEIVERS, BUFFERS, CAP., etc.)
  - FPGA (ALTERA ACEX1K30)
- Characterization of RCU → see the talks of D. Röhrich, M. Stockmayer and C. Soos

System Overview

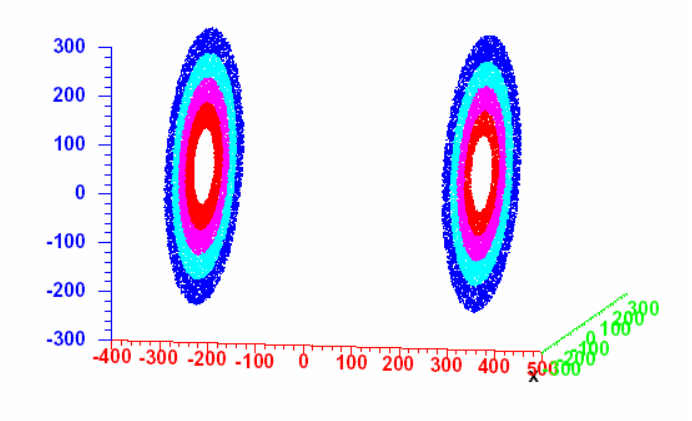
Each of the 36 TPC Sectors contains 6 Readout Partitions



Overall TPC: 4356 Front End Card 216 RCUs

Radiation Levels at the TPC

Simulation with 4 scoring regions



TID	
@ TPC_{in}	1.6 krad
@ TPC_{out}	0.22 krad

Sum Flux with E_{kin} > 10MeV (cm^{-2} s^{-1})

Layers	1	2	3	4
absorber side	384	268	187	129
Non-absorber side	245	149	112	81

Georgios Tsiledakis, GSI

Agreement with A, Morsch and B. Pastircak
ALICE-INT-2002-28 Version 1.0

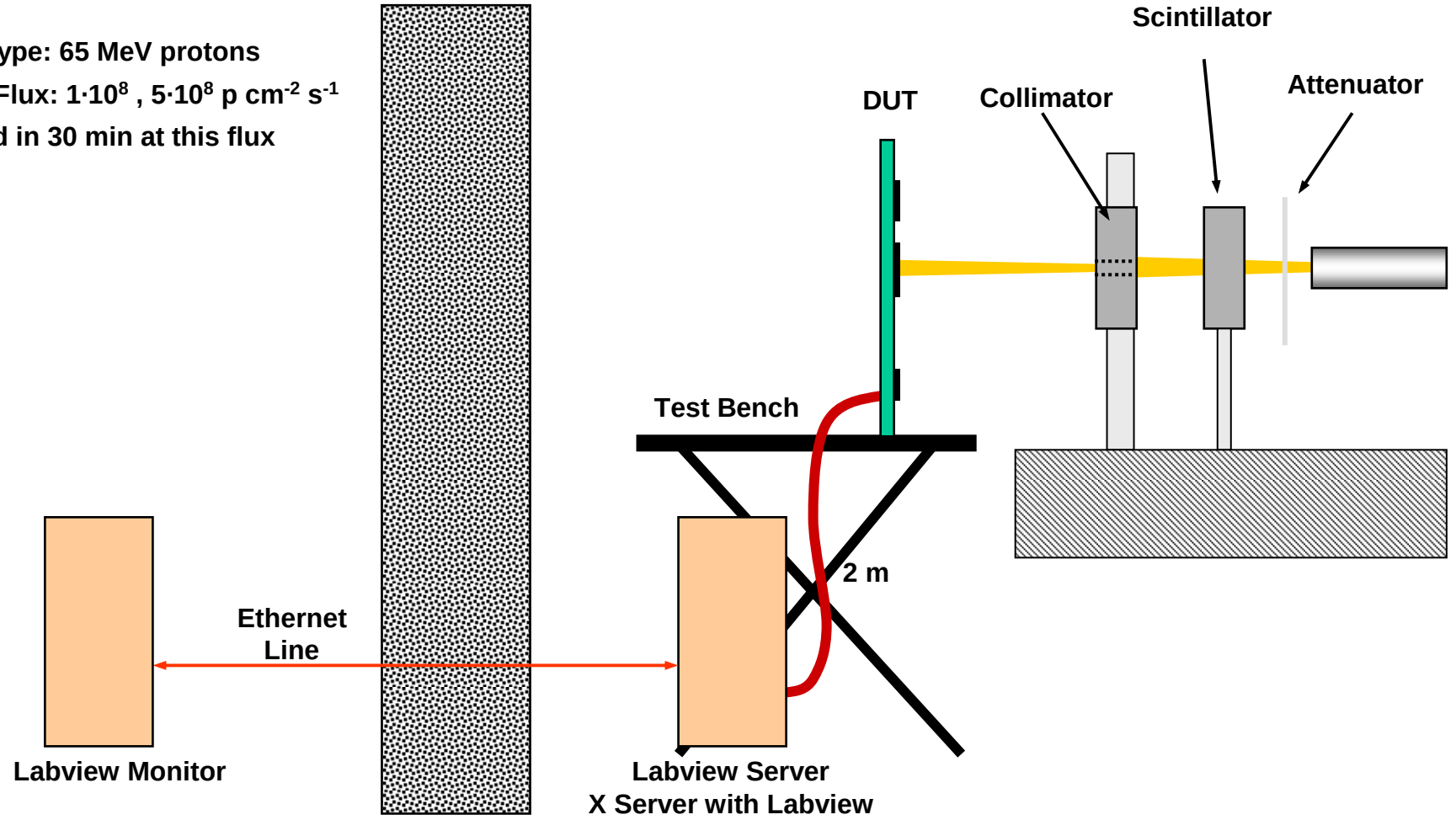
Test (I) 2002

Test at UCL, Louvain-la-Neuve, Belgium

Beam Type: 65 MeV protons

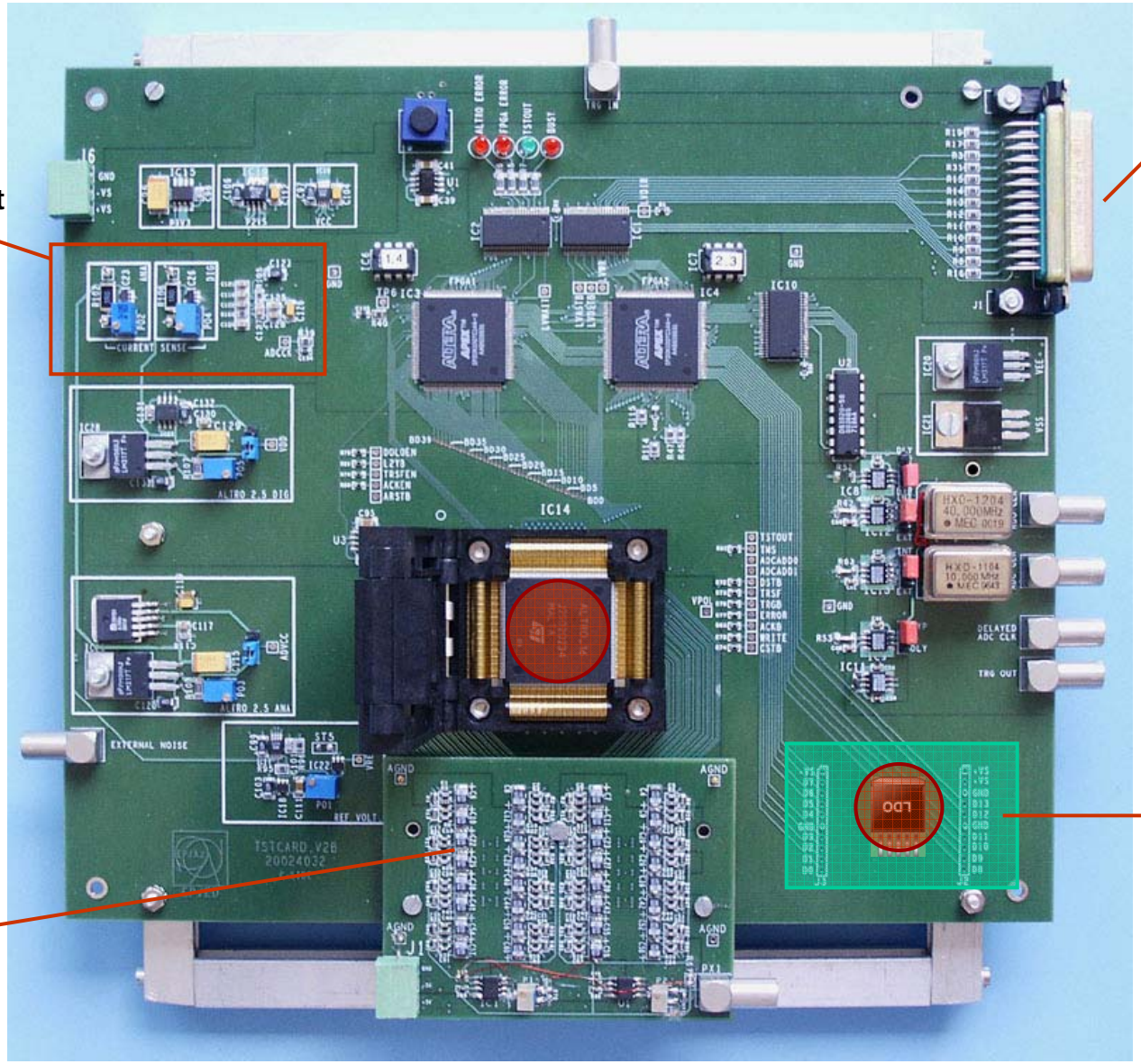
Proton Flux: $1 \cdot 10^8$, $5 \cdot 10^8$ p cm^{-2} s^{-1}

100 krad in 30 min at this flux



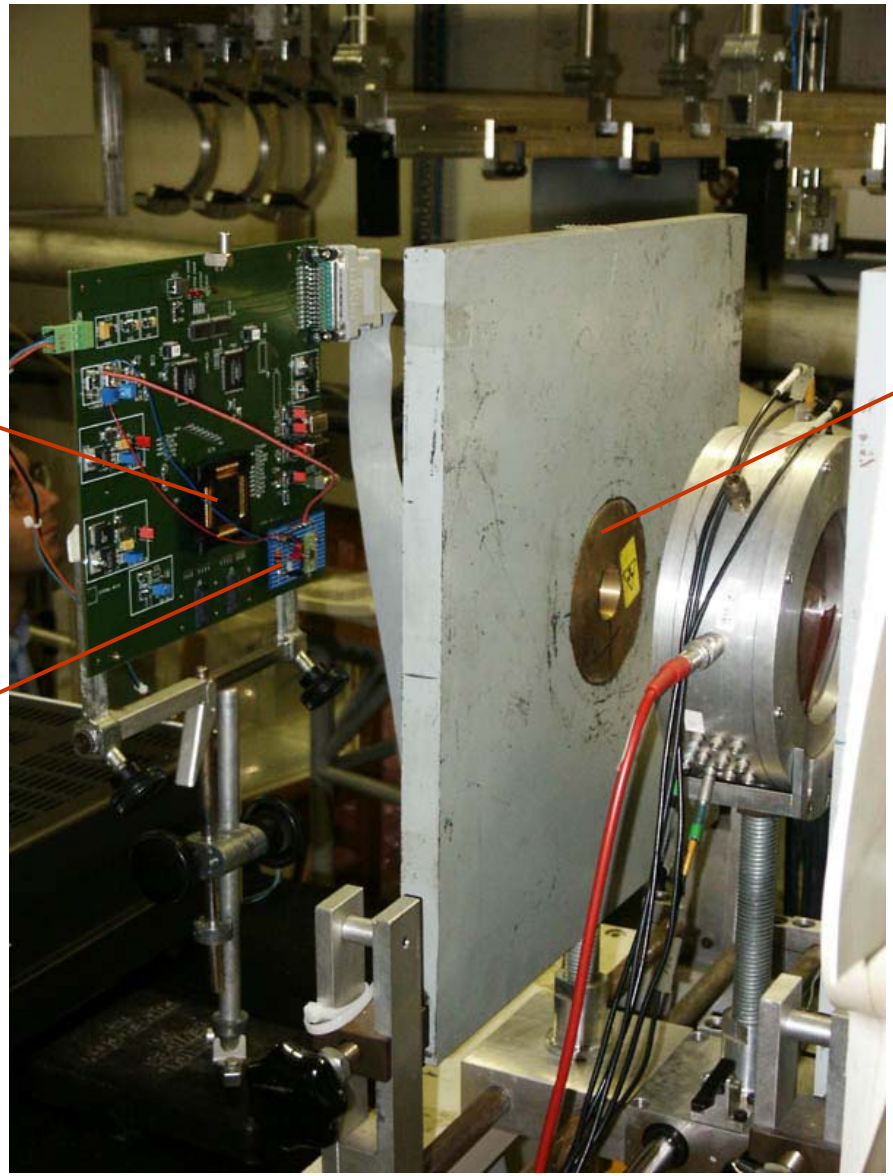
Test Setup for ALTRO and LDO

Test (I) 2002



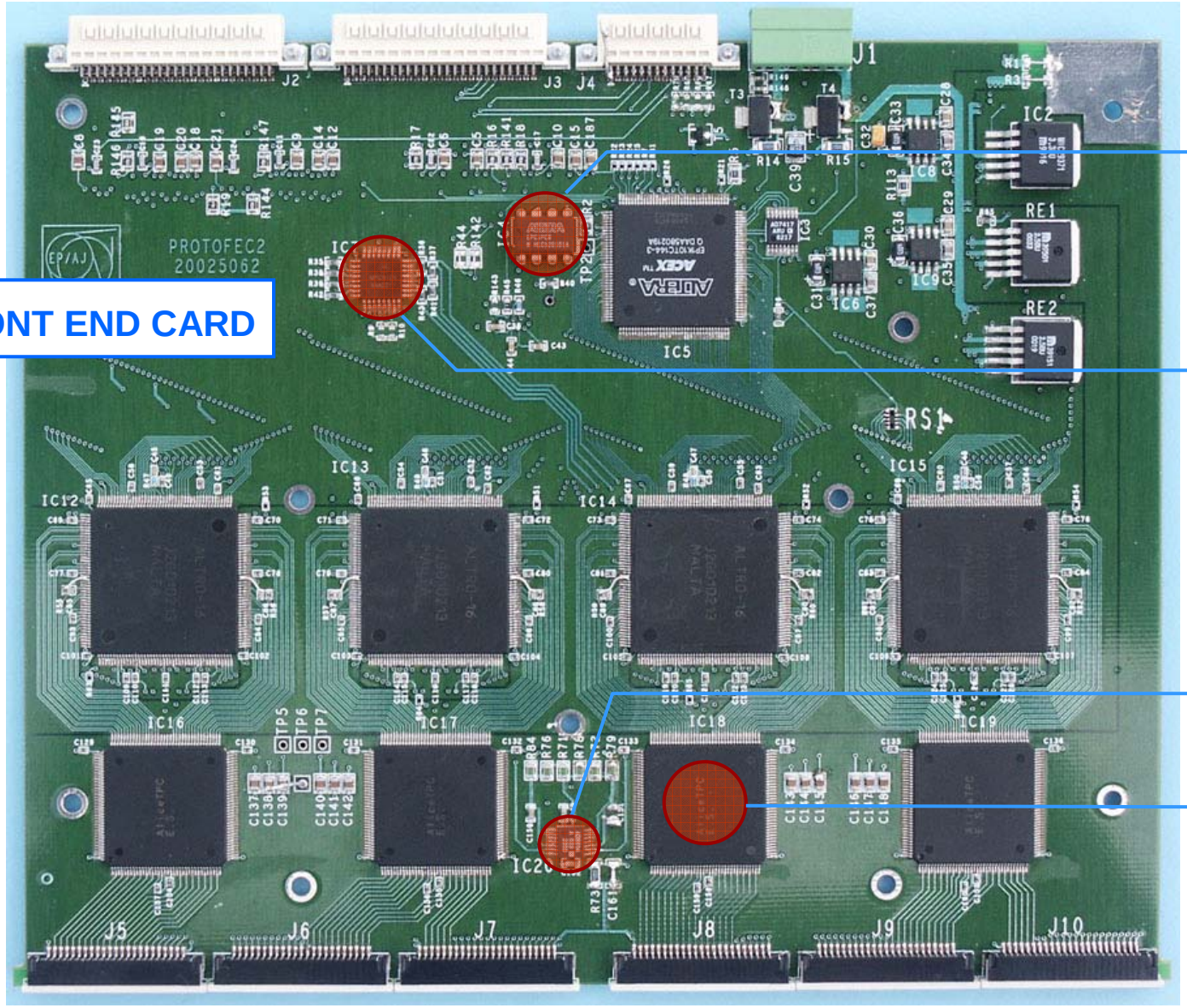
Radiation Facilities and Test Setup

Test (I)
2002



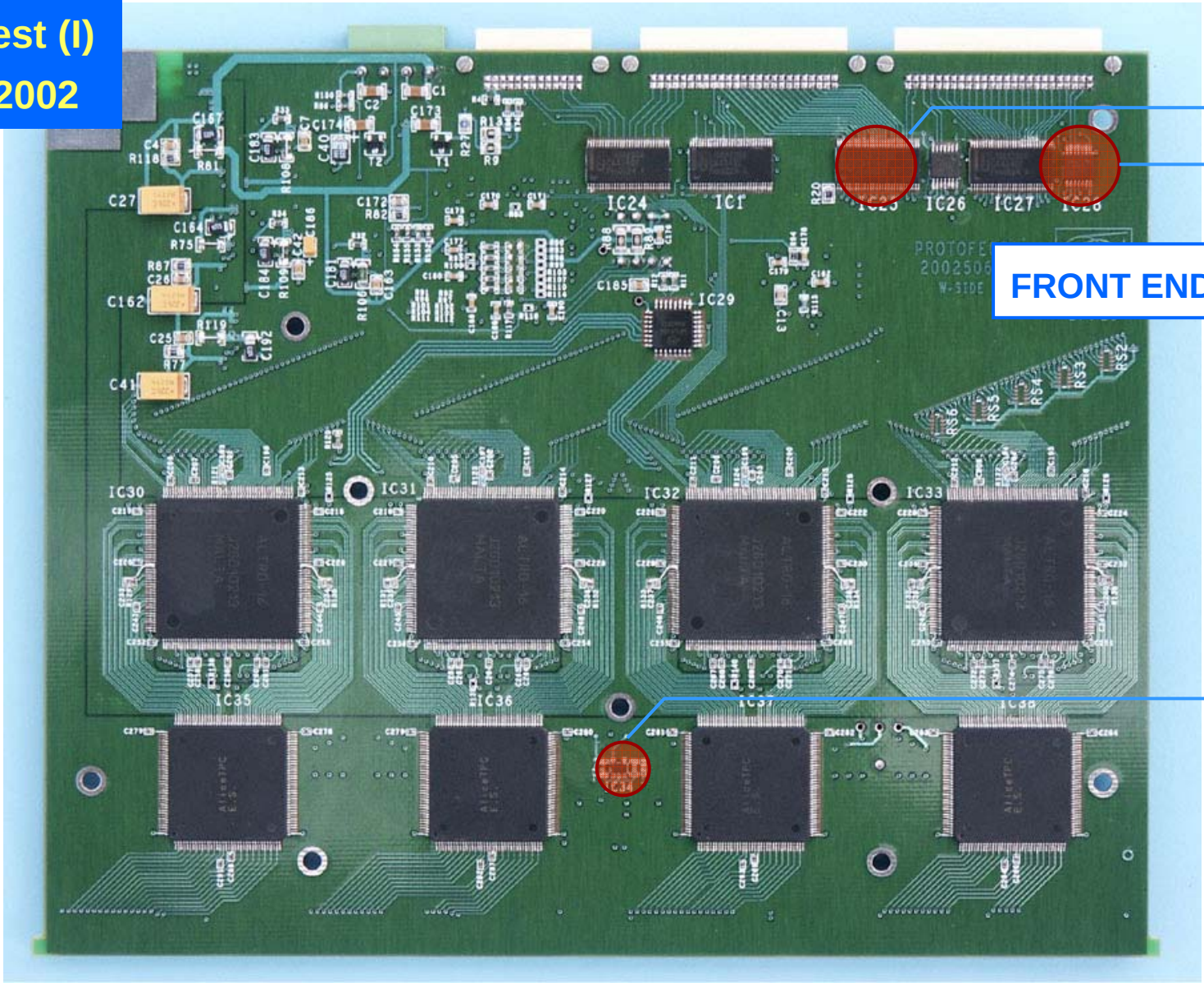
Radiation Facilities and Test Setup

Test (I)
2002



Radiation Facilities and Test Setup

Test (I)
2002



Radiation Facilities and Test Setup

Test (I) 2002

Radiation Facilities and Test Setup

Test (II)
2003 - 2004

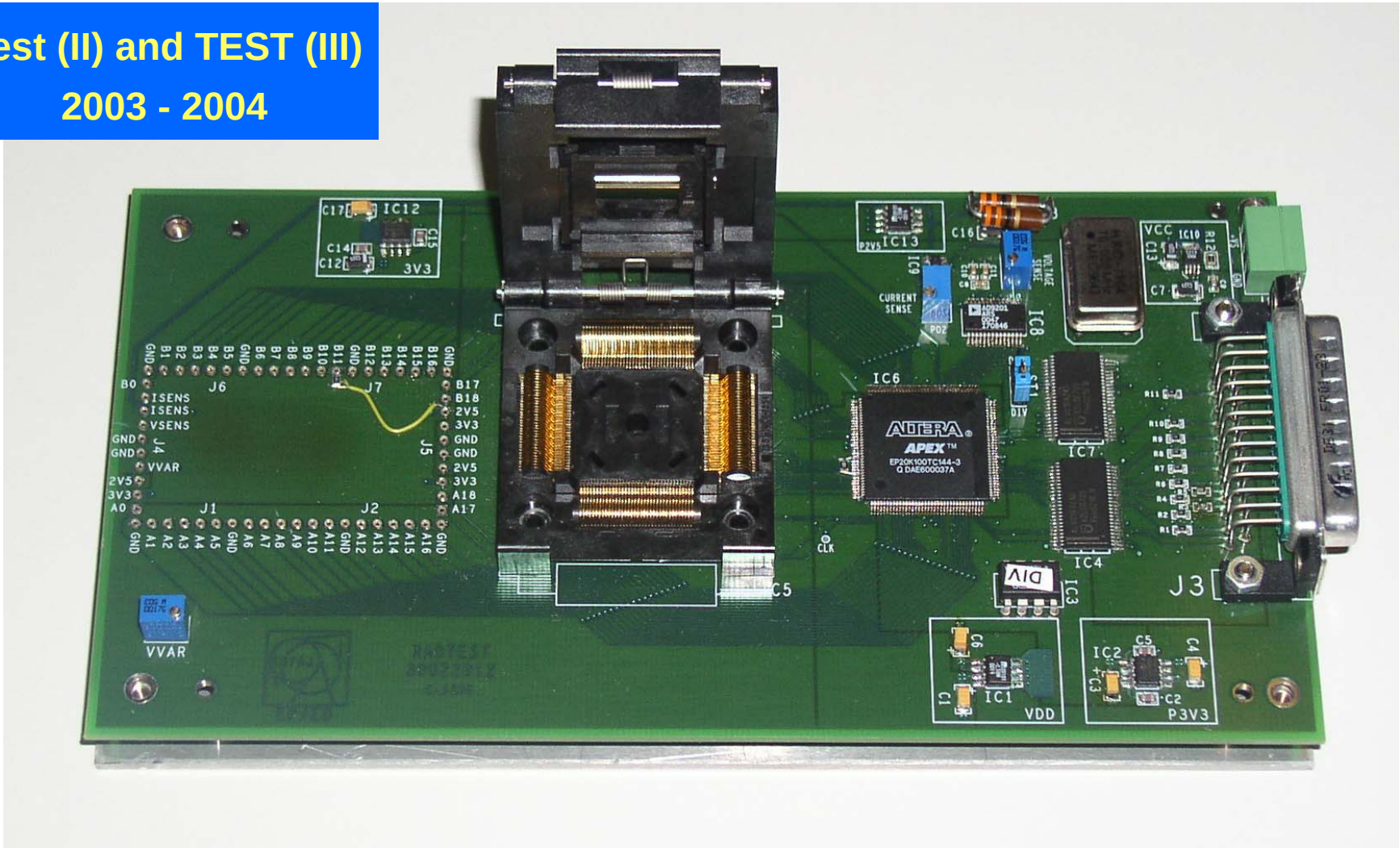
- Oslo Cyclotron
  - 25 and 28 MeV external proton beam
  - flux ~ 10^7 – 10^8 protons/s cm²
  - Beam profile: spot 1.5cm x 1.5cm

Test (III)
2004

- TSL (Uppsala)
  - 38 and 180 MeV external proton beam
  - flux ~ 10^7 – 10^8 protons/s cm²
  - Beam profile:
    - spot ∅ 3cm

Test Setup for COTS and FPGA

Test (II) and TEST (III)
2003 - 2004



Tested Parts (1/2)

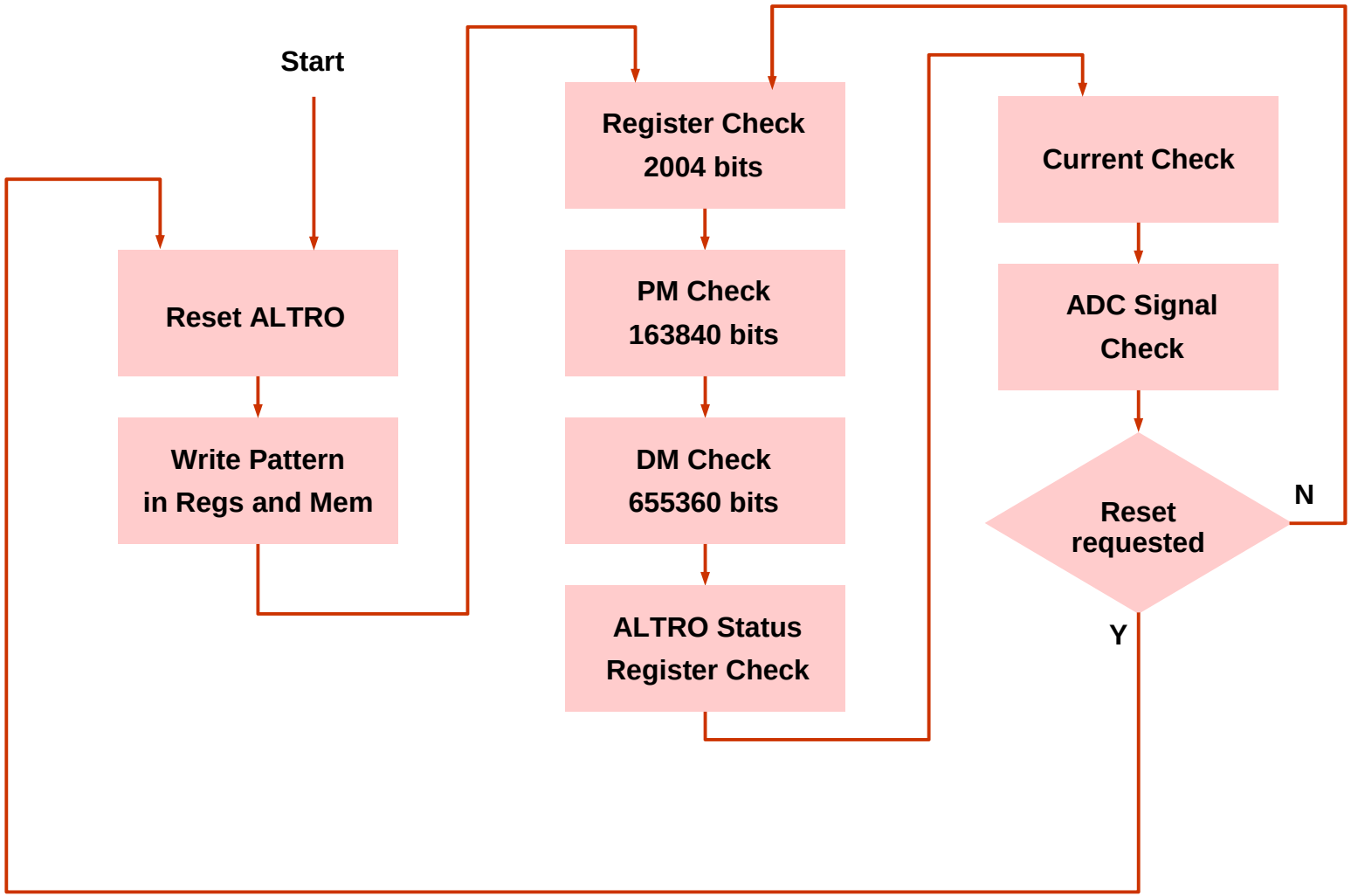
Name	Type	Technology	No. Parts	TID (krad)
ALTRO-16	ADC + DP	CMOS	4	312
PASA	Shaping/Amp	CMOS	4	96
MIC39151	Volt. Reg.	Bipolar	12	30
MIC29371	Volt. Reg.	Bipolar	10	30
TC1173	Volt. Reg.	Bipolar	6	40
LP3962/61	Volt. Reg.	CMOS	3	30
TI757	Volt. Reg.	CMOS	2	30
OPA4364	OpAmp	Bipolar	5	30
AD8604	OpAmp	CMOS	8	30
MAX4254	OpAmp	CMOS	1	30
TC1265	Ref. Volt.	CMOS	2	84
LM4140	Ref. Volt.	Bipolar	10	30

Tested Parts (2/2)

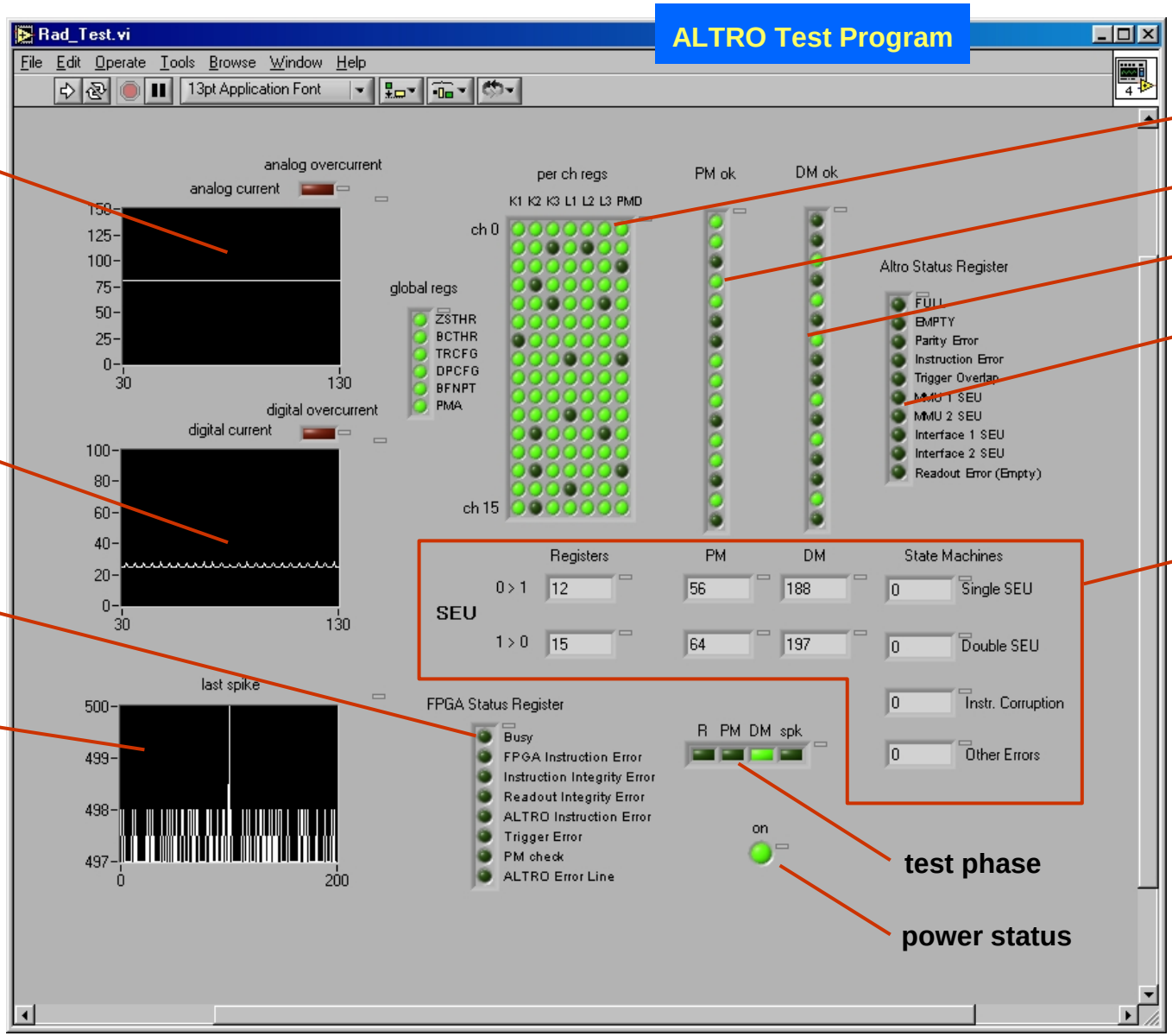
Name	Type	Technology	No. Parts	TID (krad)
LM4040 / 41	Ref. Volt.	Bipolar	10	30
LM385	Ref. Volt.	Bipolar	10	30
STM-TS821 / 2	Ref. Volt.	CMOS	4	30
GTL16612	Transceiver	Bi-CMOS	8	48
MPC9109	Buffer	CMOS	6	100
BAT54	Diode	Bipolar	4	30
MMBT2222A	BJT	Bipolar	4	30
Electrolytic Cap	Capacitors	Tantalum	20	100
EPC1441	EPROM	CMOS	10	
ACEX1K30	FPGA	CMOS	5	100

TOTAL NUMBER OF TESTED PARTS **146**

ALTRO Test Loop



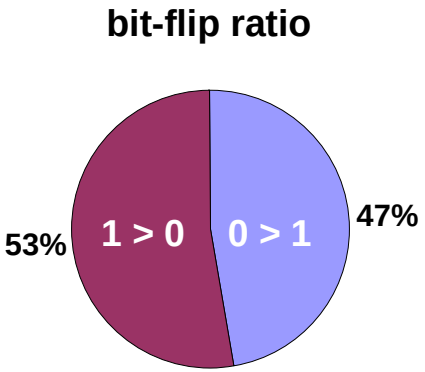
Custom Components - ALTRO



Test Results

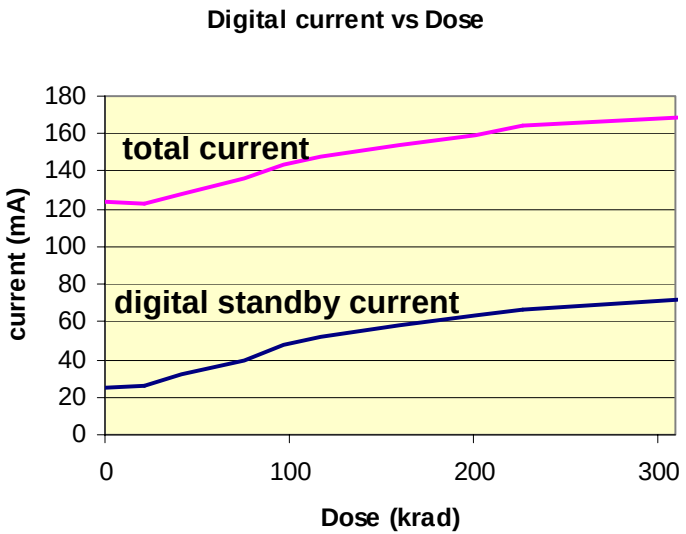
Error Cross Section

Memory Error Cross Section:	$1.10 \cdot 10^{-14}$	$cm^2\ bit^{-1}$
Register Error Cross Section:	$7.02 \cdot 10^{-14}$	$cm^2\ bit^{-1}$
Hamming Error Cross Section:	$7.50 \cdot 10^{-14}$	$cm^2\ bit^{-1}$



Observations

- Slightly more flips from 1 to 0 than from 0 to 1
- Digital current increases with dose (leakage increases)
- Analog current stays the same
- ADC bit flips very rare
- Small spikes in analog part of ADC above 160 krad



Test Results

Annealing

- After 2 weeks at room temperature: 43 mA standby current (+13.5% over total)
- After 3 months at room temperature: back to normal

- At a low flux, annealing and damage may compensate

All 4 irradiated chips continue to work today

System Level Consequences

For a sub-sector equipped with 200 ALTROS (1 RCU)

	Registers	Pedestal Memory	Data Memory	Hamming Machines
SEU per hour	0.023	0.36	1.43	0.0007
MTBF	36 hours	168 minutes	42 minutes	58 days

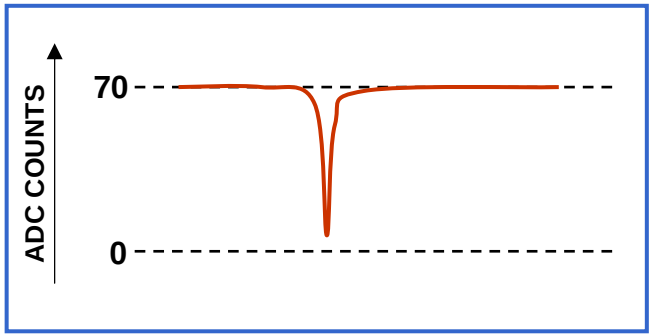
Worst-case figure

Innermost Readout Partition @ absorber side

PASA Test Results

Test Procedure

- Monitoring of current consumption
- Repetitive acquisition of output of 16 ch.
- Monitoring of baseline value
- Monitoring of gain
- Automatic spike detection



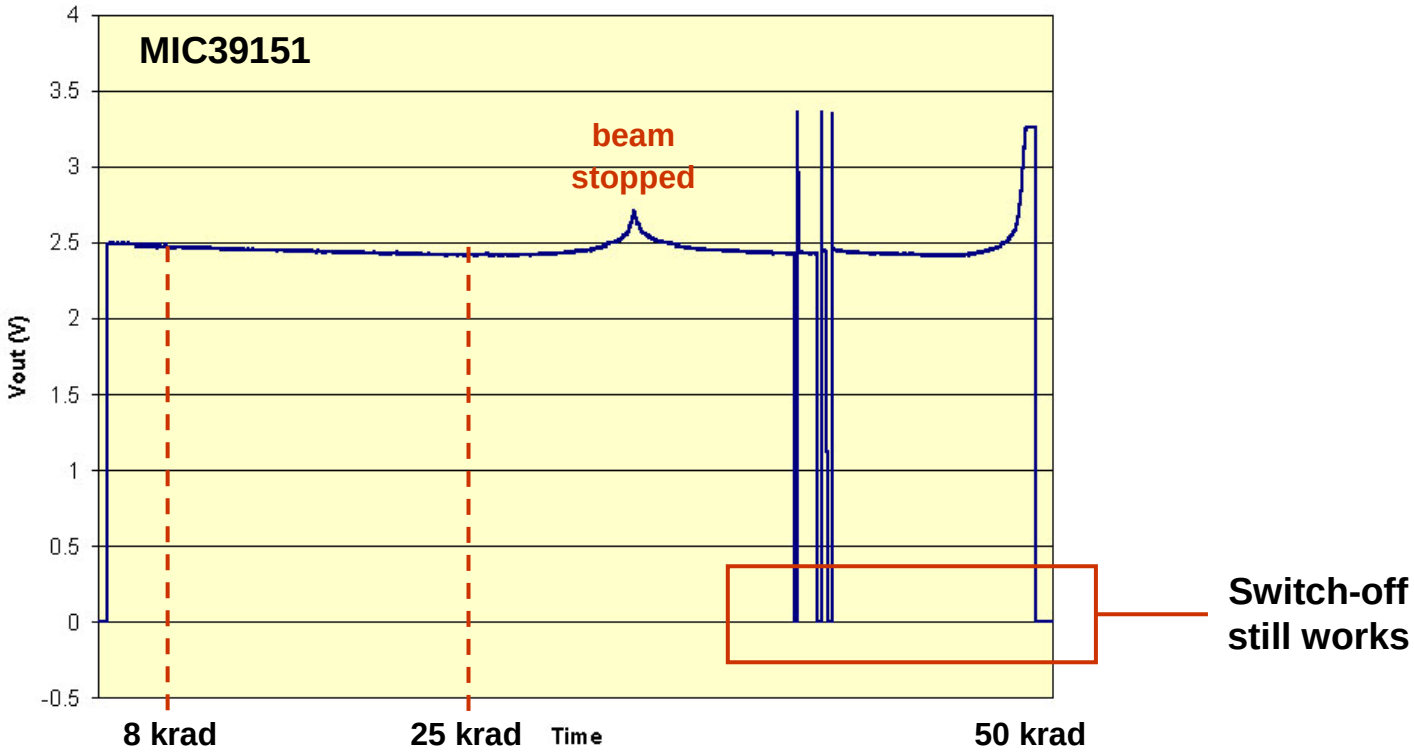
Negative spikes in the baseline

Test Results (TID = 96 krad)

- No variations in current consumption
- No variations in baseline level
- No variations in gain
- Negative spikes observed frequently (due to high flux)

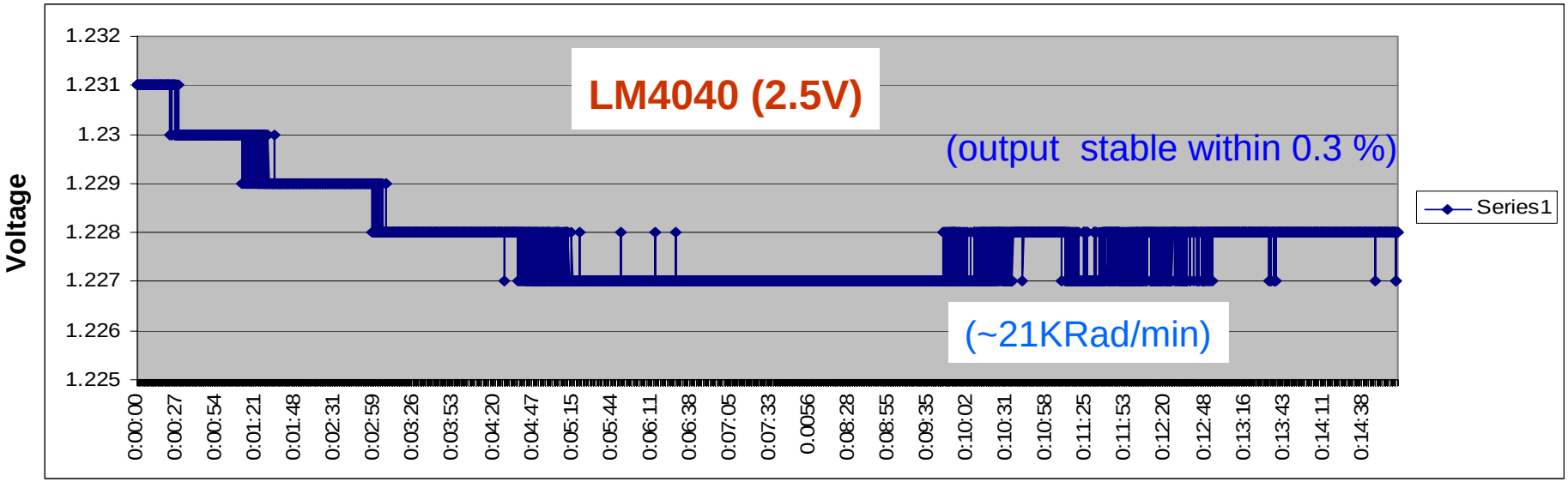
COTS – Voltage Regulators

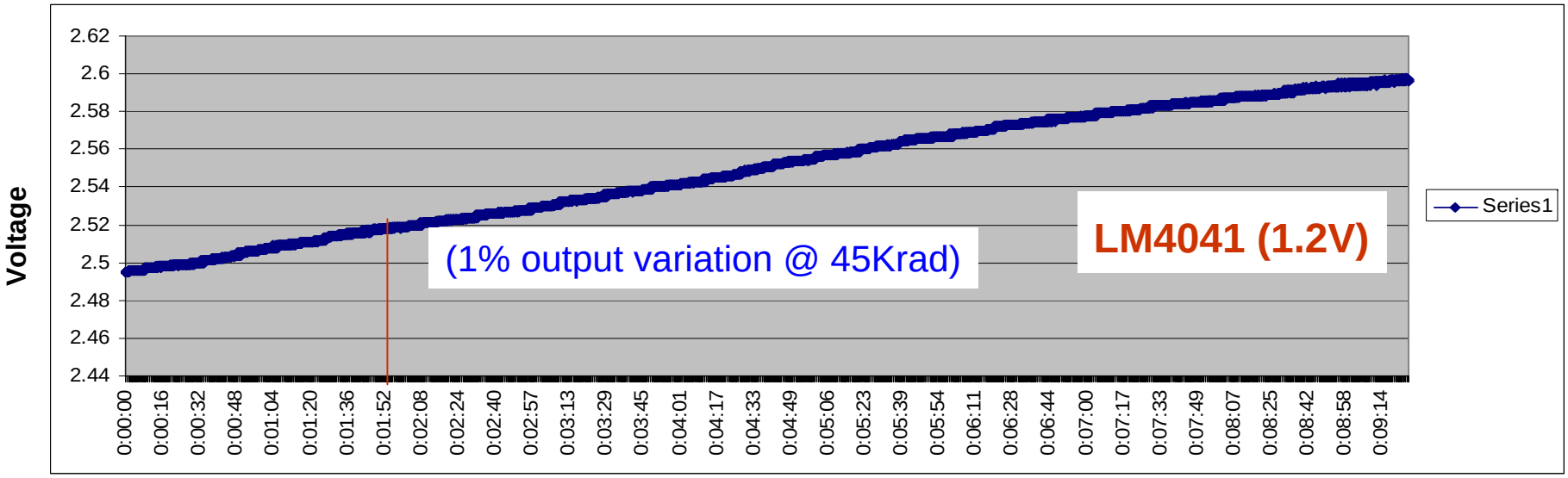
MIC39151 died after 30 krad (switch-off still possible)



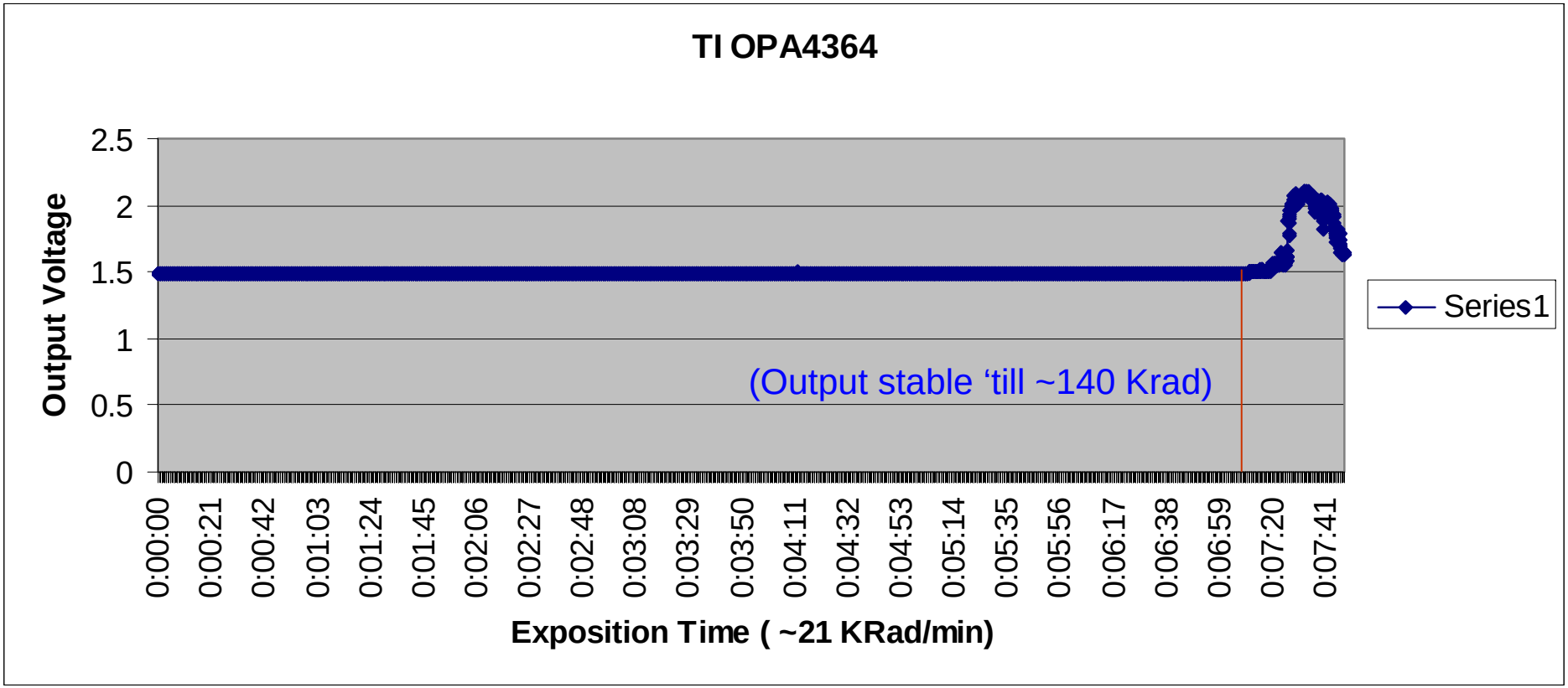
MIC39151 still usable for the TPC. Batch dispersion might be an issue

COTS – Reference Voltage Generators

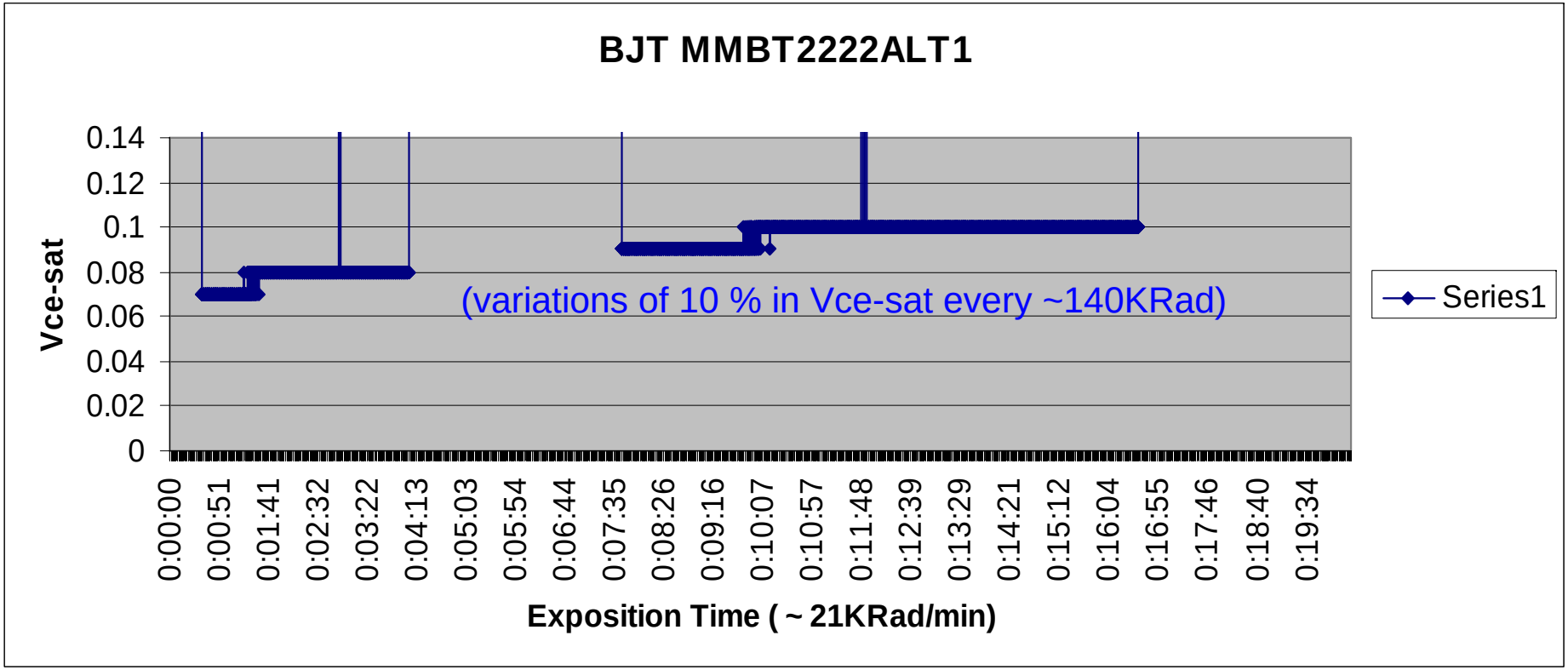




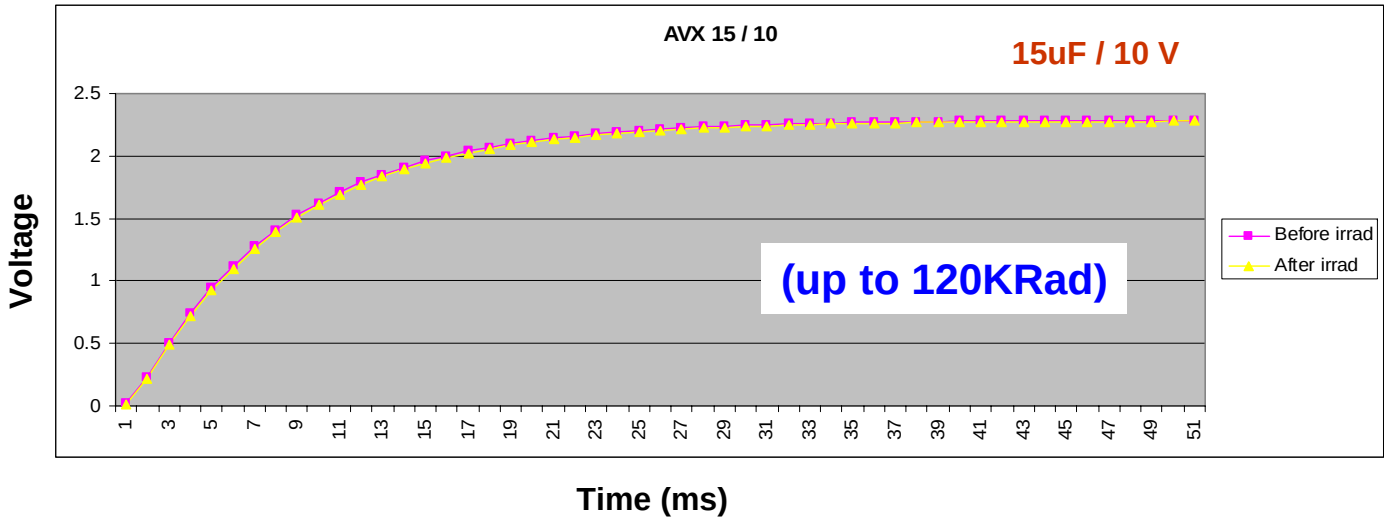
COTS – Operational Amplifier

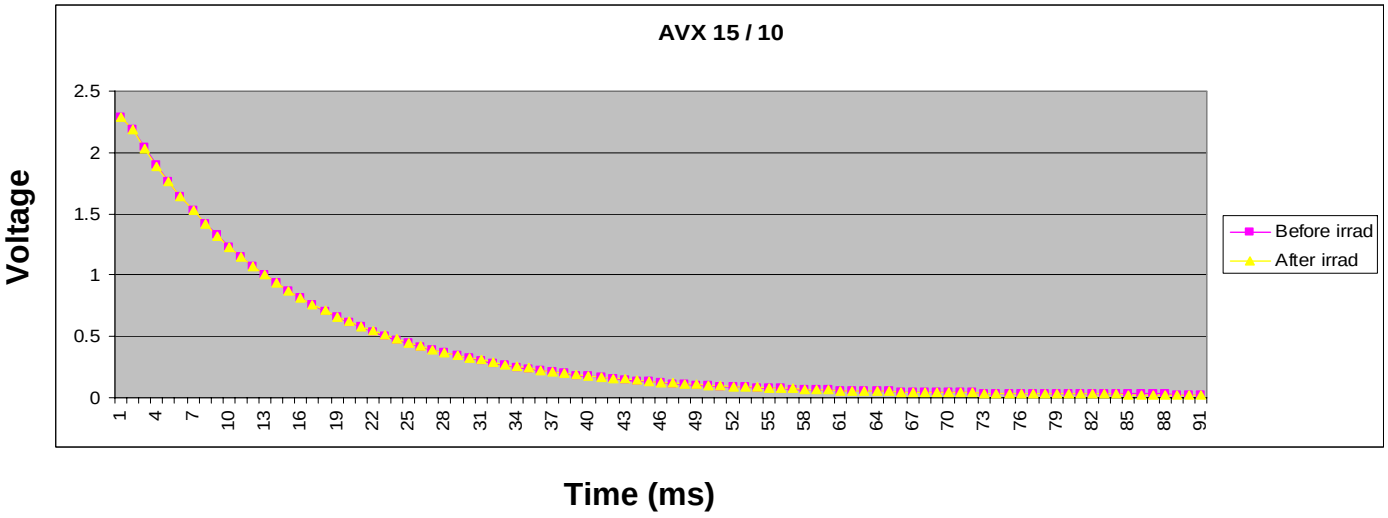


COTS – Bipolar Transistor



COTS – Tantalum Capacitors





COTS – Other Results

- **GTL16612** max TID > 80 krad SEU cross section $1.15 \cdot 10^{-12}$ cm^2 bit^{-1}
- **MPC9109** max TID > 50 krad SEU cross section $1.3 \cdot 10^{-12}$ cm^{-2} bit^{-1}
- **EPC1441** preserves configuration at TID > 20krad

COTS – FPGA (ACEX1K30)

TID is not a problem at the TPC levels

Two types of concern

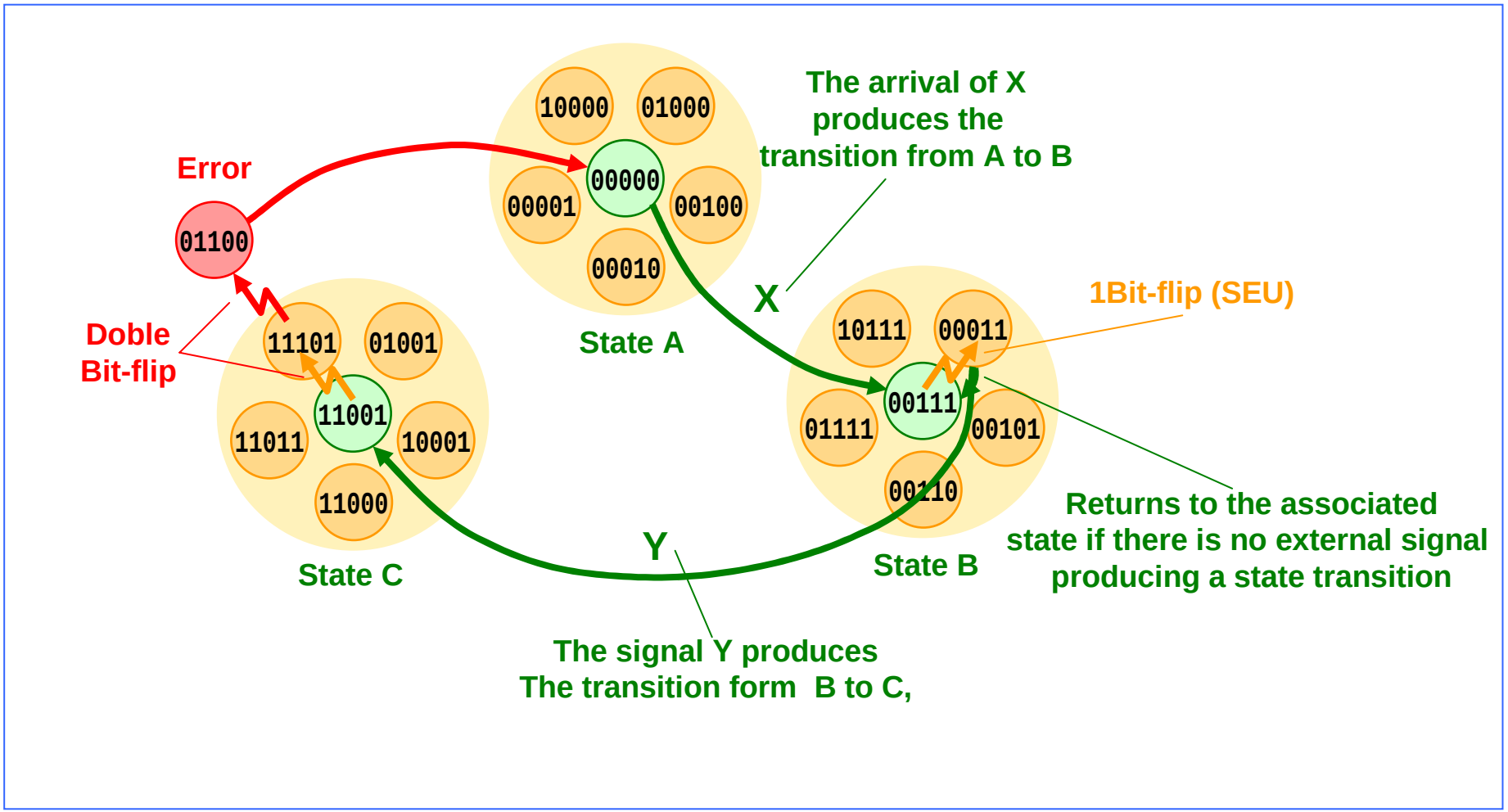
- Upsets in configuration SRAM cells
- Single bit-flips in register elements (can be avoided by design)

The ACEX1K30 offers no direct readout of configuration SRAM

- Indirectly detection of configuration upset through the internal logic

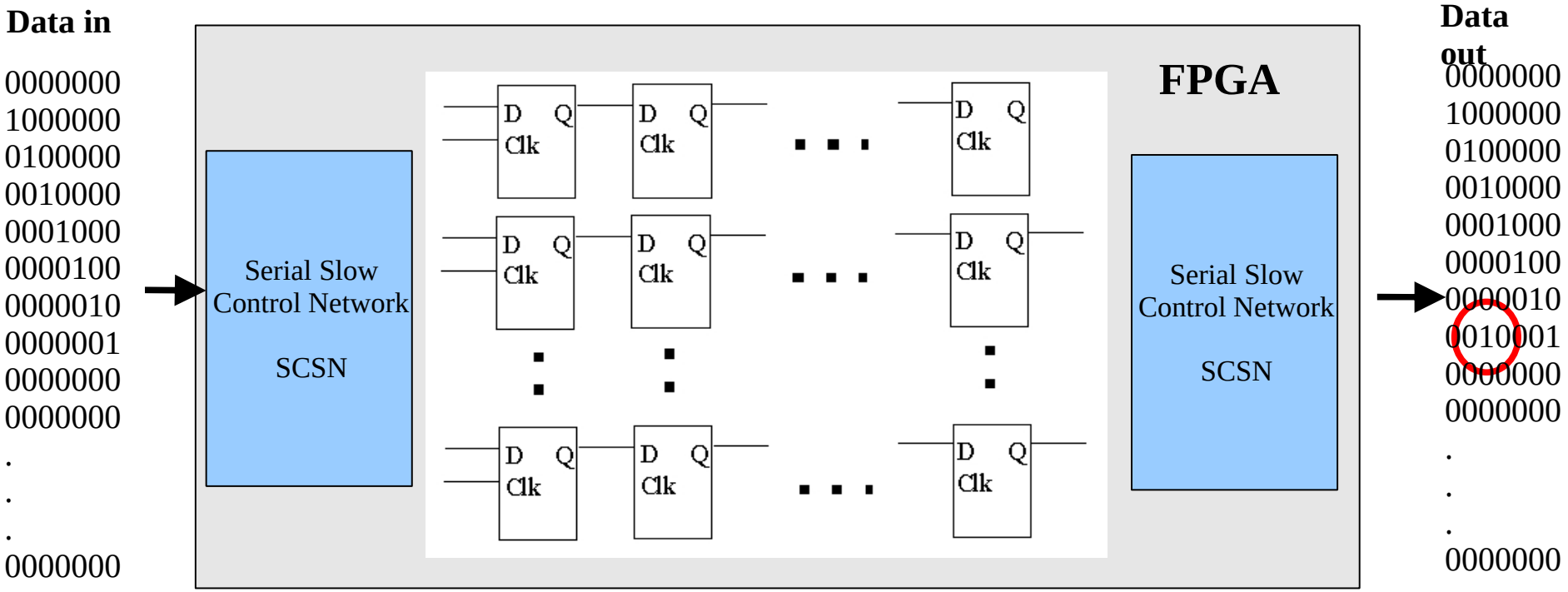
SEU Protection

- **Finite State Machine (FSM) protected by Hamming encoding**
  - **Basic principle**



Upset detection in ACEX devices

A fixed pattern is shifted through and compared for setups when read out.



COTS – FPGA (ACEX1K30)

Device	Conf. Bits	Cross Sec
ACEX1K30	**470 000**	**$4 \cdot 10^{-11}$ cm^2**

	Error rate per run (4 hours) per device	Error rate per run per system
FEC	$1.15 * 10^{-4}$	0.52

Detection of configuration loss by BIST

FPGA reconfigured by on board EPROM