

ALICE TPC Collaboration Meeting

Hardware and Software for the PASA Bulk Test

Status Update, Results and Open Issues

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Hard- and Software for the PASA Bulk Test

U.Bonnes TU Darmstadt

for Heidelberg TPC Meeting 12/13.02.2004

- Status
 - 17.600 packaged Chips from engineering run delivered to Darmstadt
 - 2400 Chips hand tested and 1600 good chips selected for delivery to Lund for FEC boards preproduction run
 - Hardware worked stable, second hardware available
 - Software improves during these tests
 - Test results and evaluation tools available
 - 38.000 packaged chips from production wafer run expected soon, delivered to Lund

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- Test results for 2400 chips
 - Error modes (87 chips, 3.6 %):
 - 14 chips: High current, supply voltage did not reached nominal value
 - 2 chips: High current, showing single channel error
 - 2 chips: High current, all channel within limits
 - 4 chips: Errors in all channels, probably problems with reference voltages
 - 2 chips: 2 channels off limits
 - 1 chip: 1 channel with high noise, all channels within limits
 - 1 chip: 1 channel with high noise and static pin voltage off limits
 - 61 chips: 1 channel gain off limits

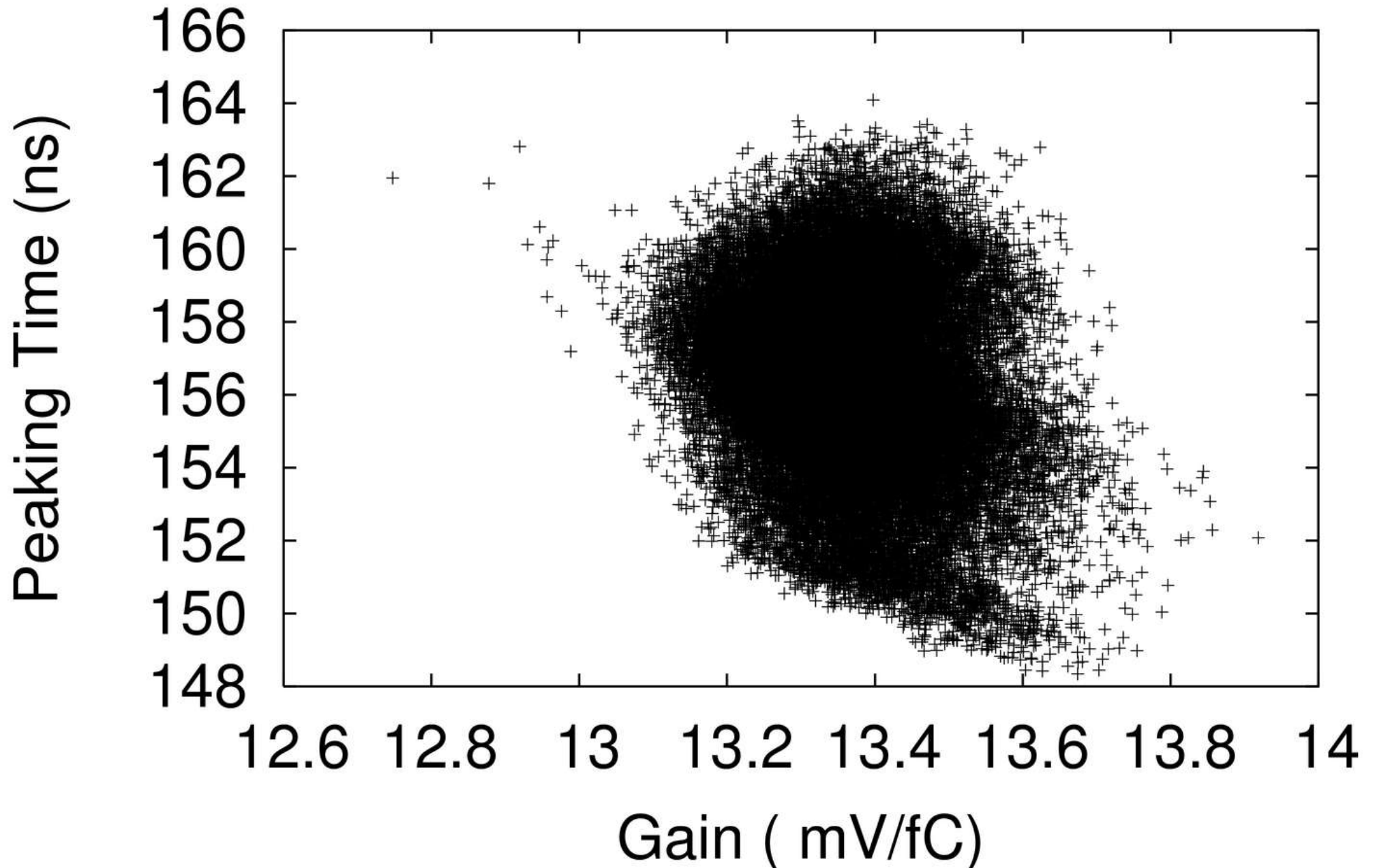
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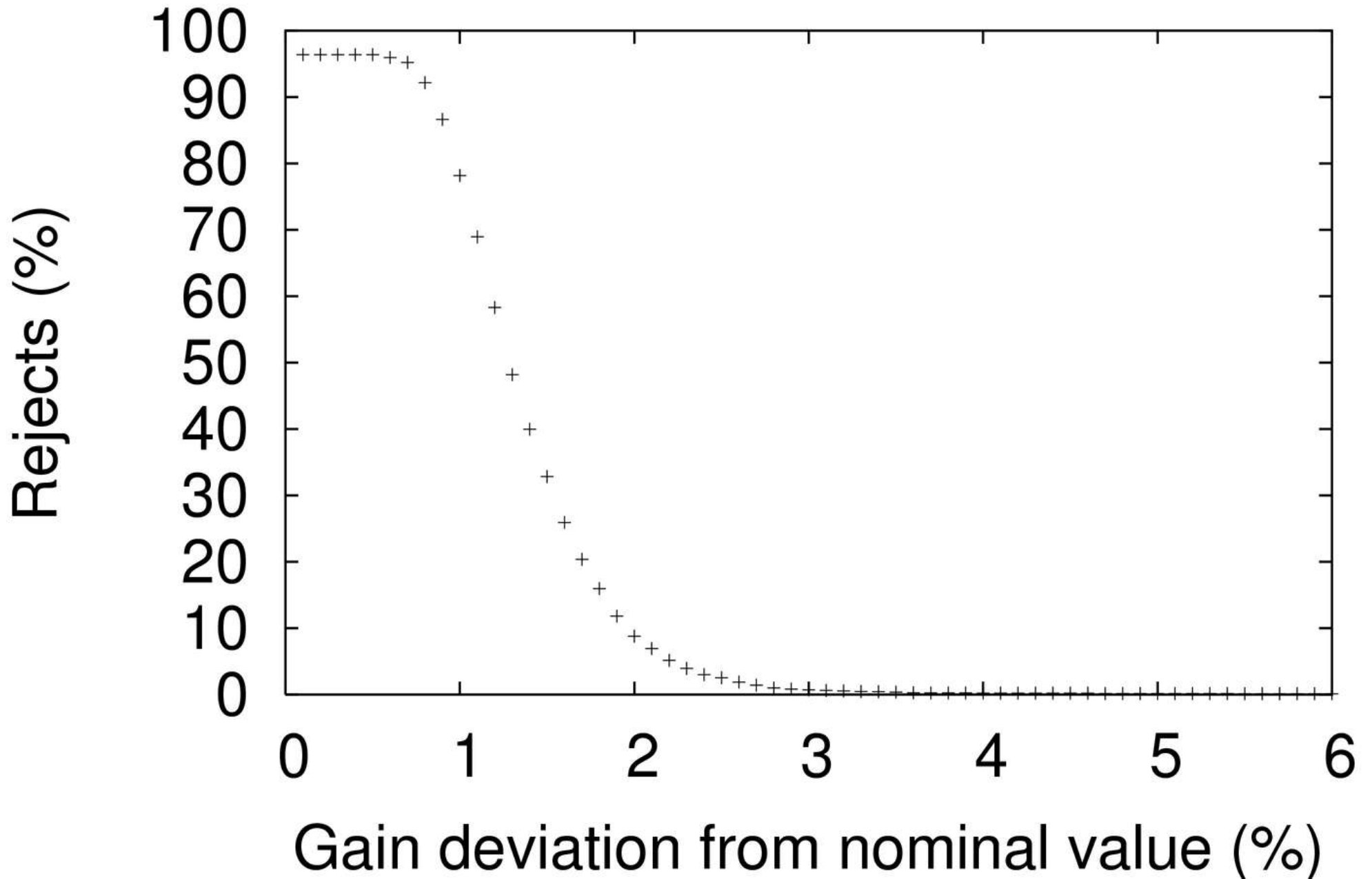
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- Test results (cont.)
 - Chips from at least two wafers, hopefully 4 wafers tested
 - Results from september test (600 chips) are similar
 - Chip/Chip and Wafer/Wafer parameter spread seems resonable
 - Gain versus Peaking time scatter plot
 - Rejects versus allowed gain deviation
 - Rejects versus allowed peaking time deviation
 - Output offset voltage distribution
 - Difference of Output offset voltage distribution inside chip
 - Rejects versus allowed output offset deviation

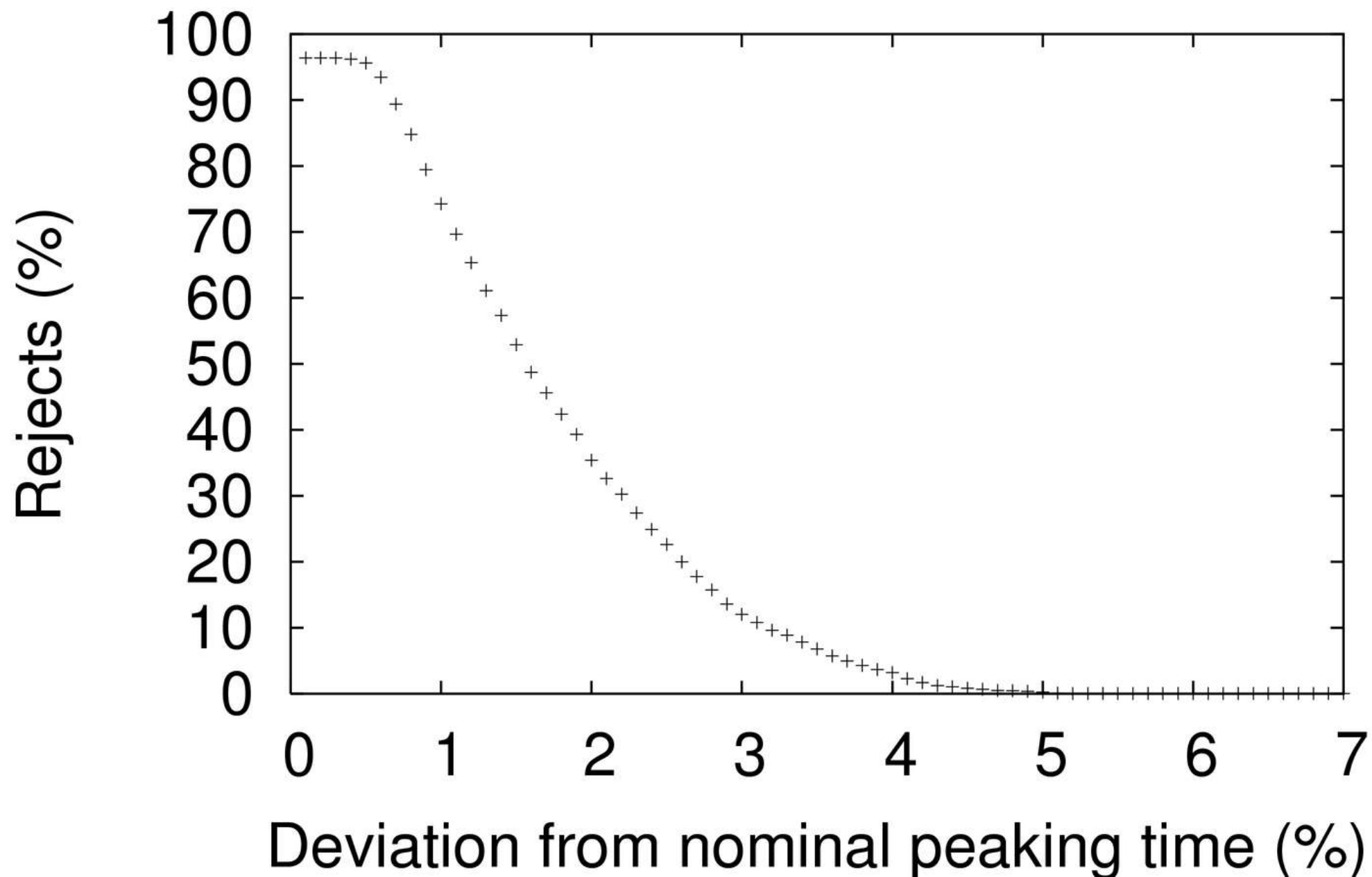
Gain versus Peaking Time



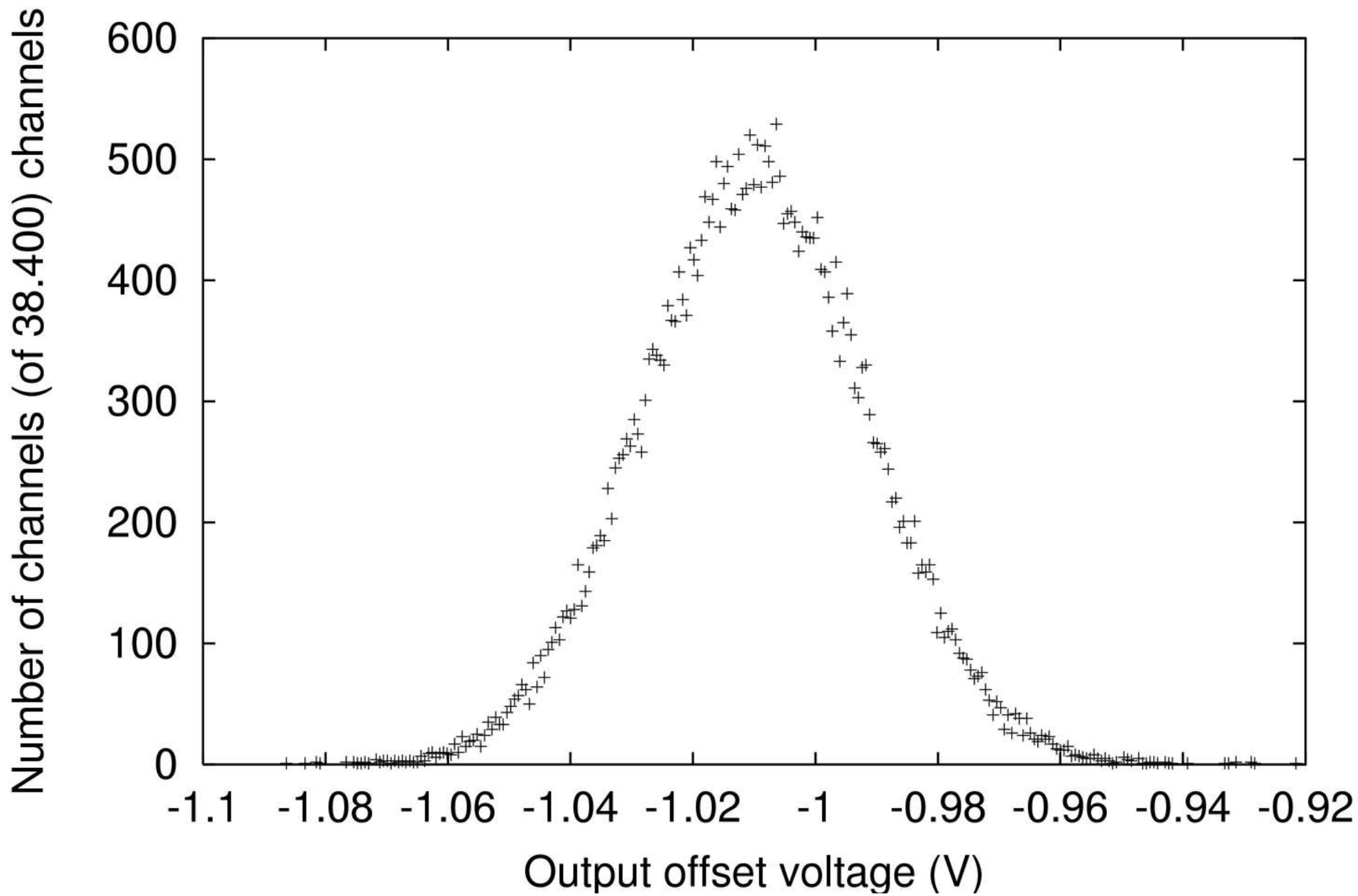
Rejects versus allowed Gain Deviation



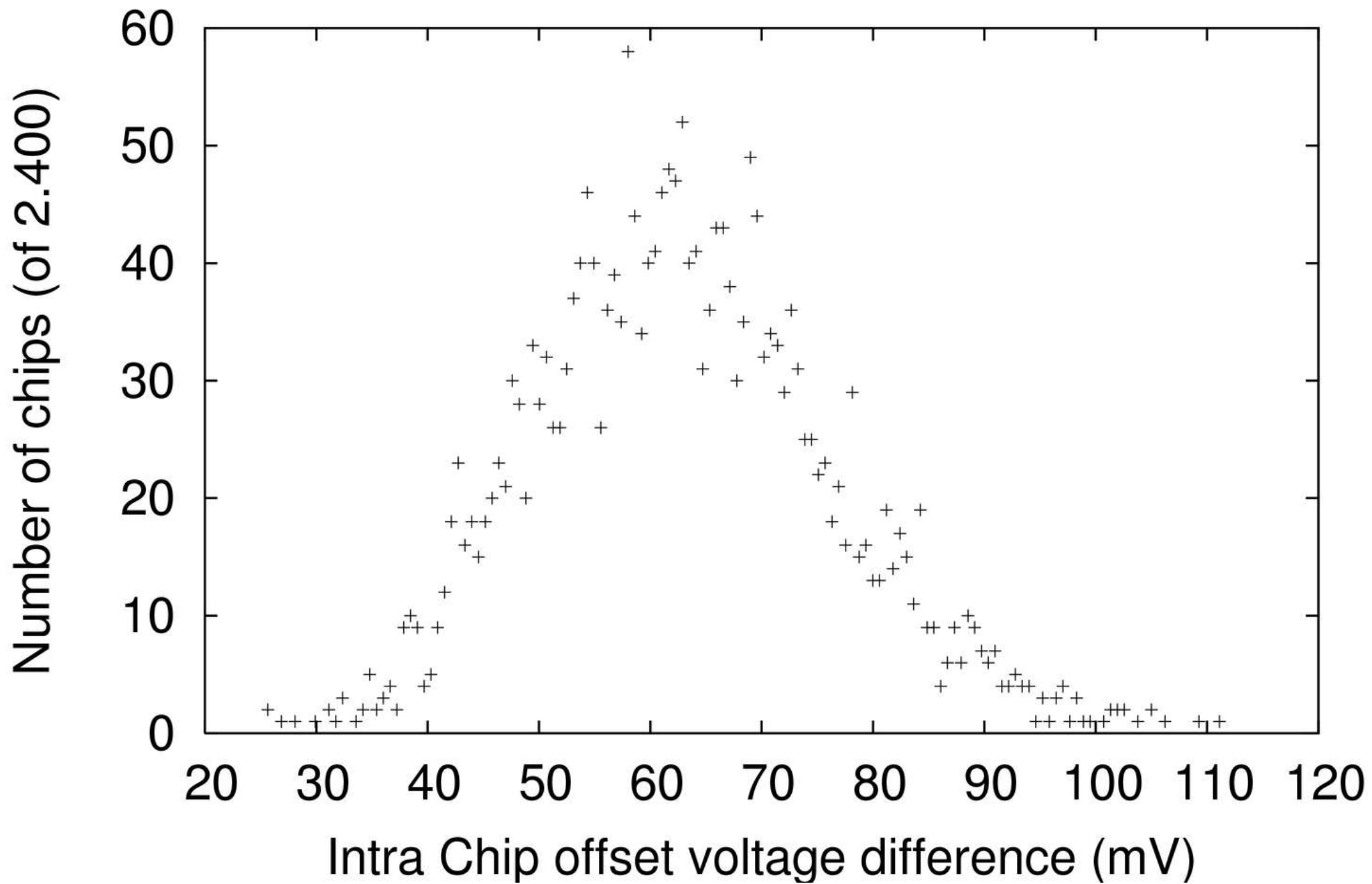
Rejects versus peaking time deviation



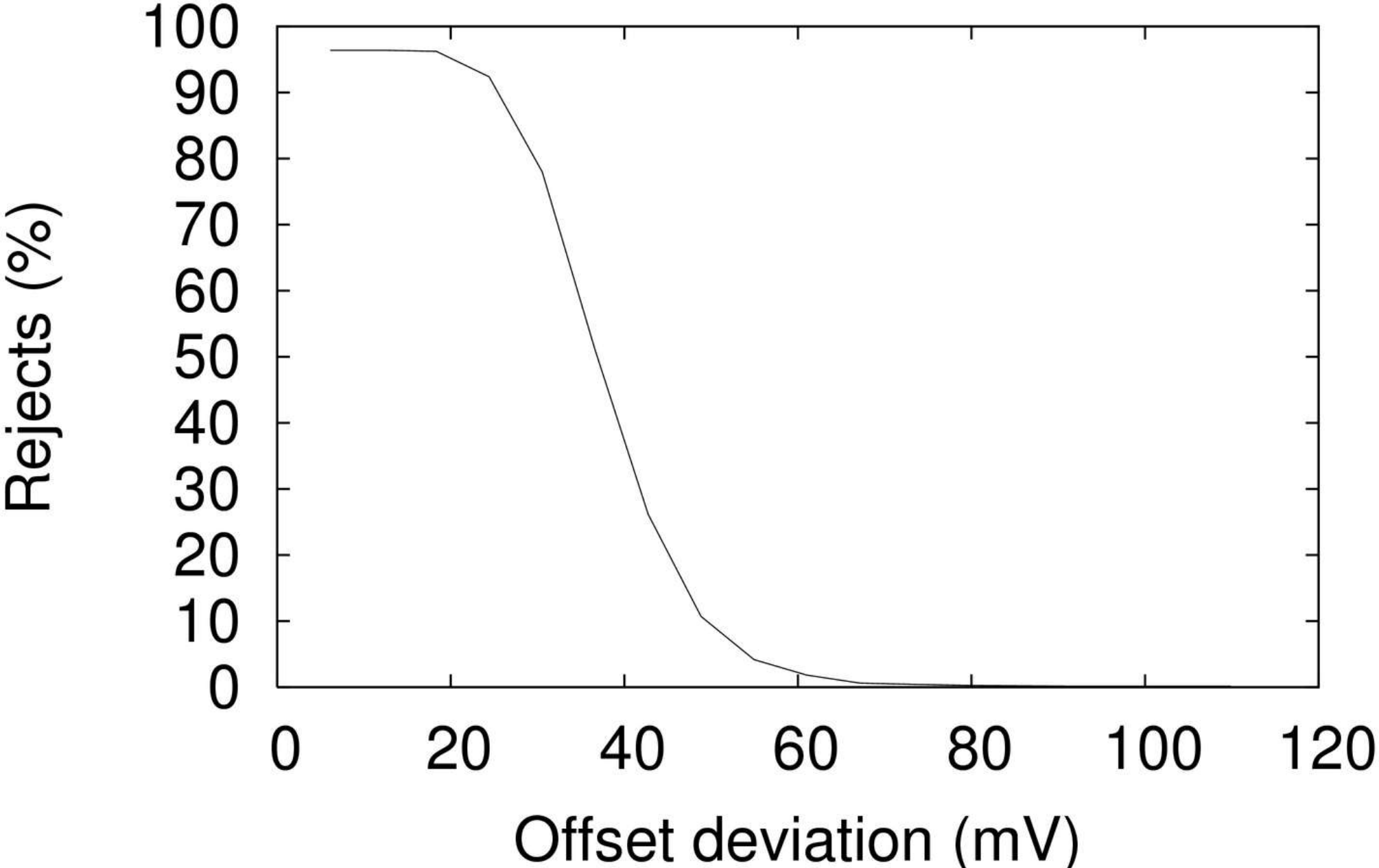
Output offset voltage distribution



Intra Chip offset voltage difference distribution



Rejects versus offset voltage



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- Test Results (cont.)
 - Channel to Channel deviation inside of one chip is in the order of the other deviations observed. Grouping therefore can not be done with sensible yield.
 - Mean values observed:
 - Gain 13.37 mV/fC (rel. value, abs. value is about 10 % lower)
 - Peaking time 156.4 ns
 - Offset -1.0095 mV
 - Socket/Chip contact is fragile, errors might be caused by bad contact and needs attention

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- Planning for bulk test
 - Use robot in Lund when available after(?) ALTRO test
 - 55.000 chips in 900 trays need to be tested
 - Each second per chips accounts for 2 working days
 - Each minute per tray change accounts for 2 working days
 - Test time for full test at 3 voltages now 15 second from before 30 seconds partly due to use of Intel C++ V8 compiler

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- Planning for bulk test (cont.)
 - Lund reports 15 seconds of time needed by the robot to change chips.
 - At least 60 working days needed with these numbers
 - Further improvements in test and chip change time should be considered
 - Use of open top socket with actuation by pressured air is evaluated, hopefully giving constant chip/socket contact
 - Test equipment will be transferred to Lund and set up, Test Software adapted to robot control

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- Open Issues and conclusions
 - Parameter for production wafer run need to be determined when packaged chips are available
 - What data from chip test and which format need to be archived?
 - Selection parameters need to be finalized
 - Functionality at minimum and maximum voltage is already tested. Should parameters at these voltage levels also be used for selection ?
 - Engineering run behaved quite well :-)

- Data Formats:

- One file for each chip at each voltage, one directory for each tray

- #VPASA IPASA VTOP ITOP VCM ICM VBOTTOM IBOTTOM
- 3307 2720 1560 2235 1060 949 561 440

- Offline sorting:

- Tray Chip ERROR Channel # Gain Peak
- 230 1 0# 0.08 +1.3% -0.2% 0.04 -0.8% -1.4% 81.7
- x 230 2 Vg N DX 1# 5.50 +2.8% -100.0% 0.11 +1.2% -0.6% 870.3

- Sum data:

- g 0 1 1 2869 2154 1052 441 550 1511 5.3543 6.0970 439.48 117.00 5.29
- g 0 1 2 2869 2154 1052 441 506 1529 5.3133 6.1216 352.85 136.30 3.21
- g 0 1 3 2869 2154 1052 441 553 1516 5.3502 6.1265 448.44 163.80 3.79
- g 0 1 4 2869 2154 1052 441 551 1546 5.3584 6.1054 393.62 168.50 3.60
- g 0 1 5 2869 2154 1052 441 536 1520 5.3427 6.1440 405.95 180.70 3.43

Distribution of peaking time

