

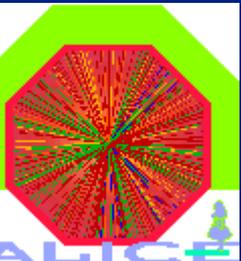
# Readout Control Unit Status

Overview

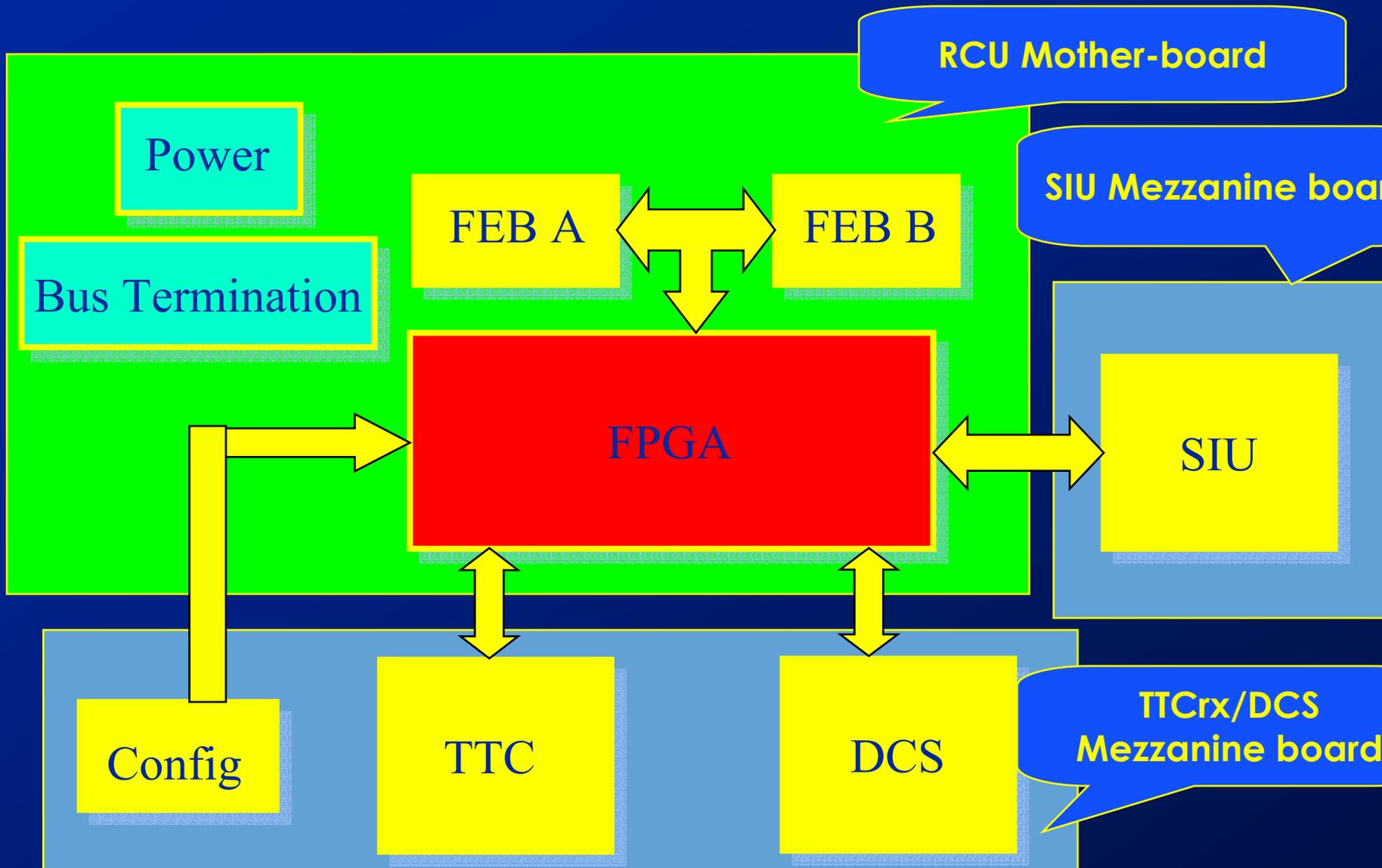
RCU card and sub-cards

Status of different modules/tasks

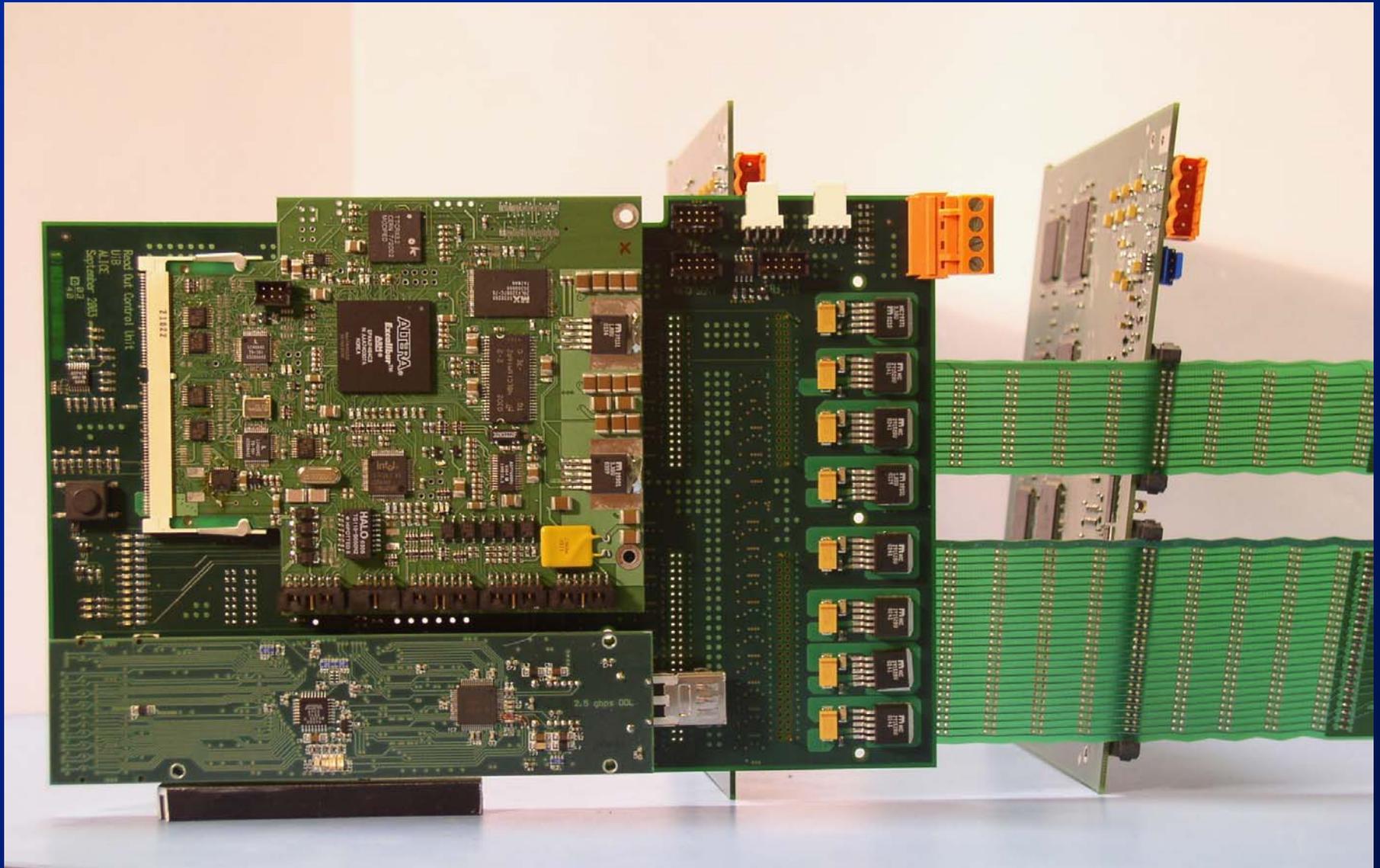
Milestones



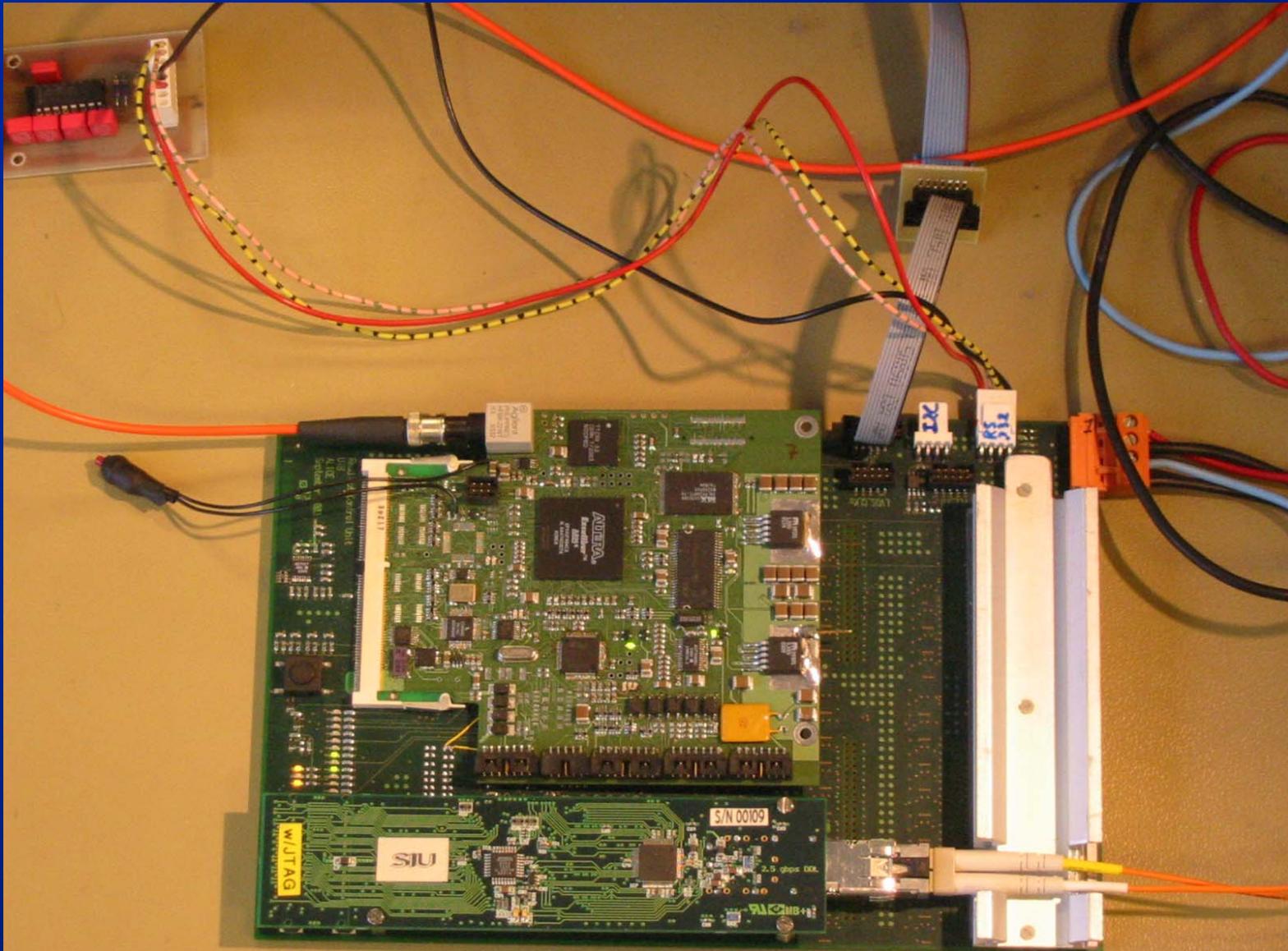
# RCU Main Building Blocks Implementation



# RCU card with FEC



# RCU Board in the Lab



# RCU-design Web Page

FEC - Microsoft Internet Explorer

Datei Bearbeiten Ansicht Favoriten Extras ?

Zurück Zurück Suchen Favoriten Medien Wechseln zu Links

Adresse D:\rcu\index.htm

## Read out Control Unit

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Read out Control Unit (revision 1.1 - Oct '03)

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- Components numbering top ([pdf](#))
- Components numbering botom ([pdf](#))
- Pinning table EP20K200EFL-BGA672 (generated from Capture Cis) ([xls](#))
- More to come
- PCB GERBER files ()

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Picture of the PCB

# Internal RCU Bus - Revised

- **BUS Master Interface**

clock        1    --> bus clock

rst\_n        1    --> bus reset

b\_addr      16   --> address

b\_data      32   <-> data

b\_RnW       1    --> Read/Write : 1=Read/0=Write

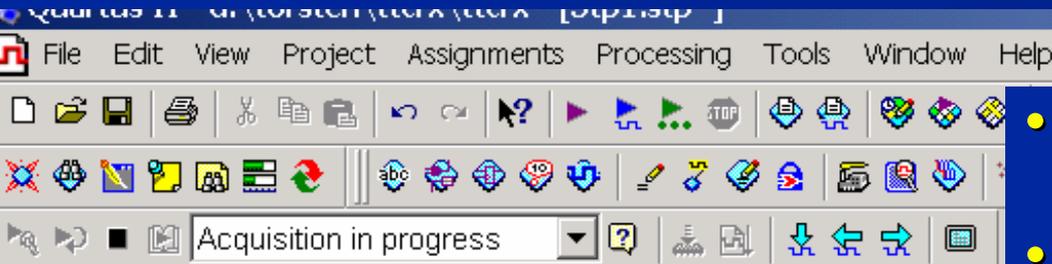
b\_cstb\_n    1    --> Common Strobe: master indicates valid address/data

b\_ack\_n     1    <-- Acknowledge: target indicates valid transaction

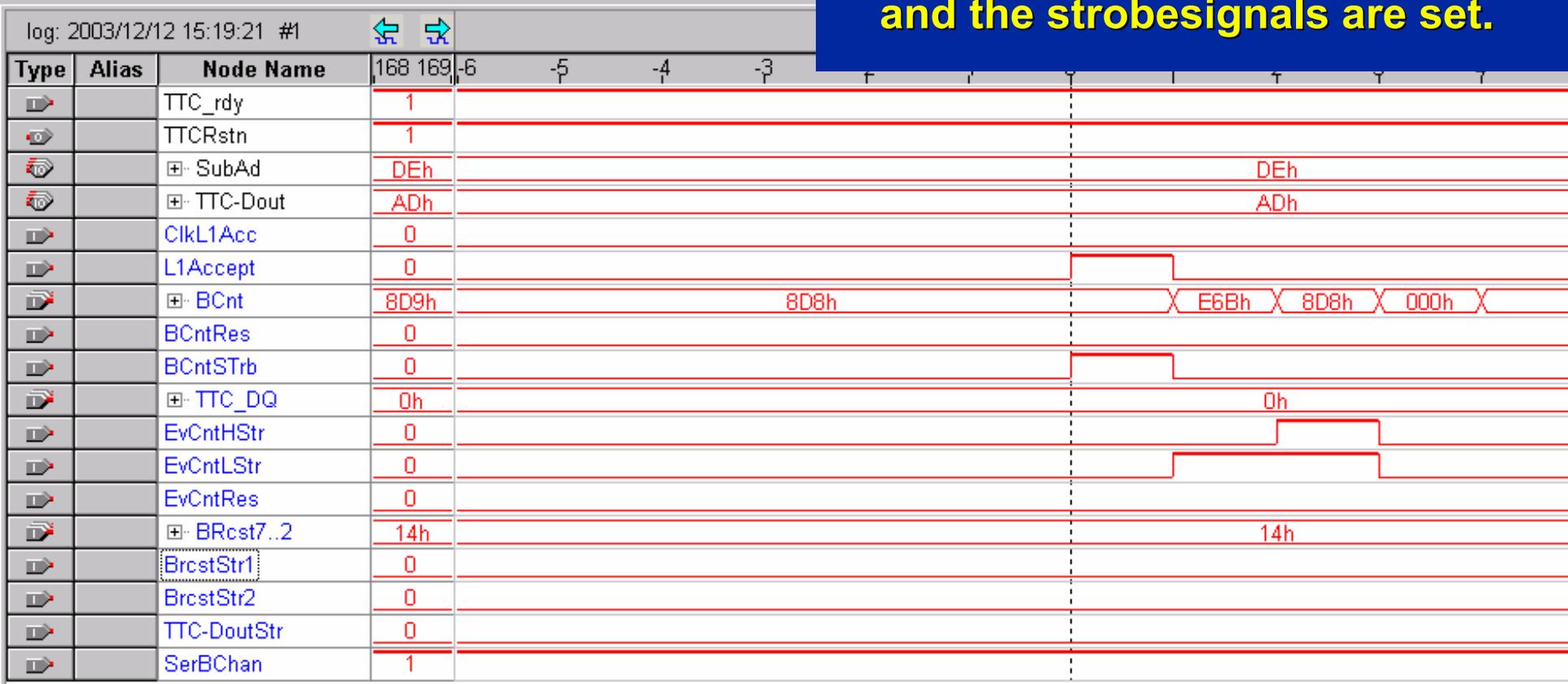
# External Communication

- RCU <-> DCS      DIM Server Client Scheme over ethernet
- RCU <-> Trigger    VME based test setup
- SIU <-> DIU        pRORC based Test setup
- RCU <-> FEC        Front End Card Interface

# TTCrx



- A snapshot of a L1Accept by the TTCrx.
- The Counters are incremented and the strobesignals are set.



# TTCrx

log: 2003/12/12 15:09:12 #0

Type	Alias	Node Name	168	169	-32	-16	0	16	32	48	64	80	96	112	128
		TTC_rdy	1												
		TTCRstn	1												
		SubAd	AFh		34h									AFh	
		TTC-Dout	FEh		89h									FEh	
		ClkL1Acc	0												
		L1Accept	0												
		BCnt	7D7h										7D7h		
		BCntRes	0												
		BCntSTRb	0												
		TTC_DQ	0h										0h		
		EvCntHStr	0												
		EvCntLStr	0												
		EvCntRes	0												
		BRcst7..2	14h										14h		
		BrcstStr1	0												
		BrcstStr2	0												
		TTC-DoutStr	0												
		SerBChan	1												

Data Setup

starmvm2600 - vme - SSH Secure Shell

File Edit View Window Help

Quick Connect Profiles

```
Enter number [0..14]: 13
short      [0..1]: 0
address    [00000000..000003fff]: 35FC
external   [0..1]: 1
sub-address [00000000..000000fff]: AF
data       [00000000..000000fff]: FE

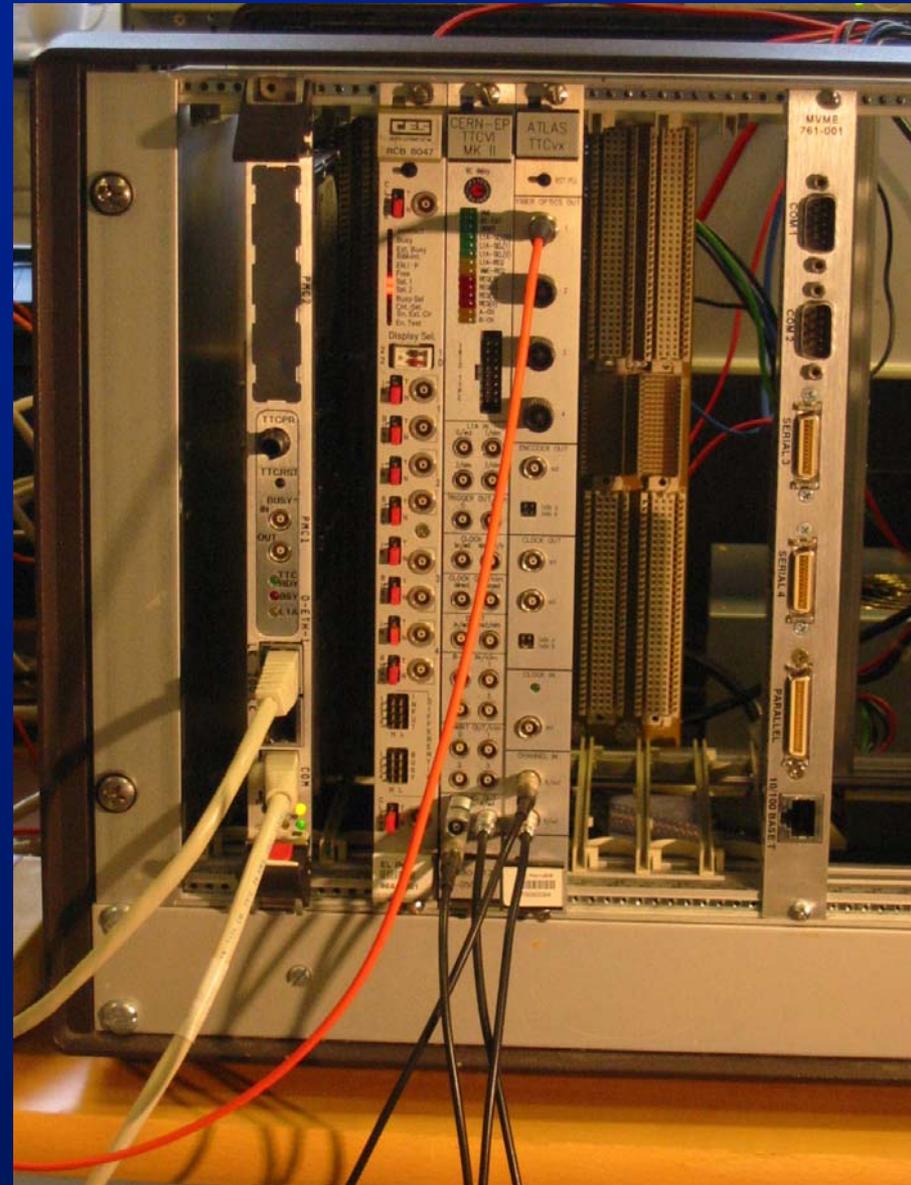
send asynchronous command returns 0
```

Connected to starmvm2600

- An individual Address Command (IAC) sent to the chip.
- The data is received by the chip and put to the outgoing lines.

# RCU <-> Trigger

- **VME based test setup:**
  - VP 110 CPU board running LINUX
  - TTCvi, TTCvx
- **TTCrx chip communication has been tested successfully**

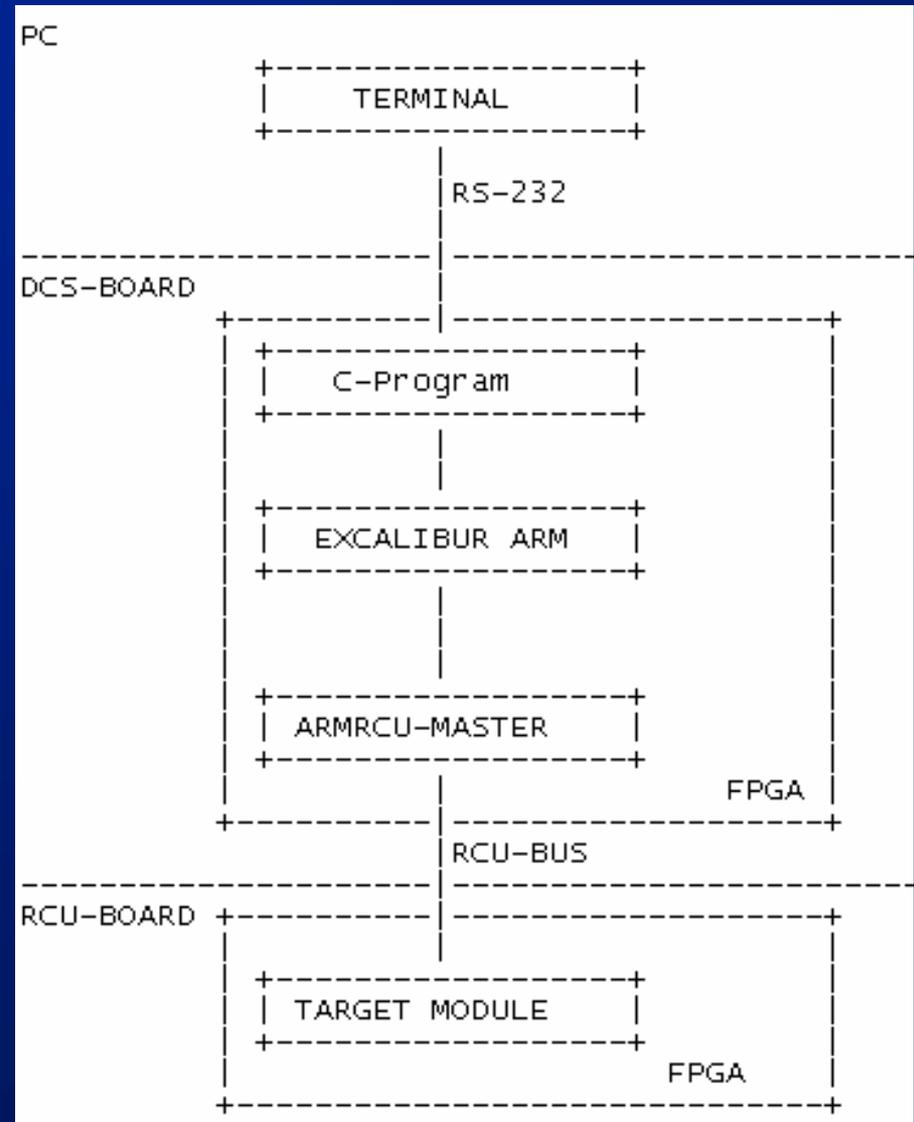


# RCU <-> DiU

- **pRORC based Test setup**
- **The Data Assembler Module also contains a pattern generator**
- **The PG can be configured and started by writing to the command register**
- **Bidirectional functionality implemented**
- **Has been successfully tested with the SIU-DIU link**

# A simple RCU module debugging environment

- The ARMRCU design provides a simple interface to enable the user to test RCU target modules.
- Based on the Excalibur ARM connected to a RCU master module.
- A simple C-program makes it possible to execute RCU bus transactions as reading and writing from/to a RCU target module.
- Altera SignalTap is used to capture and store signal activity from any internal device node



# RCU Board Final Layout

DDL fiber

RCU Mother board  
W=appr. 250 mm  
H=max 143 mm

TTCrx fiber

SIU

W=150mm  
H=37mm

DCS

W=Max appr. 150 mm  
H=MAX 90 mm



# Milestones

- **Milestones:**
    - **Radiation tests:**
      - Oslo Cyclotron  
Uppsala TSL
    - **Final PCB Layout:**
    - **Partial System Integration**
    - **Beam Test (3 RCUs)**
    - **Qualification of the final design**
    - **Production of the final prototype**
- Ongoing**  
**Next Beam Time - March 2004**  
**Next Beam Time - March 2004**  
**June 2004**  
**March 2004**  
**May 2004**  
**October 2003-May 2004**  
**June 2004-July 2004**



# Open issues

- Migration to Actel