

ALICE Club 2005

The TPC Front End Electronics – Progress report

Roberto Campagnolo – CERN Ph-Ed

TPC FEE Collaboration:

- Bergen
- CERN
- Darmstadt
- Frankfurt
- Heidelberg
- Lund



Alice

Outline

The ALICE TPC Front End Electronics

Progress overview of the main components :

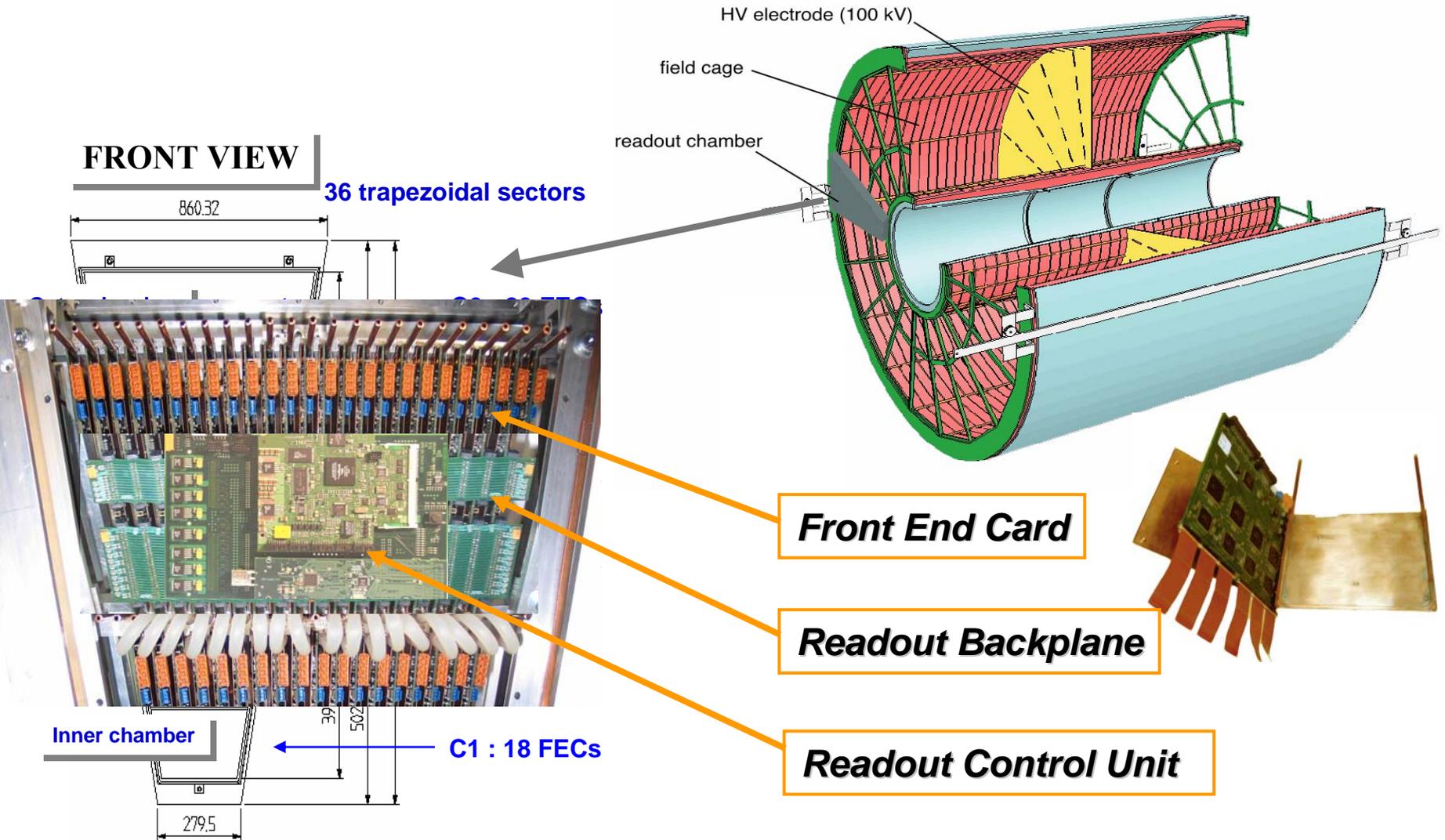
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 - Shaping Amplifier (PASA)
 - Digitizer and digital processor (ALTRO)
 - Board Controller
- Readout and Control Backplane
- Readout Control Unit (RCU)
 - Functions and performance
 - FPGA - radiation strategy
 - Prototyping status

Integration with the Detector :

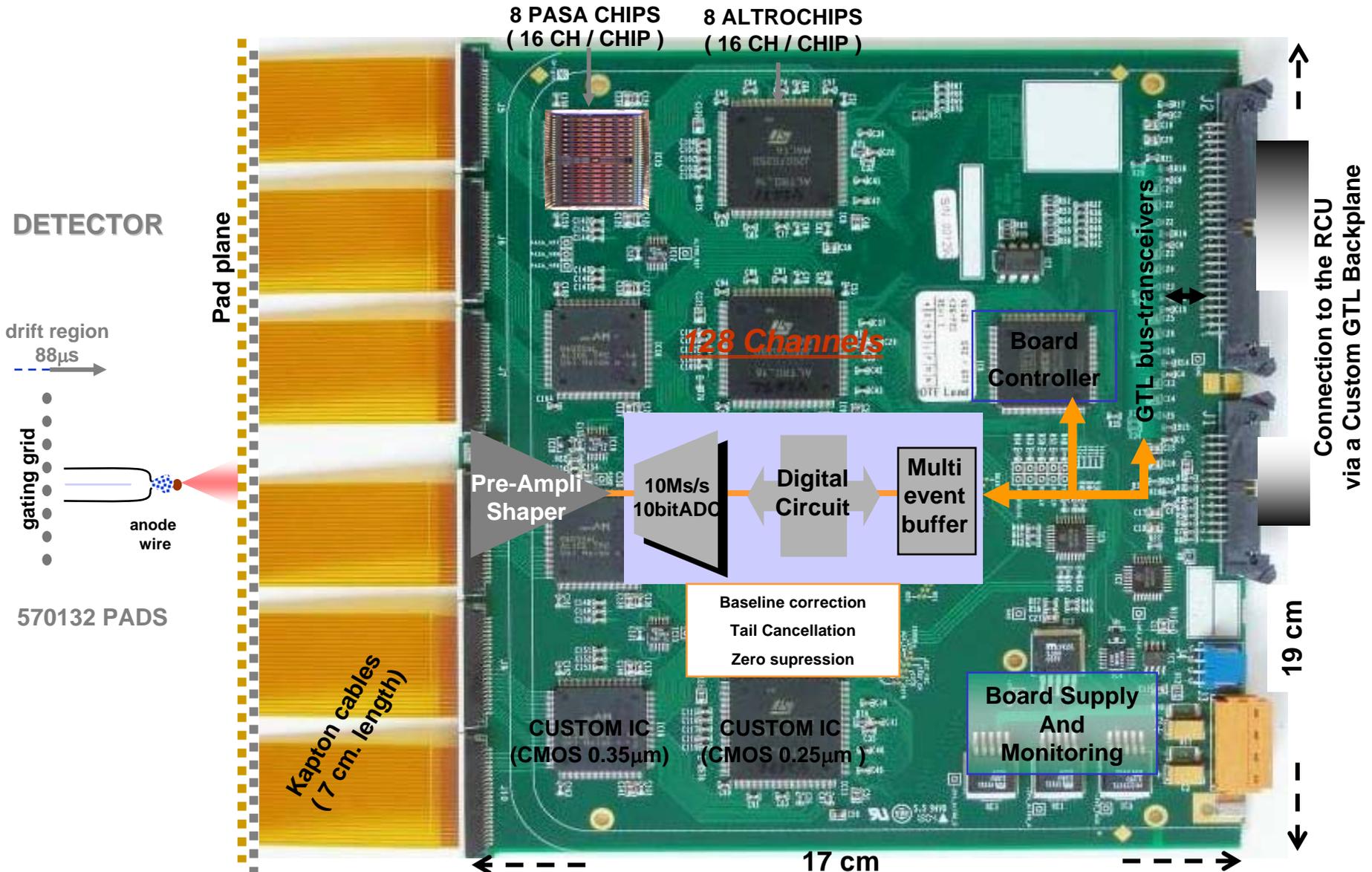
- TPC Field Cage prototype in hall 167
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Conclusions and future work

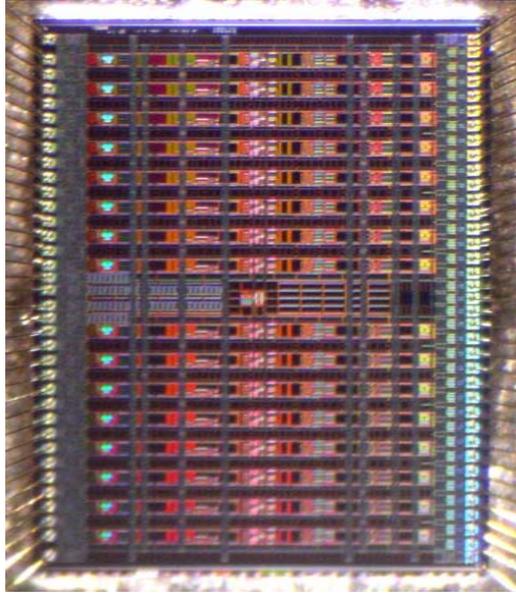
ALICE TPC readout components



Front End Card Overview 1/3



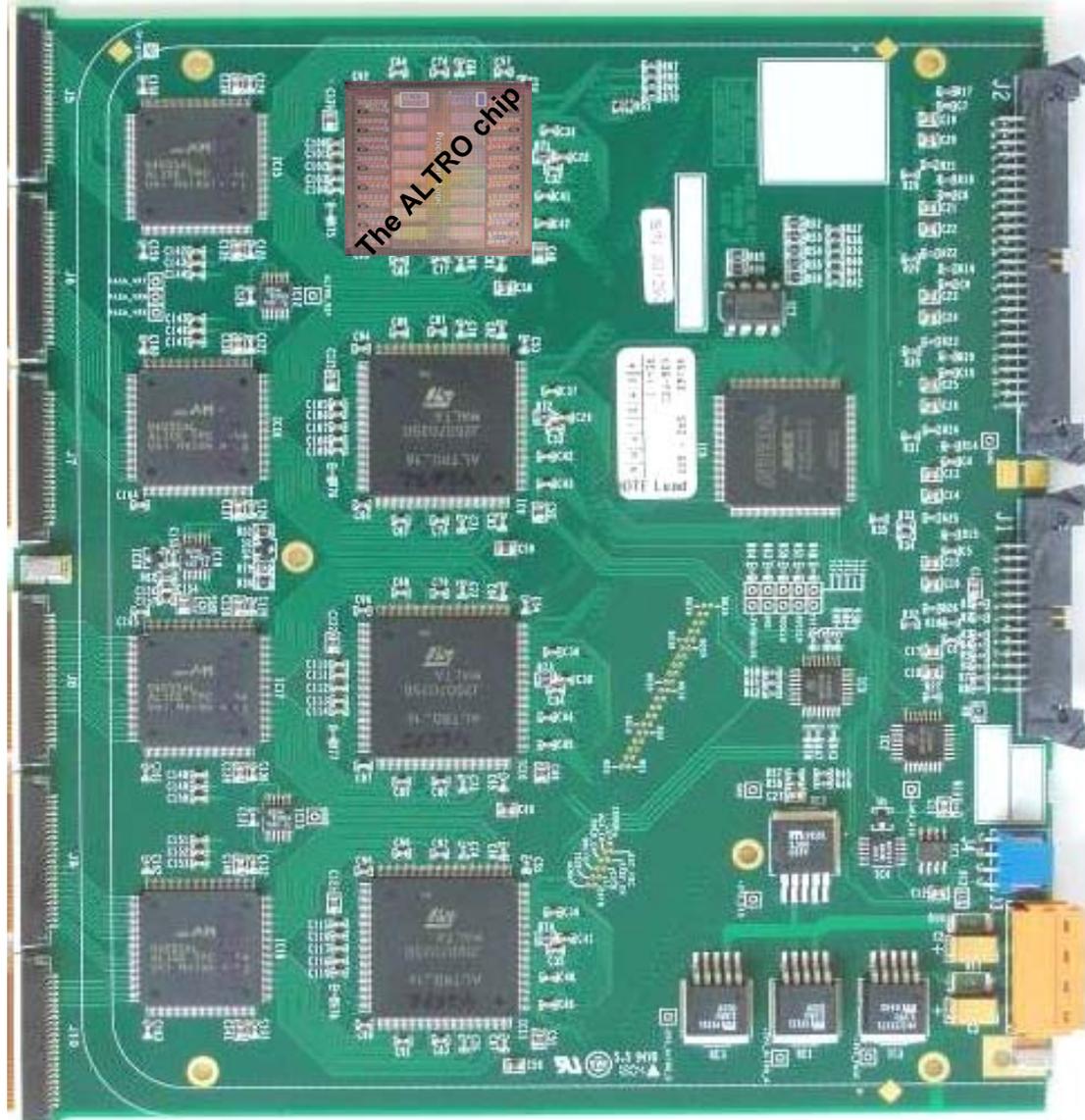
PASA Production and Test Summary



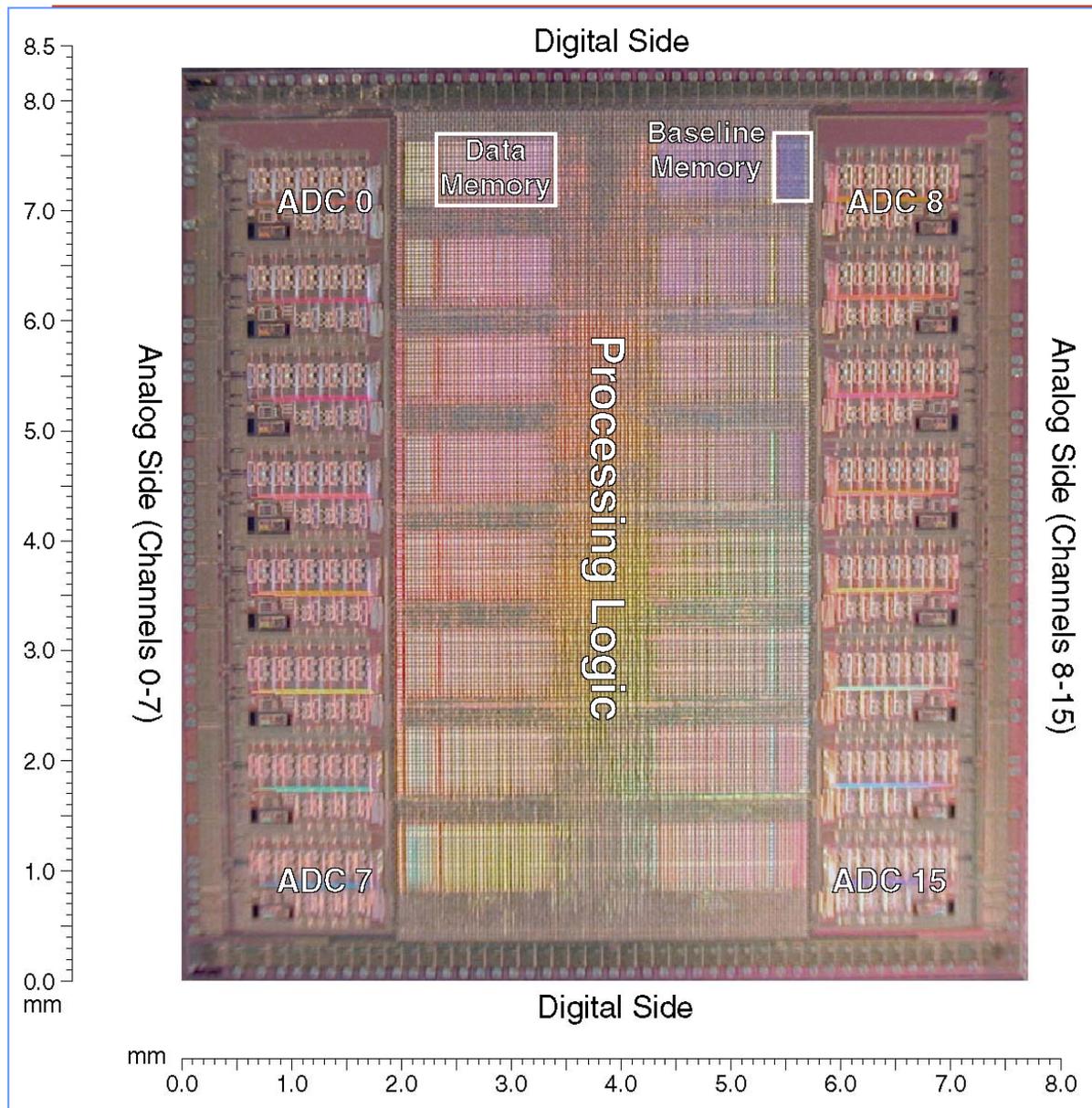
- Noise: 560e (12pF)
- Conversion gain: 12mV / fC
- Shaping time: 188ns
- Power consumption: 11mW / ch

- process: AMS CMOS 0.35 μ m
- area: 18 mm²
- ER samples (500 chips): Sep '03
- full delivery (49359 chips): Jan '04
- Completion of mass test: Jun '04
- yield (working chips): 94%
- Yield: 83% |CG| < 5%, |PT| < 5%, |BSL| < 5%

Front End Card Overview 2/3



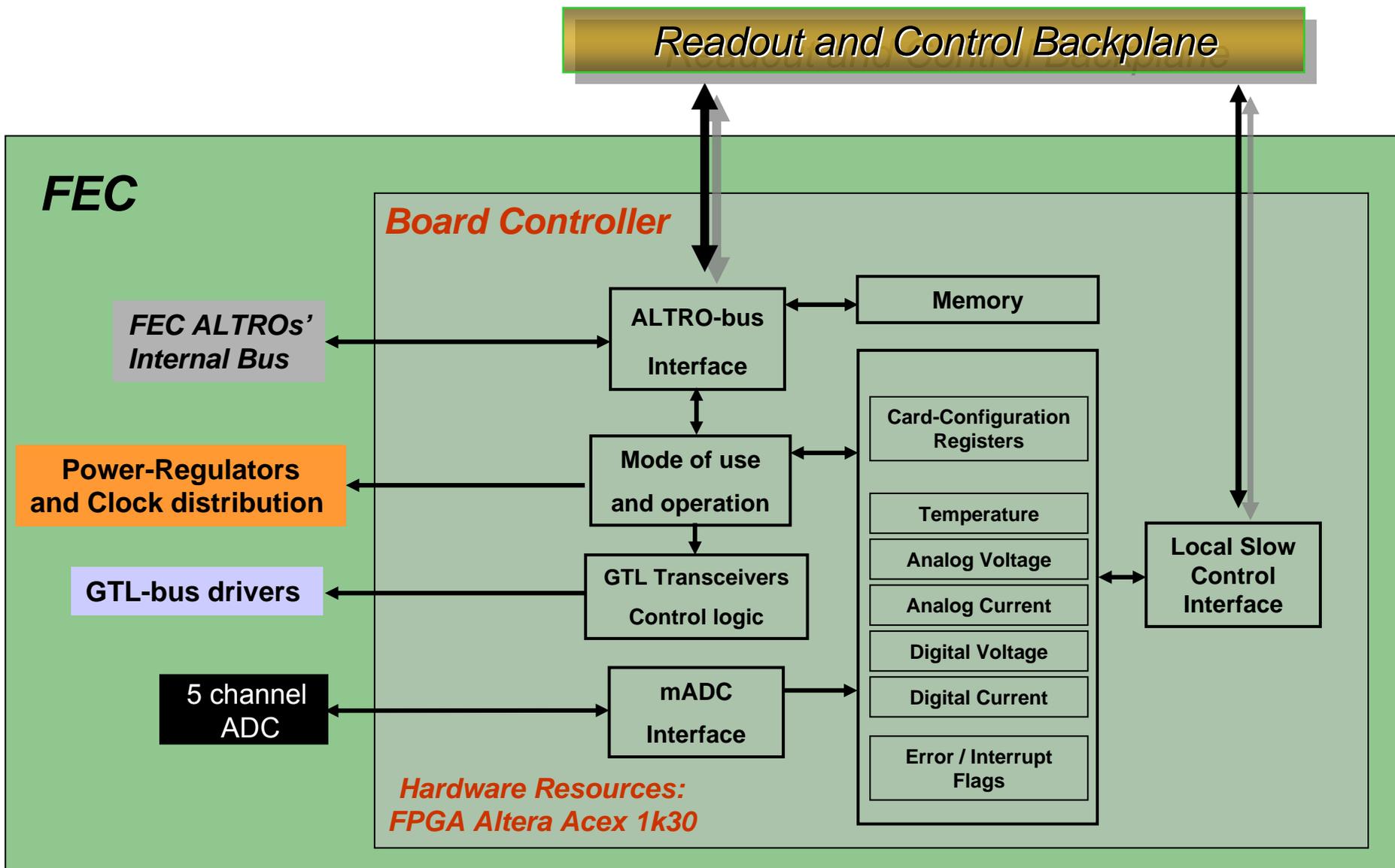
ALTRO Production and Test Summary



Process	HCMOS-7 (0.25 μm)
Area	64 mm²
Transistors	6 millions
Embedded memory	800 kbit
ENOB	9.7
Power	16mW / channel

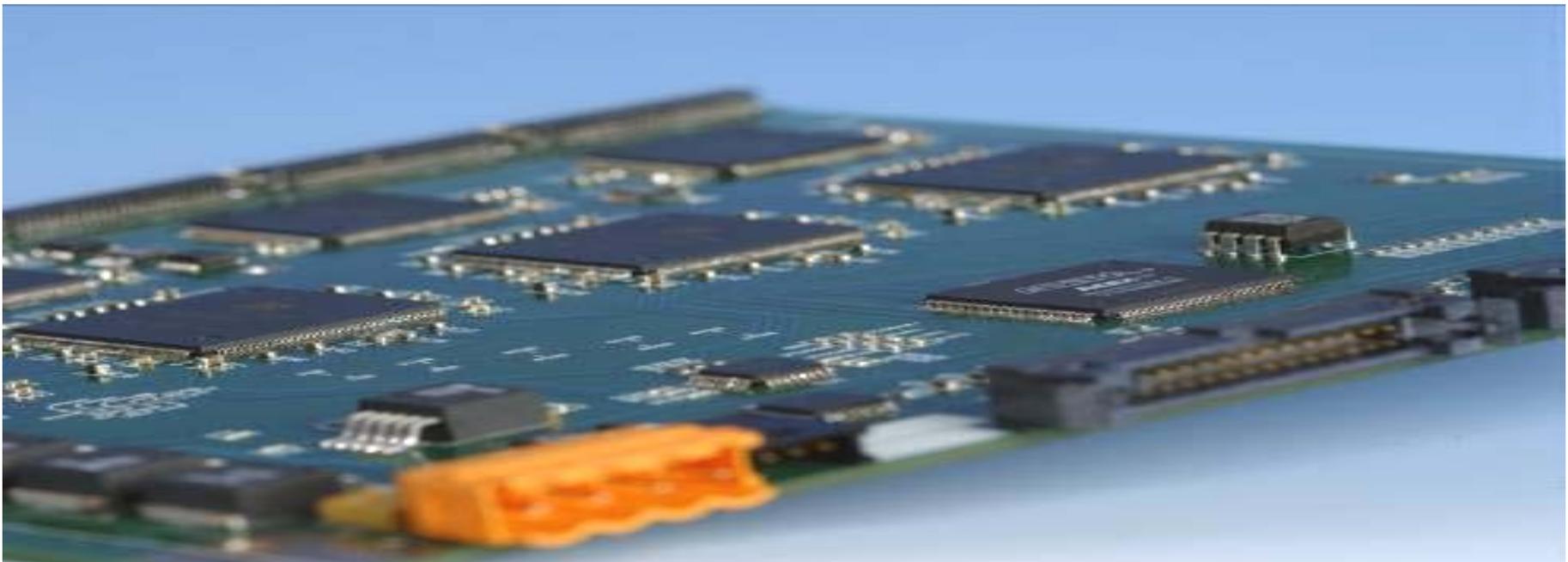
ER (4K chips)	Apr '02
Mass prod. (44K chips)	Dec '02
Mass test	Aug '04
Yield	84%

The Board Controller logic



Alice TPC FEE

The Front End Card Mass Production and Test – Status Report



FEC Mass Production summary

□ Production of 4800 FEC

- Contract signed in Dec '03 (Note-Xperi @ Lund)
- Pre-series of 50 boards with good quality (Feb '04)
- Pre-series of 200 boards (May '04)
- Full production started in Oct '04
 - Reached a production rate up-to 400 boards/week with 2100 boards delivered so far
 - Production quality is surveyed at CERN by testing 5x lots of 50 boards (5% of the full production)
 - 2 lots received and tested @ CERN : Yield > 90%

FEC Mass Production Tests Summary

Test sites

- **Frankfurt** (mass test), and **CERN** (production quality survey)

Test Procedure

- Verification of the supply voltages and currents
- Combination of the PASA and ALTRO tests
- Test of FPGA, Readout and Control Network interfaces
- All information stored in the ALICE Detector Construction Database

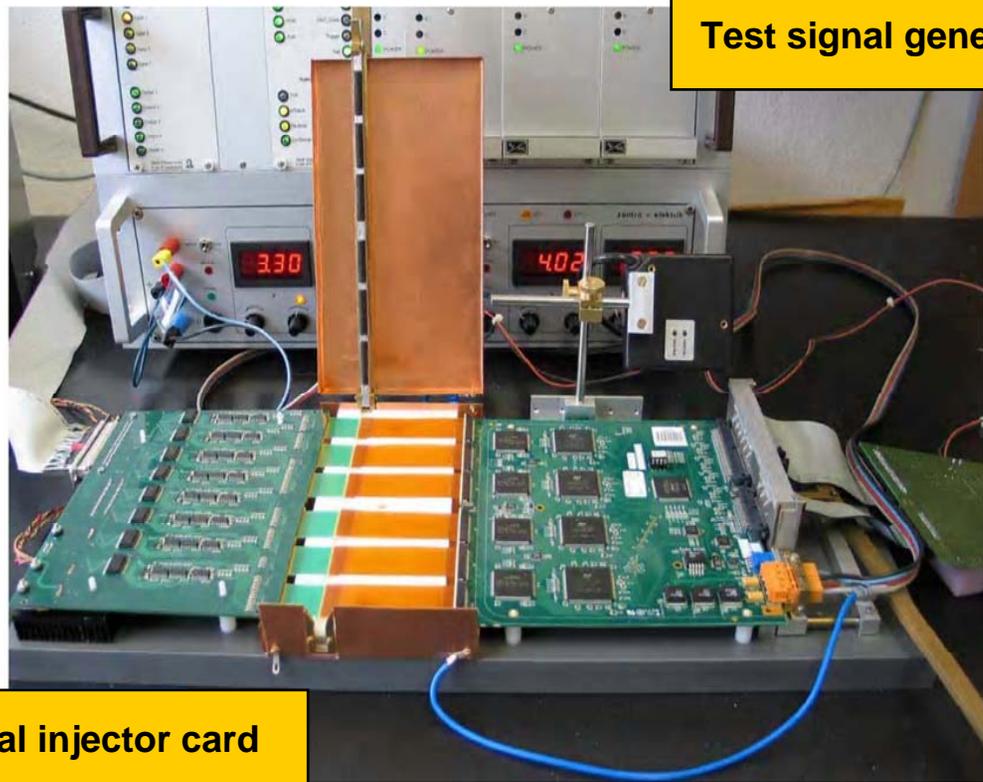
Status

- **Hardware:** test bench and test procedures (semi-automatic) **fully operational**
- **Software:** Control, Acquisition and Analysis - **ready**
- **Projected test rate:** 80 boards / dd → 1600 boards / mm
- **Starting from end of February → Full mass test completion by April 2005**

FEC Mass Test – Card Tester in Frankfurt



Kapton insertion tool



Test signal generator

Signal injector card

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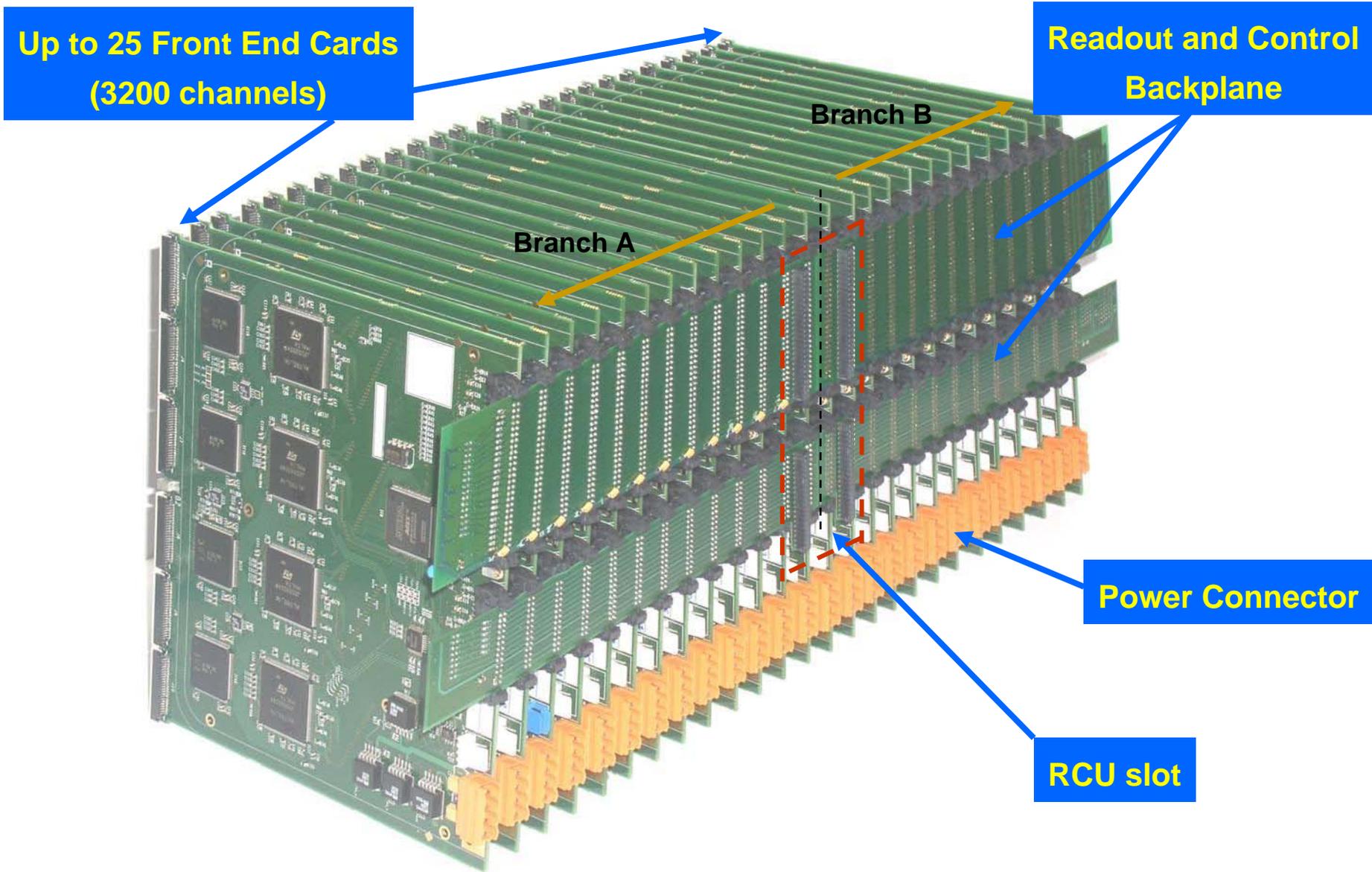
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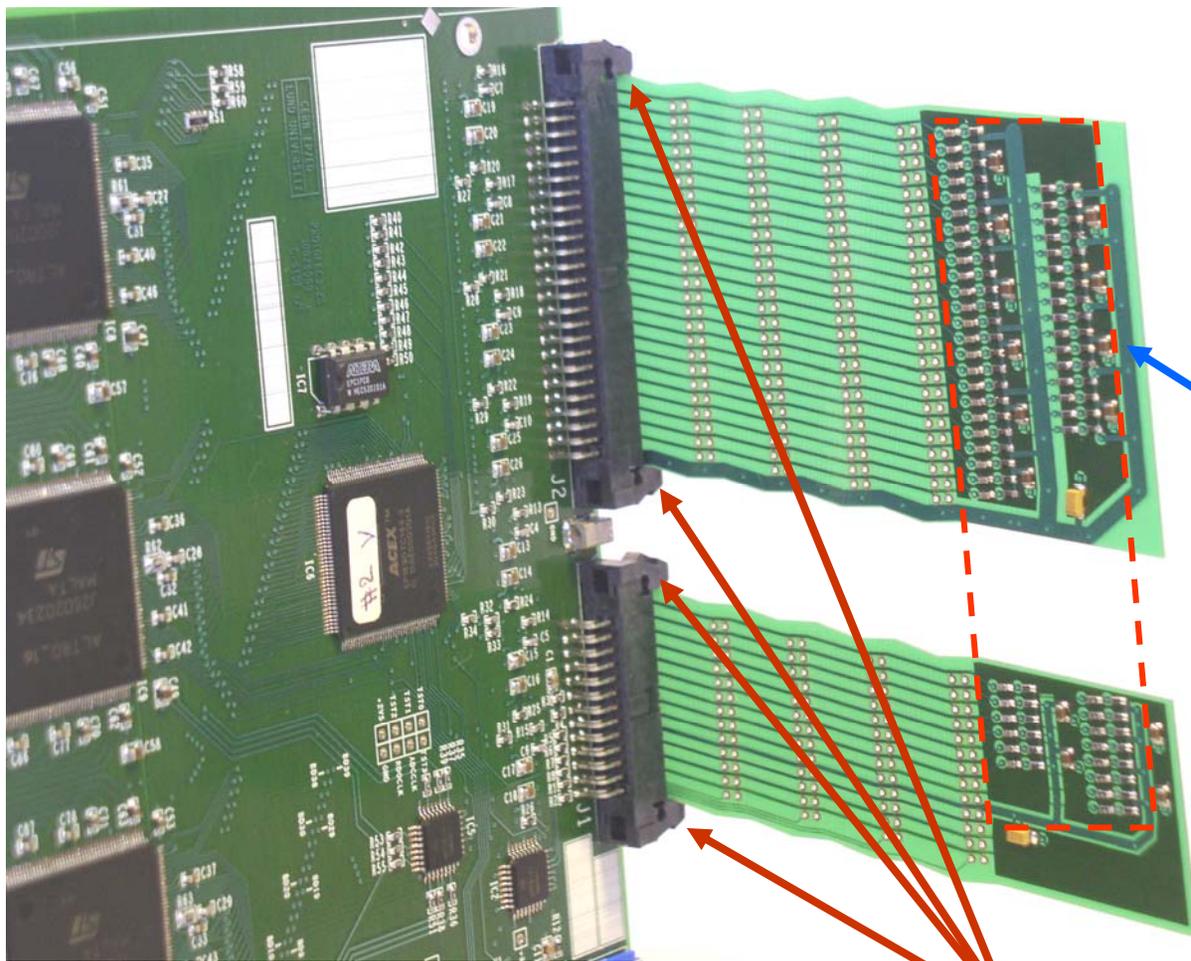
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Conclusions and future work

Readout Backplane – example of readout partition



Readout Backplane - Electrical and Mechanical details



Technology :
4 Layers , Class 4 PCB
(4 x 35 μ m Cu + 3 x 200 μ m FR4)

**service card integrated
in the backplane**

**FECs SIDE
Connectors' Locking Mechanism**

Readout Backplane – Status report

- ❑ All backplanes (24 different PCBs) are ready for production
 - Mechanical test OK
 - Electrical test OK
 - Integration Test: in SSW in progress,
with new RCU to be done
 - Production database submitted to several Manufacturers

- ❑ Test Bench for mass test ready

- ❑ Test Software in progress

- ❑ Production will start after integration test with final RCU (Feb '05)

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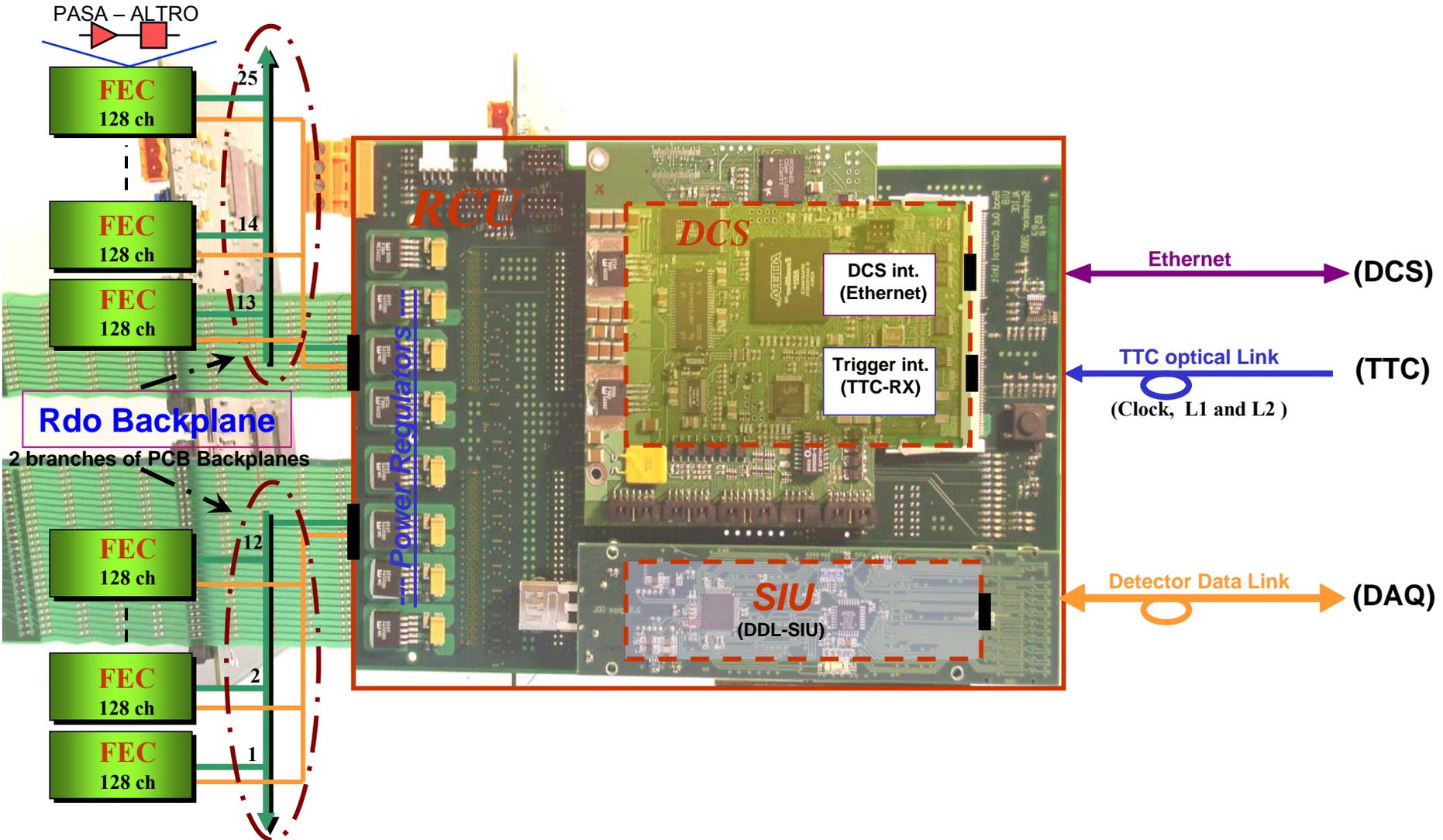
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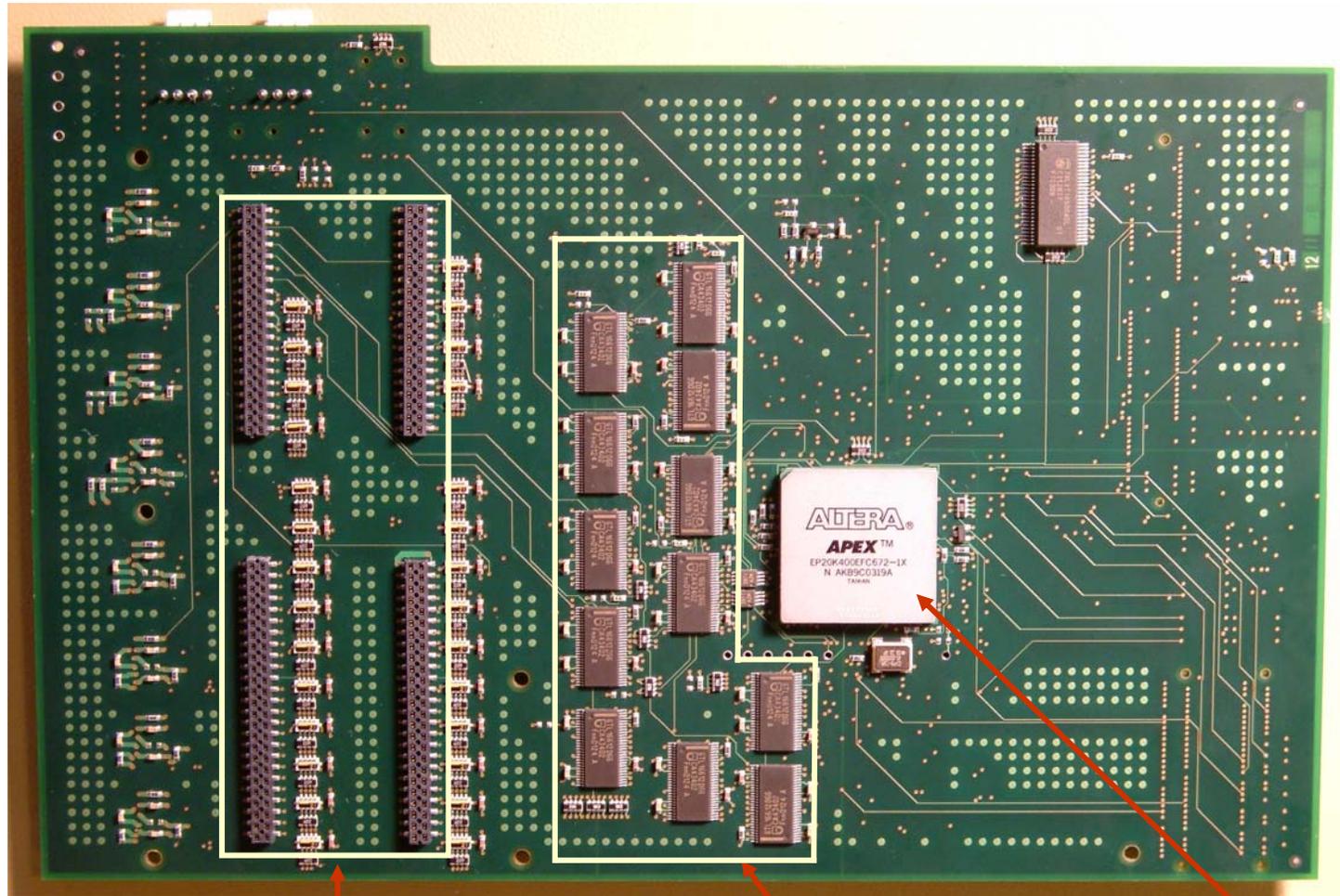
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FEE Architecture and Components: the Readout Control Unit



Readout Control Unit – Bottom Side



RCU to FECs
CONNECTORS

BUS
Transceivers

FPGA
Altera APEX20K400E

Readout Control Unit – FPGA Main Functions

– Readout related:

- FEE Initialization
- Distribution of the trigger and clock signals
- Dataflow control

*by the **ALTRO bus (VME-like custom bus)***

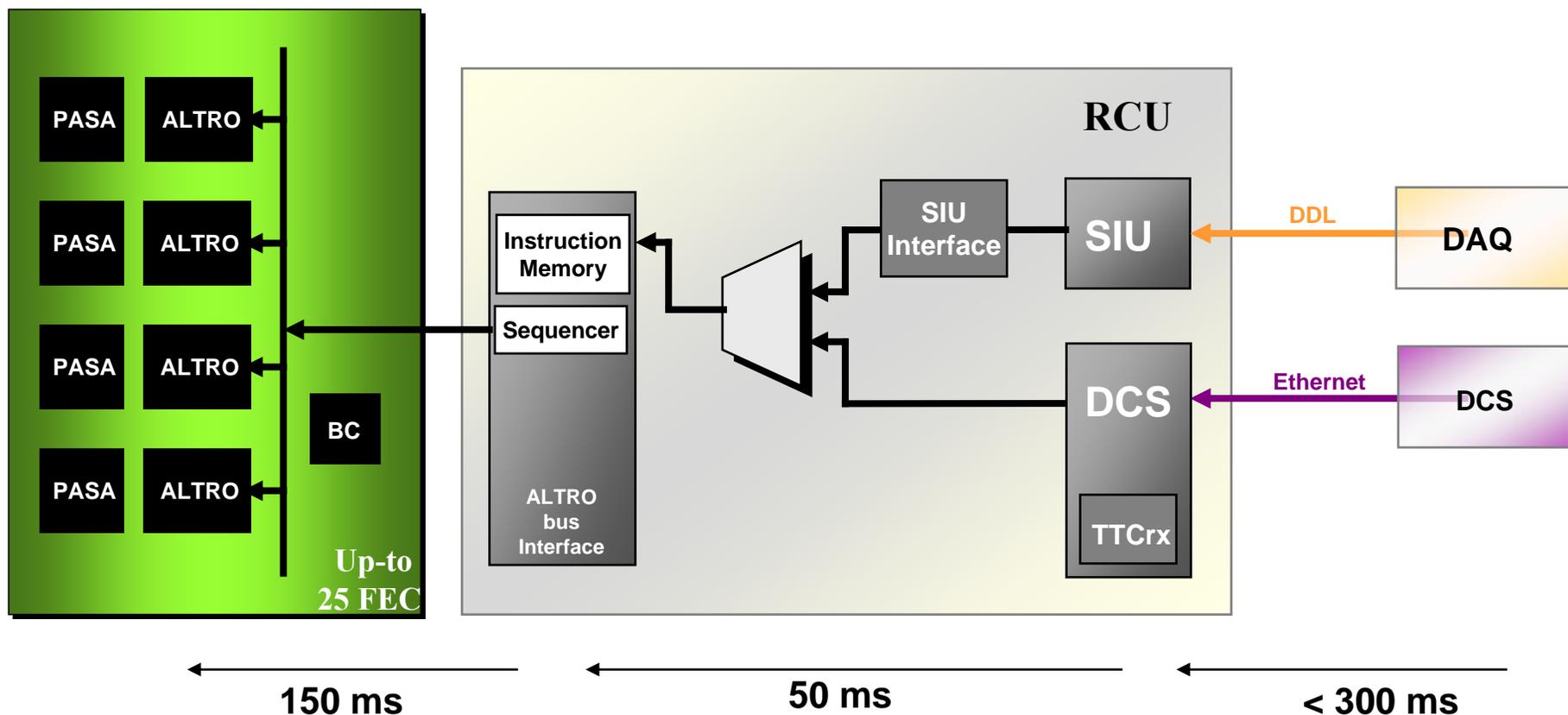
– Slow Control related:

- Supervision and monitoring:
 - FEE Power-on procedure
 - FEE Status parameters (Temperature, Voltages, Currents, Counters, ...)
 - Interrupt and error handling

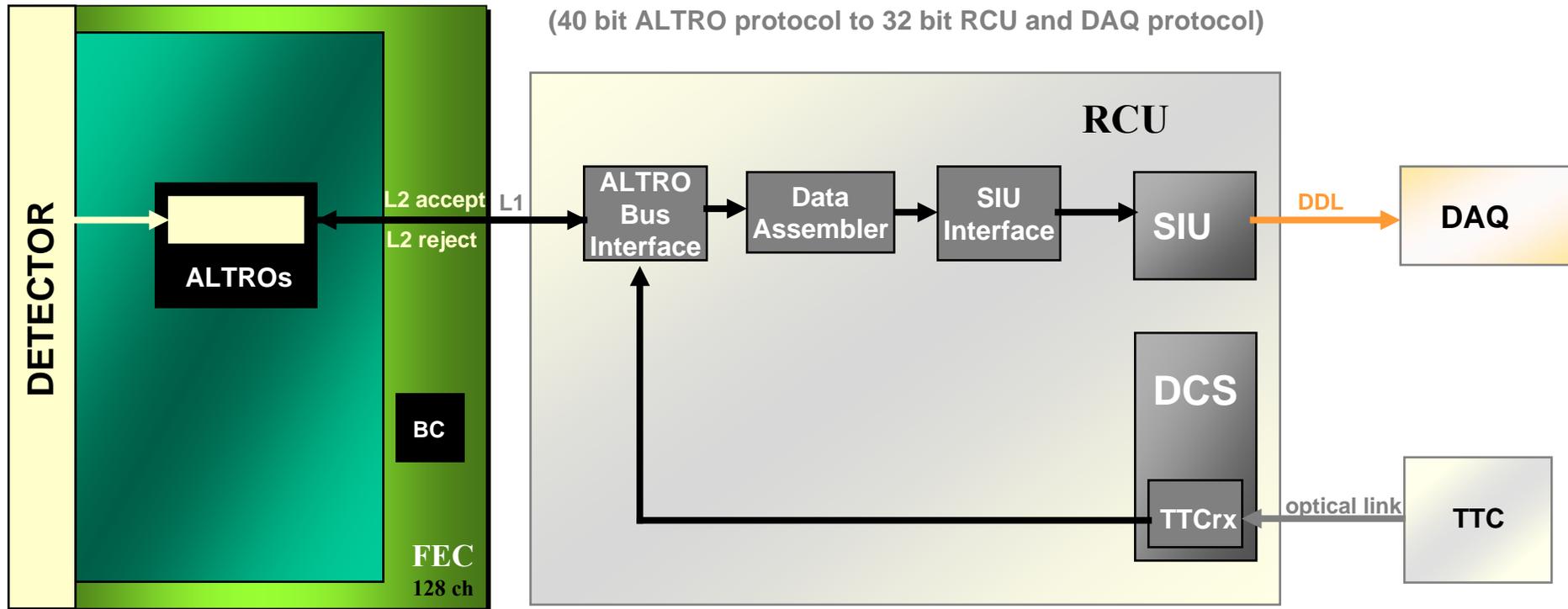
*by the **Local Slow Control bus (I2C-like custom bus)***

System Performance 1/3 : Initialization (set up time)

Typical configuration data per partition: 350 Kbytes ,
they can be transferred to the RCU both via the DDL or via the DCS link

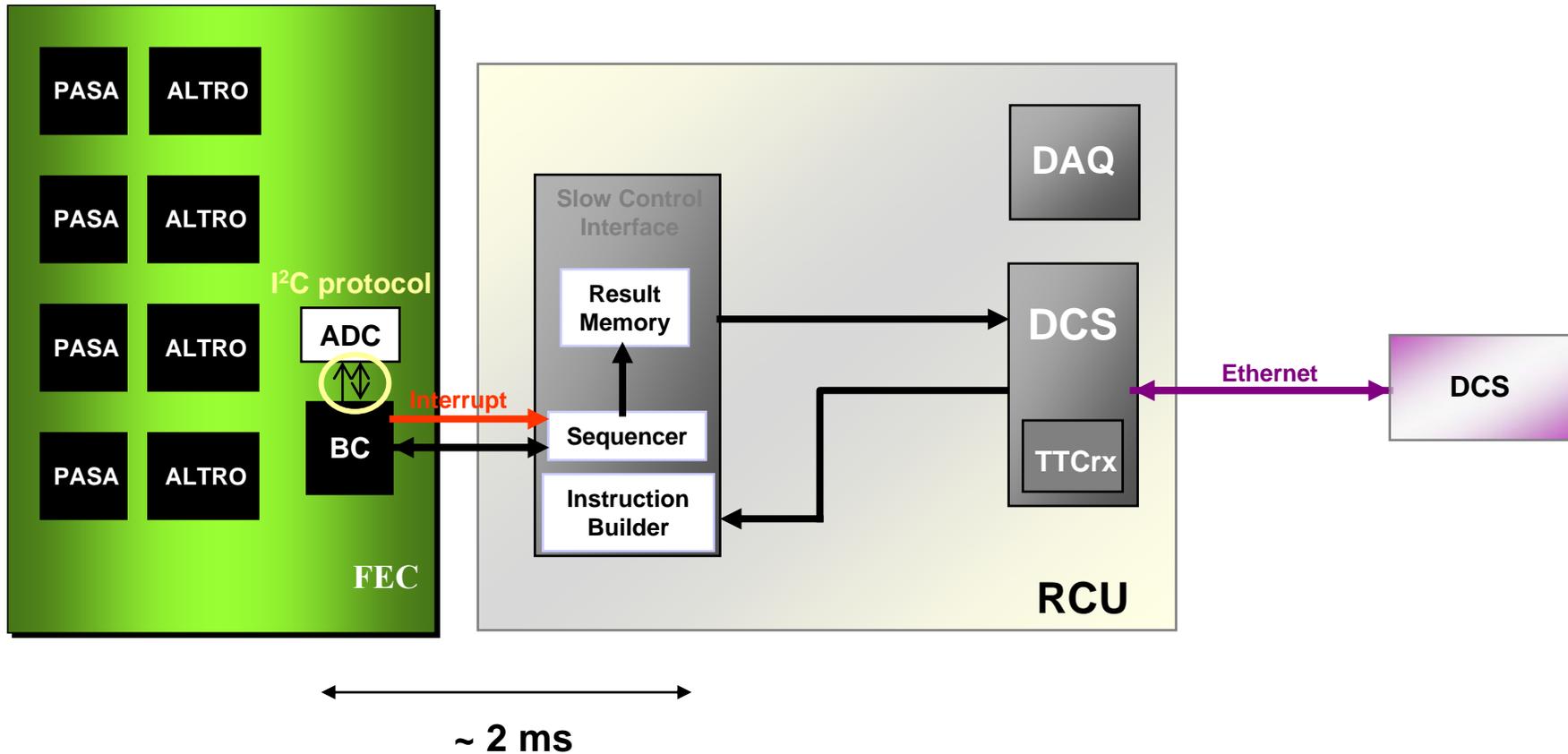


System Performance 2/3 : Data Readout (run time)



(The readout time is dependent by the event size)

System Performance 3/3 : Local Slow Control



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Readout Control Unit – Expected Single Event Upset in the 20K400E

- **SEU in RCU FPGA**

Expected numbers of SEUs for the different scoring regions in the TPC detector

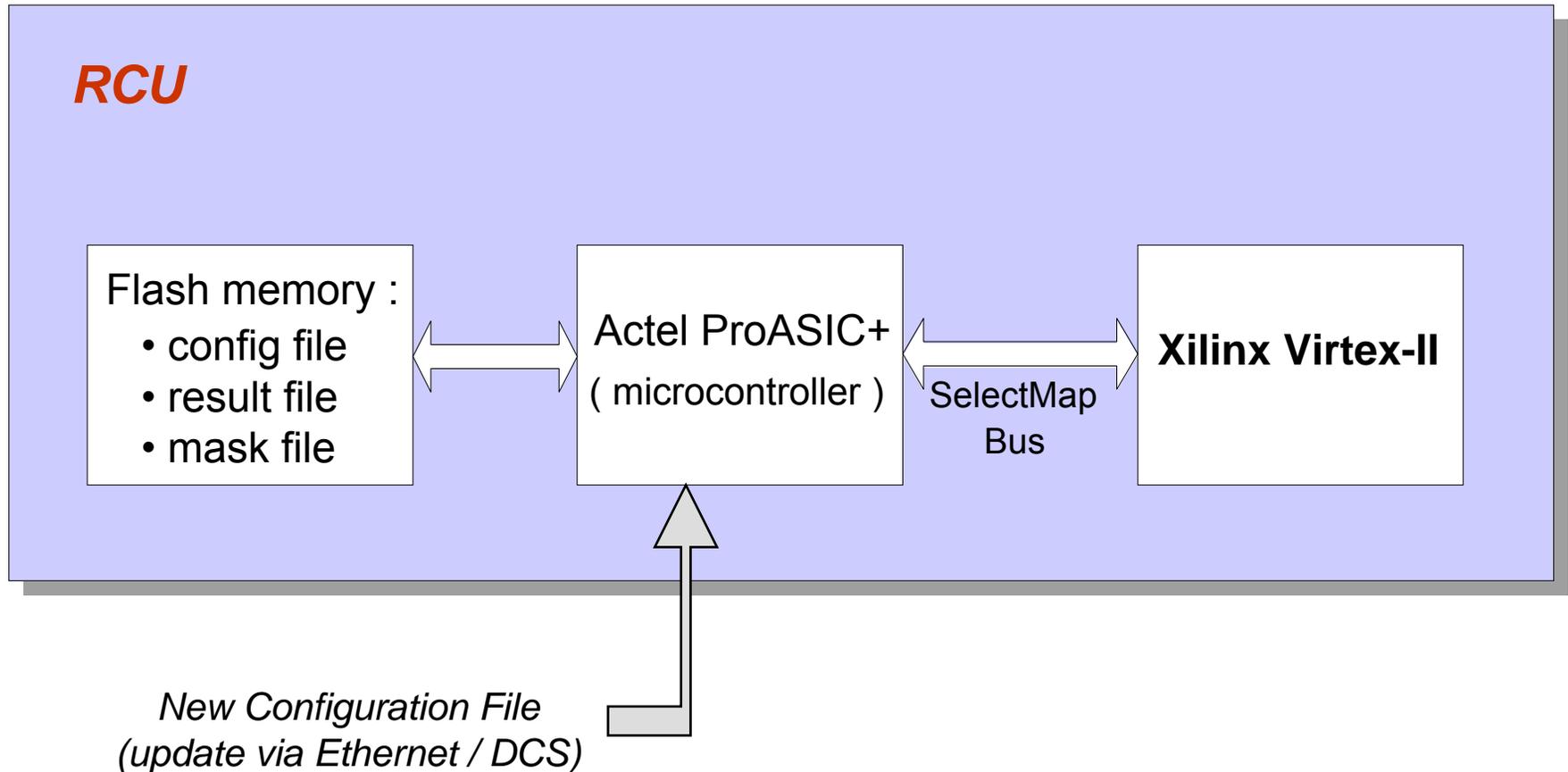
	μ -absorber side					
Sector	1	2	3	4	5	6
SEU/(FPGA s) [$\times 10^{-6}$]	2.4 ± 0.4	2.0 ± 0.4	1.6 ± 0.3	1.1 ± 0.2	0.9 ± 0.2	0.8 ± 0.1
	non-absorber side					
SEU/(FPGA s) [$\times 10^{-6}$]	1.6 ± 0.3	1.3 ± 0.2	0.9 ± 0.2	0.7 ± 0.1	0.6 ± 0.1	0.5 ± 0.1

- **Errors per run (4 hours) per TPC system**

RCU	3.7 (Altera Apex 20KE)
SIU	1.0 (Altera Apex, new version with Actel pAsic ready soon)
DCS	1.9 (Altera Excalibur, with ARM hardwired processor)

- SRAM based FPGAs
 - Error rate is so low that one can cope with it – if SEUs can be detected instantaneously and FPGA can be reconfigured in real-time
 - ALTERA FPGAs do not provide real-time readback of configuration data
 - Better choice: XILINX Virtex-IIPro FPGAs
 - Real-time (= while running) readback of configuration data for verification
 - Partial reconfiguration while running

Xilinx-based solution : Configuration Block Diagram

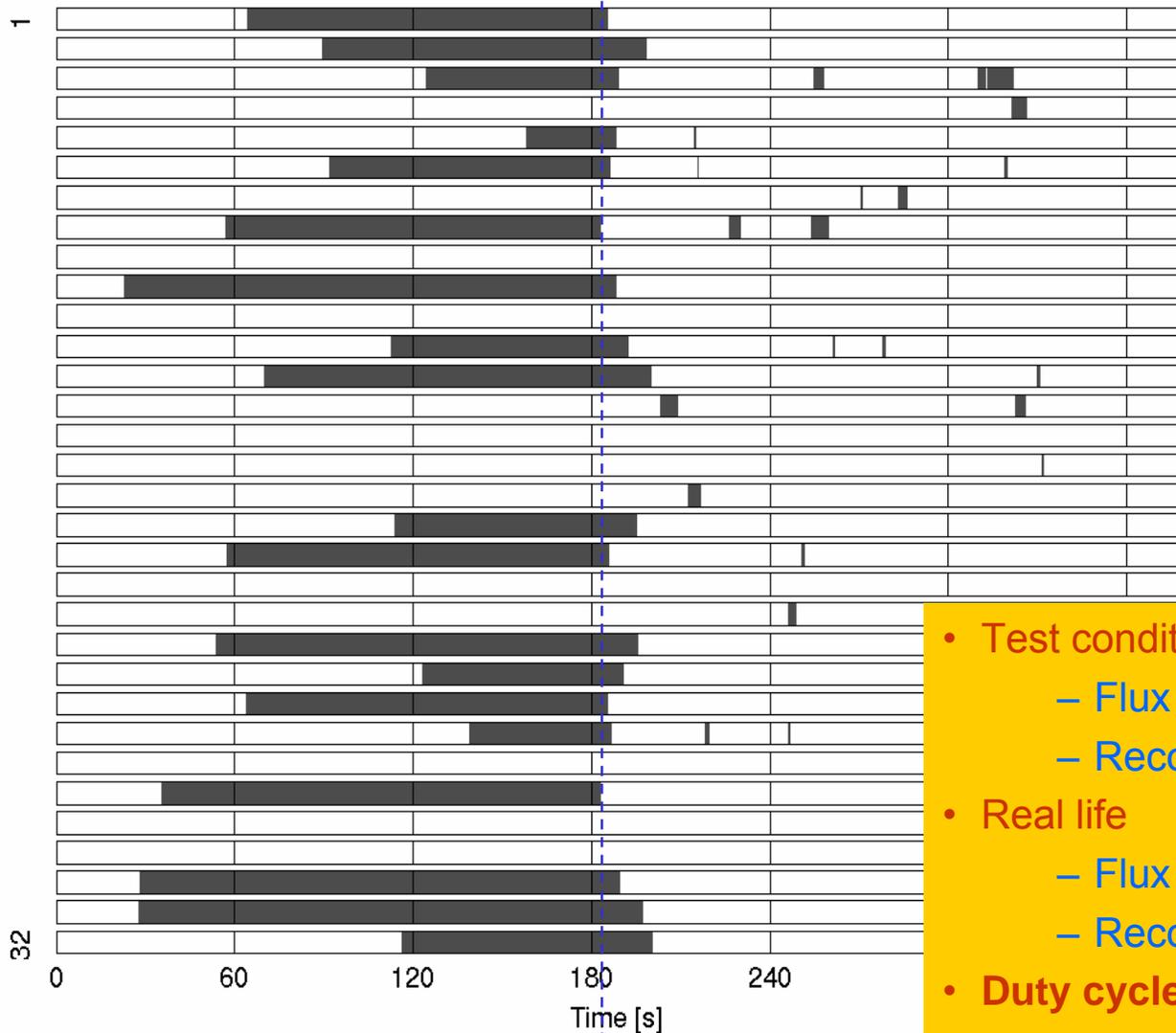


FPGA Radiation Tolerance Strategy 2/2

- Decide to migrate RCU-FPGA to XILINX
- Select appropriate device w.r.t. resources (e.g. number of I/O cells)
- Decide to keep DCS board unchanged (it can tolerate the possible failure rate)
- Port RCU design to new development environment
- Verify expected performance under irradiation :
 - XILINX test @ OCL in August
 - System test @ TSL Q1 2005 with large beam spot

Readout Control Unit – Xilinx FPGA radiation tests

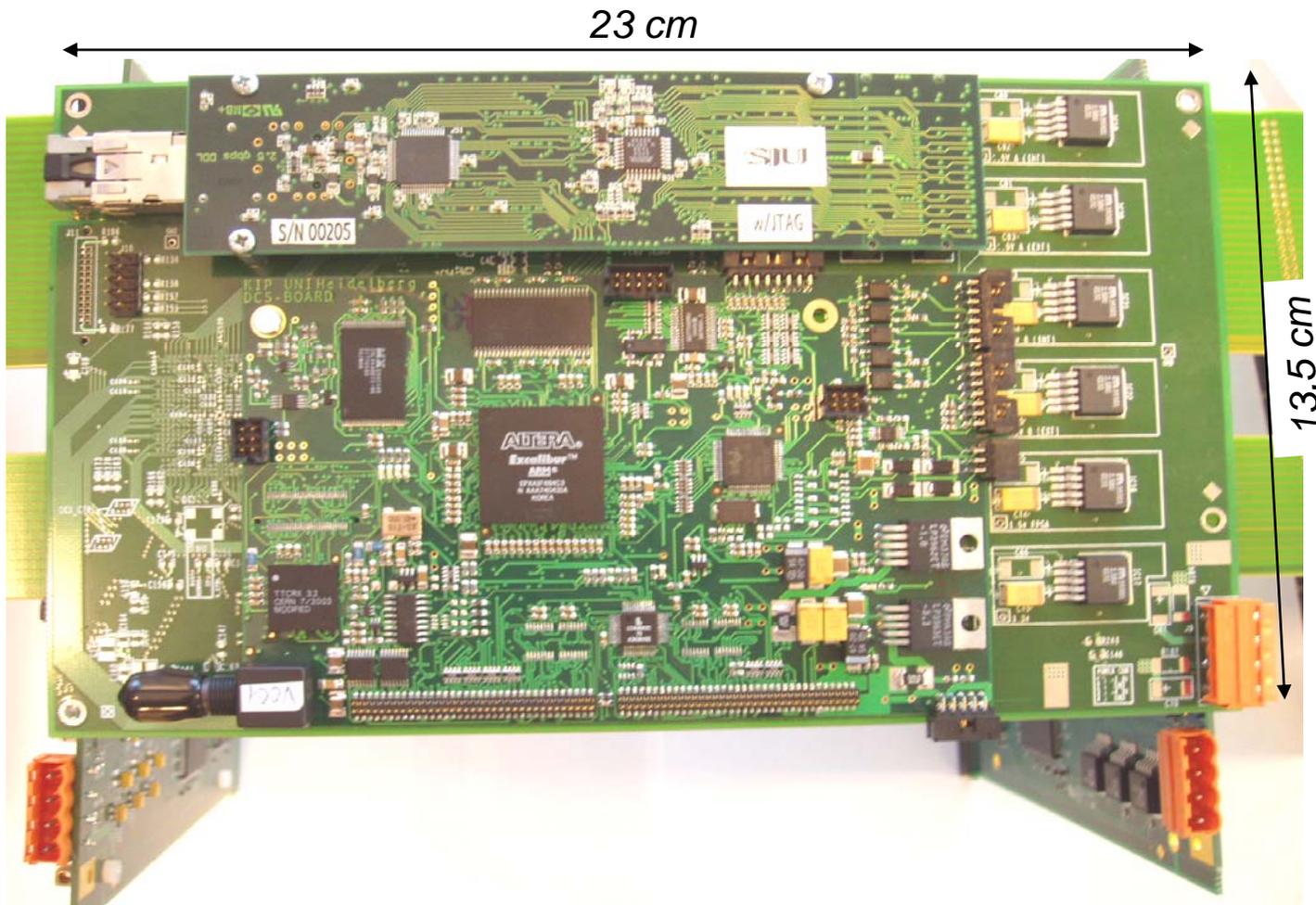
SEFI vs time, Flux: $1.5e7$ MeV/cm² s
Shiftregister design (32x300), starting repairing after half time



**Single Event Functional Interrupts
with Xilinx Virtex-II Pro FPGA
(Reconfiguration started after 200
seconds, errors are then
continuously detected and
corrected)**

- Test conditions
 - Flux = 3.7×10^{11} protons/cm²/s
 - Reconfiguration time = 5 s
- Real life
 - Flux = 7.9×10^2 hadrons/cm²/s
 - Reconfiguration time = 10 ms
- Duty cycle: 10^{11} times better in real life

New RCU – Final prototype



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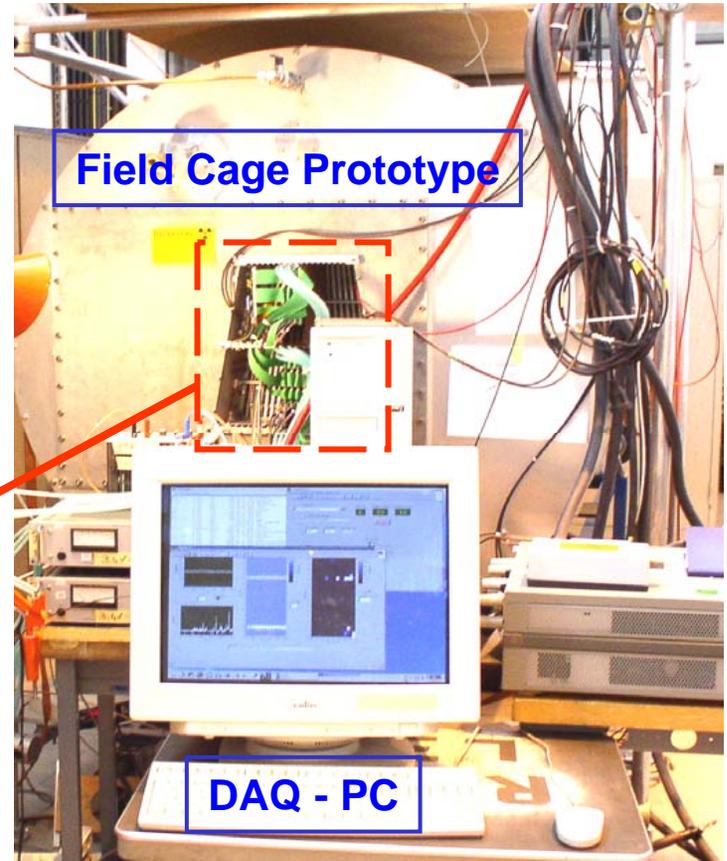
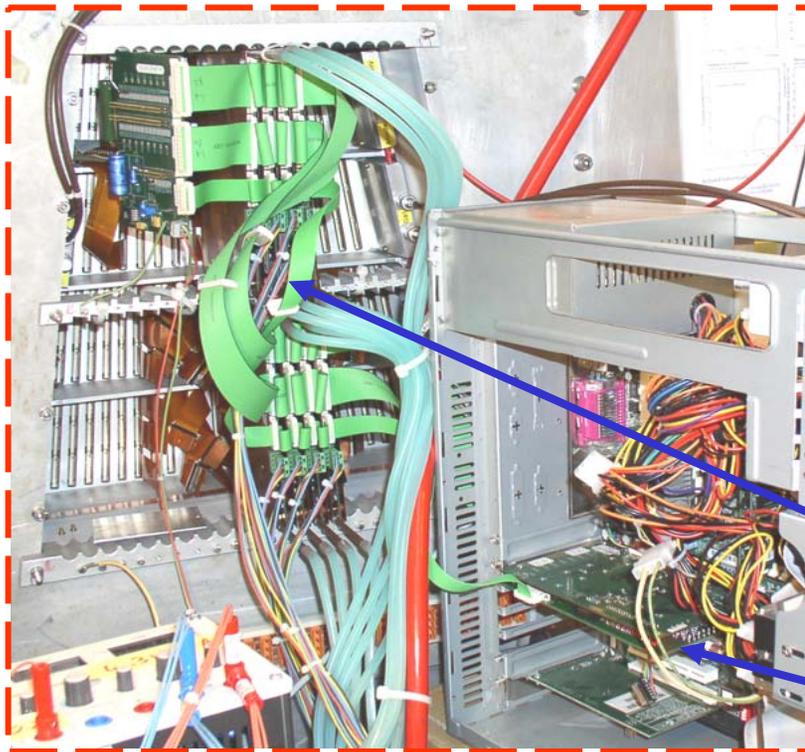
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hall 167 - Integration of FEE components with the Detector

TPC Test Facility at CERN (fall 2003 – spring 2004)

Inner Readout Chamber readout by
8 prototypes of Front End Card

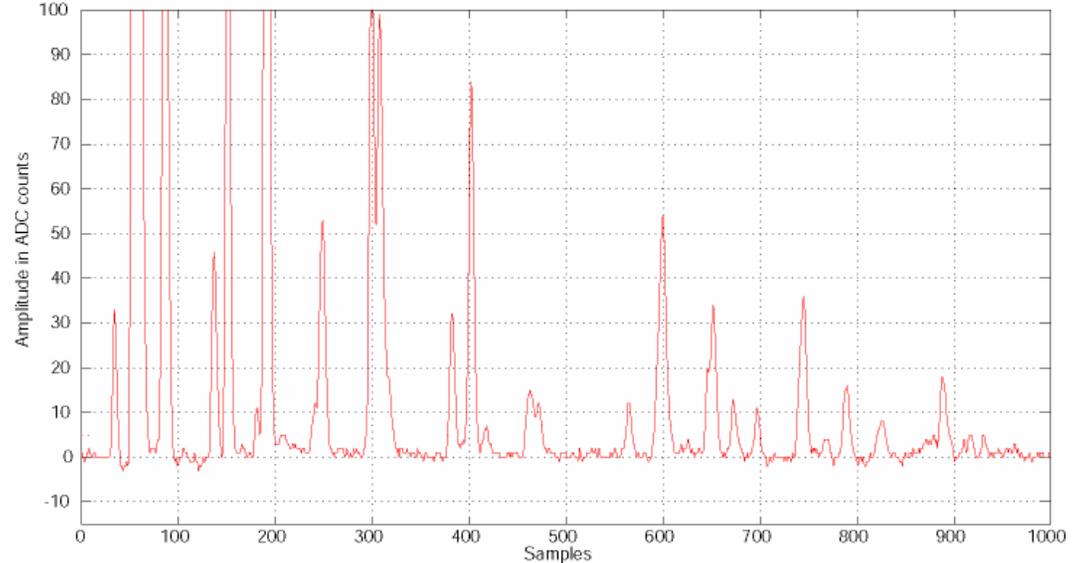


Front End Bus cables

Pci-based Readout Control Unit

First integration with the detector

Use of Cosmic Rays,
some of them generating high multiplicity events



On top of the Field Cage measurements under different conditions, the test allowed:

- To complete the PASA characterization
- To verify the performance of the Tail Cancellation and Moving Average Filters of the ALTRO
- To qualify the FEC grounding scheme.

(see *'TPC sector tests results'* by L. Musa and *'Cosmic ray measurements with TPC prototype'* by M.Kowalski and M.Ivanov in the previous Alice Clubs)

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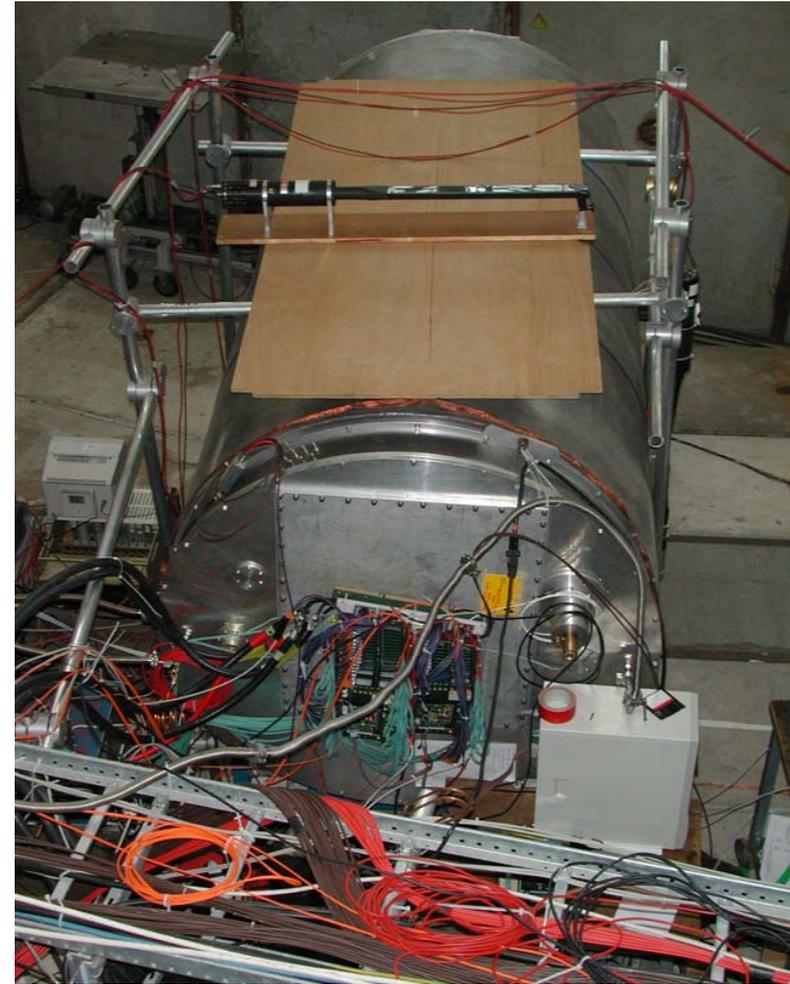
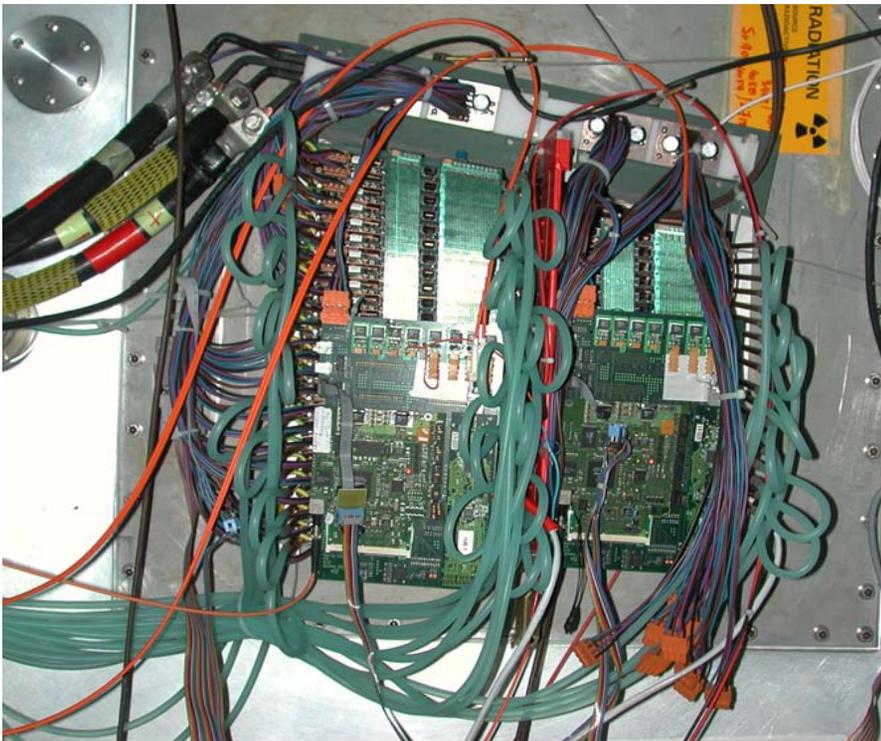
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Beam test @ CERN (T10)

Configuration for the Test-Beam (May 2004)

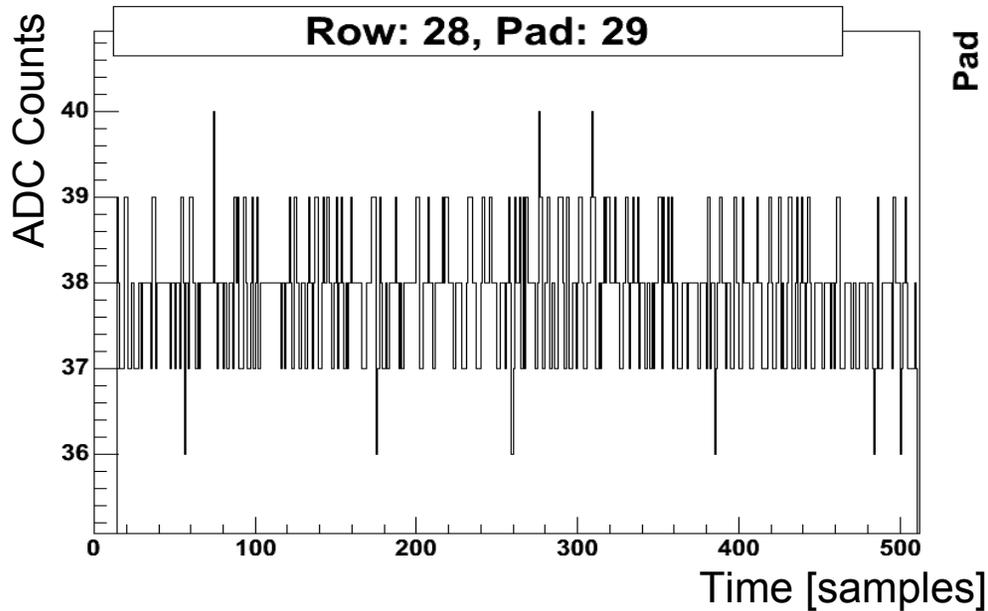
IROC in Field Cage prototype readout with:

- 43 FECs (5500 channels , ~1 % of Alice TPC) connected to
- 2 RCUs by
- 4 branches of ALTRO readout backplanes.
- 2 DCS boards interfaced to the RCUs and connected to the TTC,
- 2 SIUs for the DDL
- 'Realistic' Power supply distribution: Wiener500 with 40 m. cables

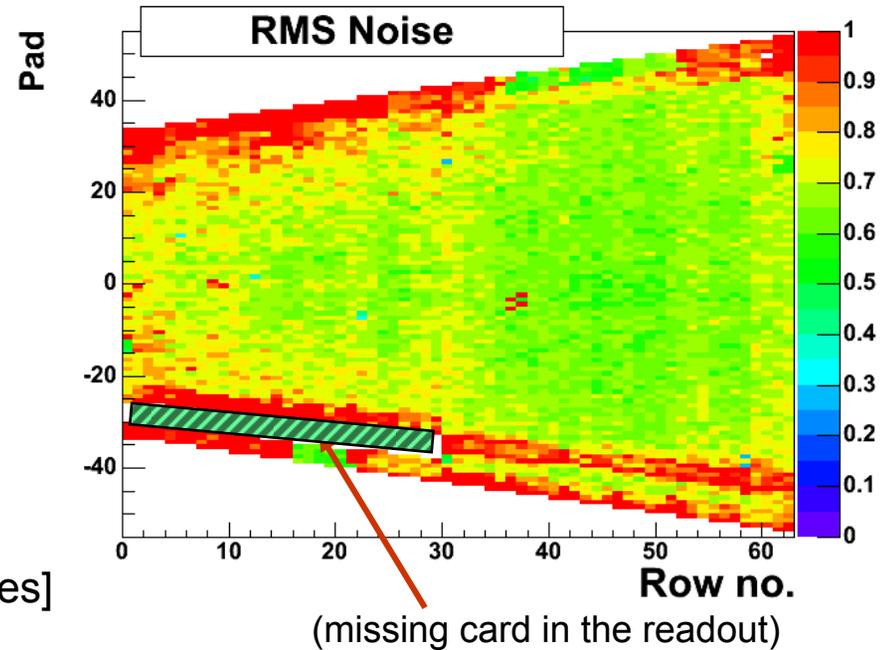


Noise Level

Example of a channel sampled at 10 MHz



Full IROC

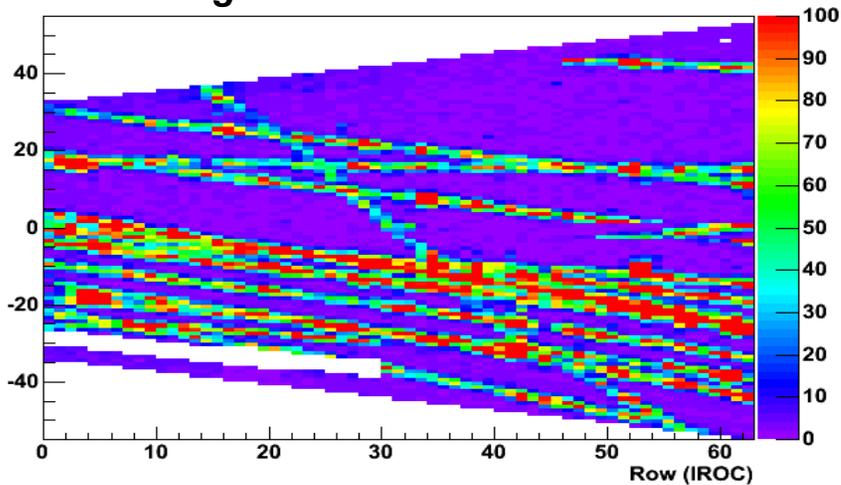


Noise average level : ~ 0.65 ADC counts (r.m.s.) $\approx 700 e^-$ [TDR: $<1000e^-$]

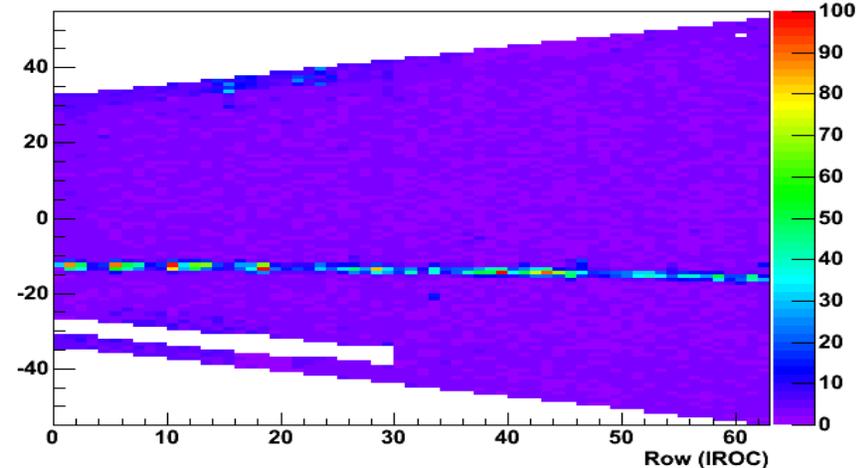
(Results from the T10 test beam activity reported by J. Baechler in the 22.11.04 Alice Club talk)

TPC On-line Monitor - Beam tracks

With target



Without target



On-line Monitor status:

- Recently upgraded to the latest version of DATE
- Completed the mapping of the IROC and OROC pads

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2004 has been a crucial year for the ALICE TPC Front End Electronics

Lot of progress, in particular :

Front End Card and main components:

- delivery and mass test of 49500 **PASA**
- mass test of 44000 **ALTRO** chip
- Integration of the Card with other detector components gave **excellent results**
- Mass production of 4800 cards, 400 of them already tested with yield higher than **90%**

The design of the **Readout Backplanes** has been **finalized**: mechanical and electrical tests fully satisfactory. Mass production of 950 units will start after completion of integration tests with the SSW and the final RCU)

The **final prototype** of the **Readout Control Unit** is now available for validation tests.

- ❑ Final RCU prototype validation (Feb / March 05)

- ❑ 6 FEE partitions - sector test @ Cern (March 05)

- ❑ Verify expected full system performance under irradiation
(System test @ TSL-Uppsala March 2005 with large beam spot)

- ❑ Mass Production and Test of the RCU (April – June 05)

- ❑ Mass Production and Test of the Backplanes (April – May 05)

Thank-you for your attention_

End of presentation